Analog Electronic Circuits

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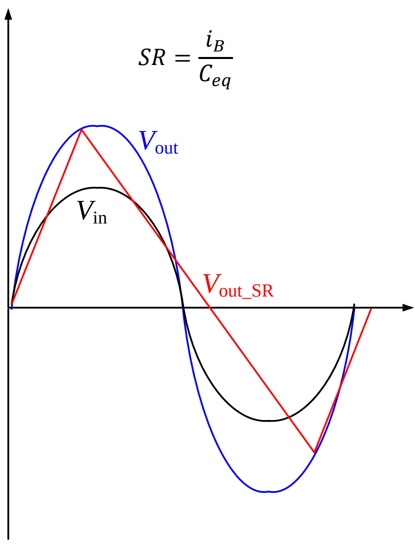
Lesson #4
Outline

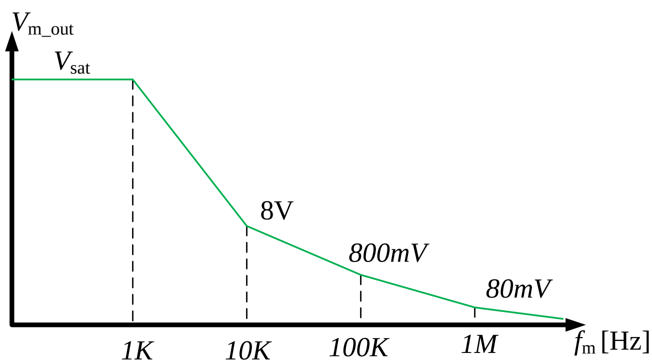
- Slew-rate (summary)
- Input Impedances
  - Differential
  - Common-Mode
- CMRR
- Effect of feedback on impedances
  - Blackman's theorem
  - Output
    - Current and voltage feedback
  - Input
    - Series and parallel summation
- Instrumentation amplifier
- Stability

Transient response
Slew-Rate

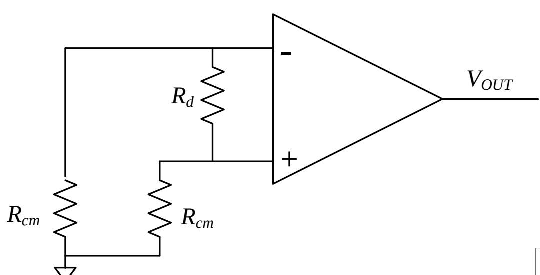
$$SR = \frac{i_B}{C_{eq}}$$

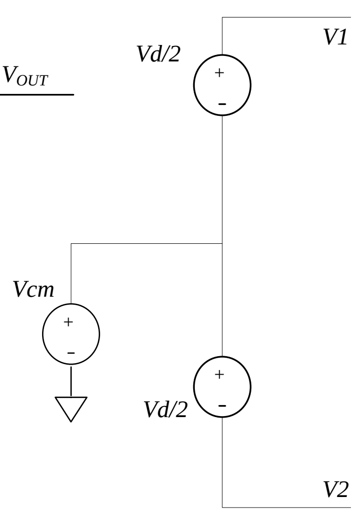


Sine wave $V_{m\_out} = min\left(\frac{SR}{2\pi f_m}, V_{sat}\right)$



Input Impedances

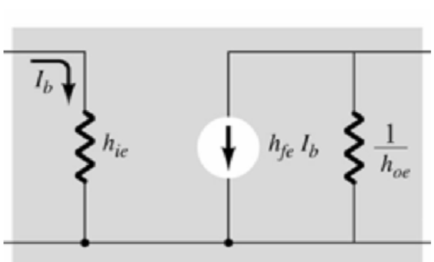


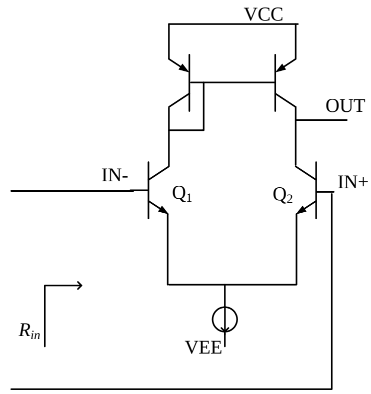


$$V_{cm} = \frac{V_1 + V_2}{2}$$
$$V_d = V_1 - V_2$$

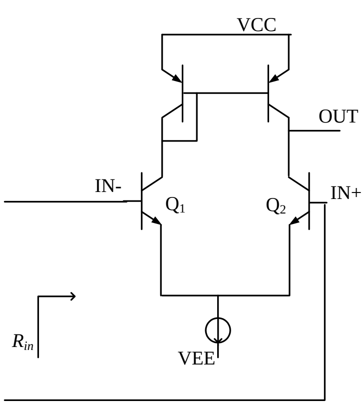
Input Impedances
Differential

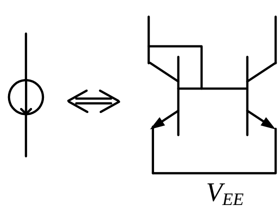
$$h_{ie} = \frac{V_T}{I_e}(h_{fe}+1)$$
$$R_d = 2h_{ie} = 2\frac{V_T}{I_e}(h_{fe}+1)$$





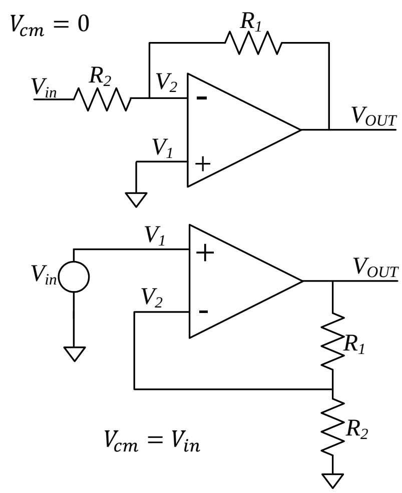
Input Impedances
Common-mode





$$R_e = \frac{1}{h_{oe}}$$
$$R_{cm} = 2R_e(h_{fe}+1)$$

Common-Mode Rejection Ratio (CMRR)

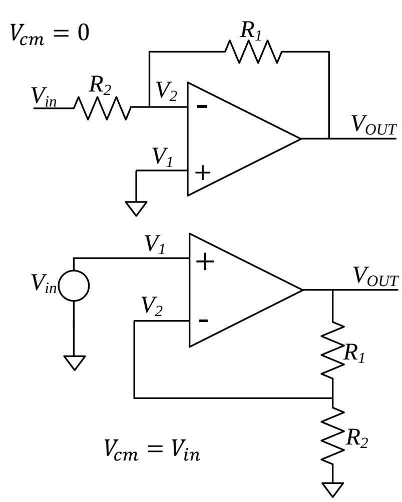


$$CMRR \equiv \frac{A_d}{A_{cm}} = \frac{A_d A_2 A_3}{A_{cm} A_2 A_3}$$

$$V_{cm} = \frac{V_1 + V_2}{2}$$
$$V_d = V_1 - V_2$$

$$V_{out\_cm} = A_{cm} V_{cm} = A_{cm} \frac{V_1 + V_2}{2}$$

Common-Mode Rejection Ratio (CMRR)



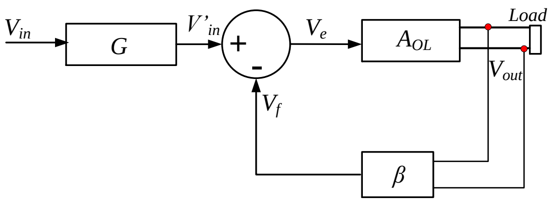
$$V_{out} = A_{cm} V_{cm} + A_d V_d$$

$$\frac{V_{out}}{A_d} = \frac{V_{cm}}{CMRR} + V_d$$

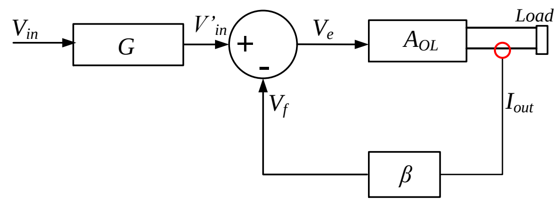
Reflected to input
(as done to ALL non-idealities)

Blackman's Theorem

$$Z_F = Z_{NF}\frac{1+\beta A_{SC}}{1+\beta A_{OC}}$$



Voltage feedback



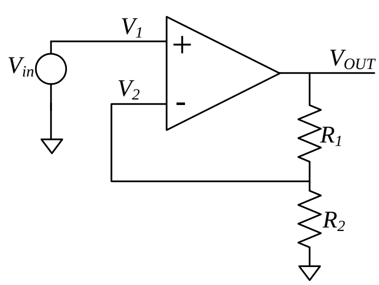
Current feedback

$$Z_F = \frac{Z_{NF}}{(1+\beta A)}$$

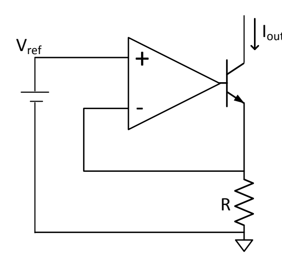
$$Z_F = Z_{NF}(1+\beta A)$$

Effect of feedback
Output impedance

Voltage feedback



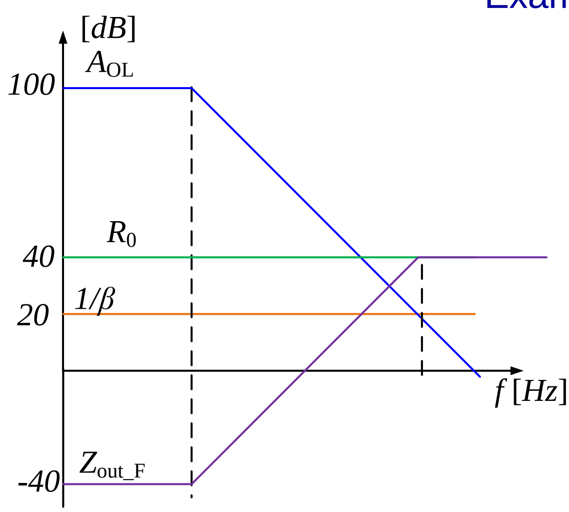
Current feedback

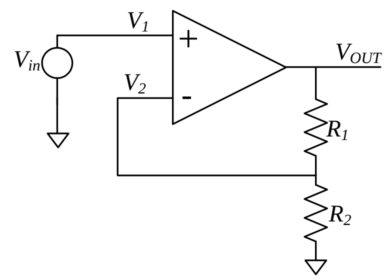


$$Z_{out\_F} = R_0\frac{1+\cancel{\beta A_{SC}}}{1+\beta A_{OC}}$$

$$Z_{out\_F} = R_0\frac{1+\beta A_{SC}}{1+\cancel{\beta A_{OC}}}$$

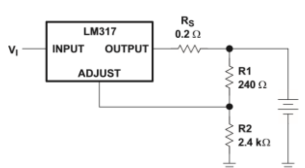
Effect of feedback
Example

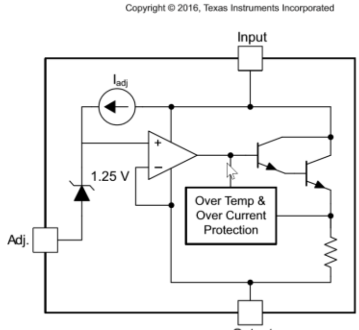


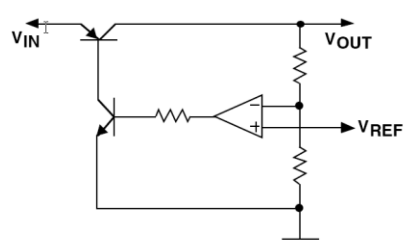


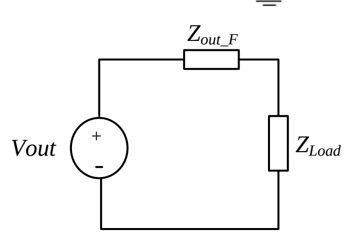
R1=10k
R2=1k
R0=100

Linear regulator
Low-Drop Out (LDO)

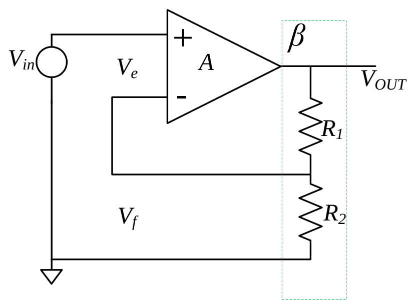






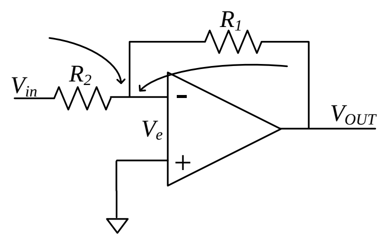


Effect of feedback
Input impedance



Series (voltage) summation

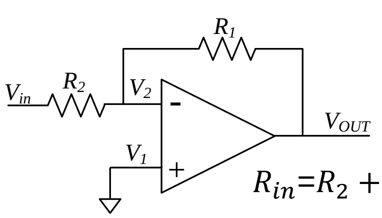
$$Z_{in\_F}=Z_{NF}(1+\beta A)$$



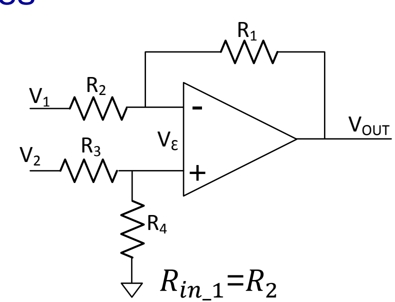
Parallel (current) summation

$$Z_{in\_F}=\frac{Z_{NF}}{(1+\beta A)}$$

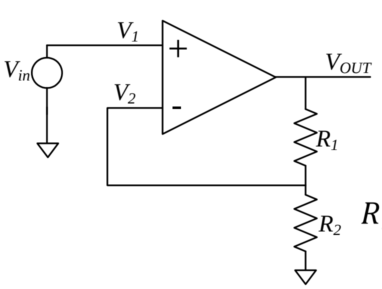
Input Impedances



$$R_{in}=R_2+\frac{R_1+r_O}{(1+\beta A)}\approx R_2$$

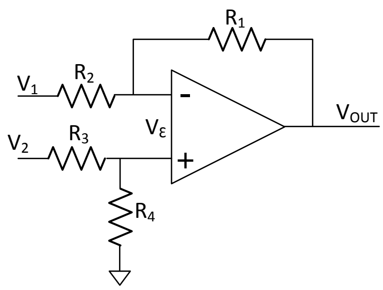


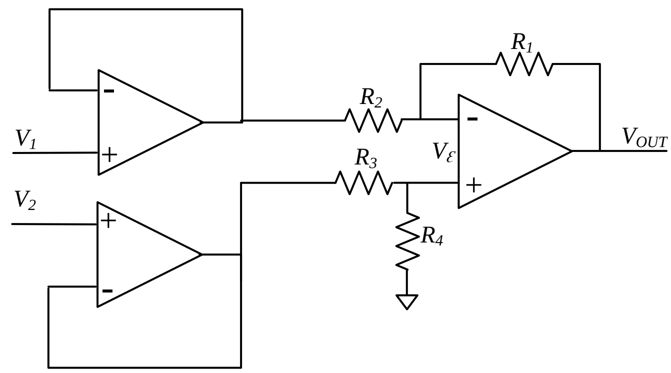
$$R_{in\_1}=R_2$$
$$R_{in\_2}=R_3+R_4$$
$$R_{in\_1,2}=R_2+R_3$$



$$R_{in}=R_d(1+\beta A)$$

Difference Amplifier





$$V_{out\_1} = -V_1\left(\frac{R_1}{R_2}\right)$$

$$V_{out\_2} = V_2\left(\frac{R_4}{R_3+R_4}\right)\left(1+\frac{R_1}{R_2}\right)$$

$$\frac{R_2}{R_1} = \frac{R_3}{R_4}$$

$$V_{out} = \frac{R_1}{R_2}(V_2 - V_1)$$

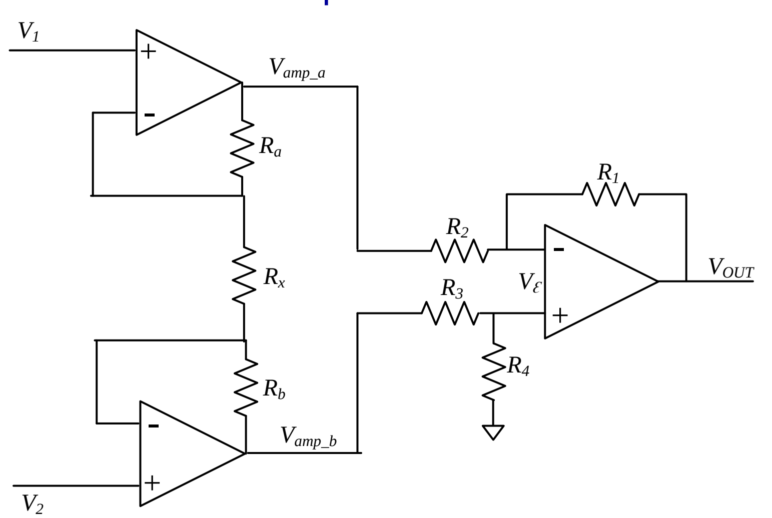
Instrumentation Amplifier

$$V_{out} = \frac{R_1}{R_2}(V_{amp\_b} - V_{amp\_a})$$

$$I_x = \frac{V_1 - V_2}{R_x}$$

$$V_{amp\_b} - V_{amp\_a} = I_x(R_x + R_a + R_b)$$

$$V_{out} = \frac{R_1}{R_2}(V_2 - V_1)\left(1+\frac{R_a+R_b}{R_x}\right)$$

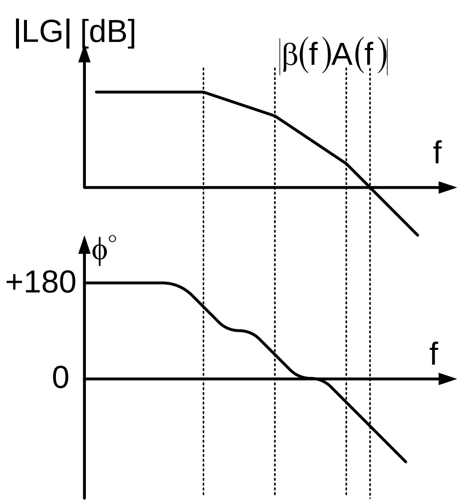


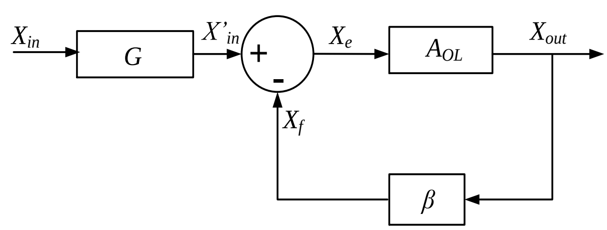
Loop-Gain
Nyquist Criterion

$$A_{CL} = G(s)\frac{A_{OL}(s)}{1+\beta A_{OL}(s)}$$

- The system is unstable if the characteristic equation $\{1+\beta A_{OL}(s)\}$ has roots in the right half of the complex plane
- Nyquist criterion is a test for location of $\{1+\beta A_{OL}(s)\}$ roots
- Nyquist criterion can be viewed on the frequency domain (Bode)

Loop-gain on the frequency domain

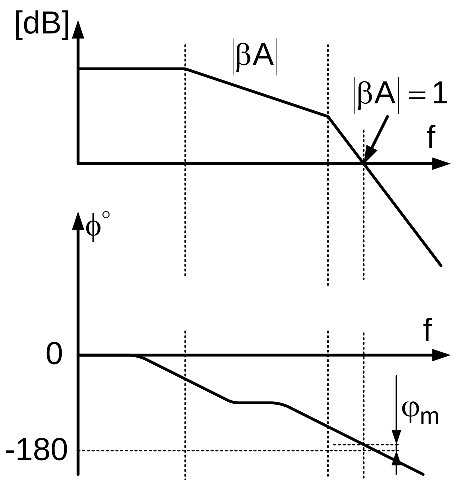




In negative feedback systems $\phi = 180^{o}\,(-180^{o})$

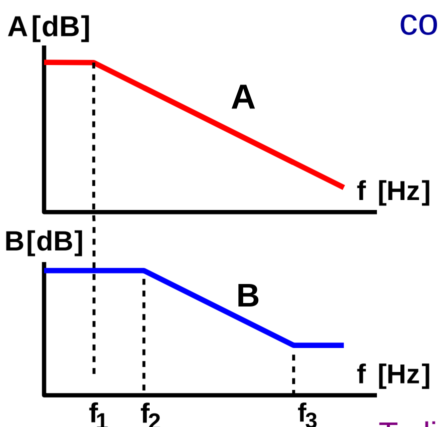
At $f \rightarrow 0$

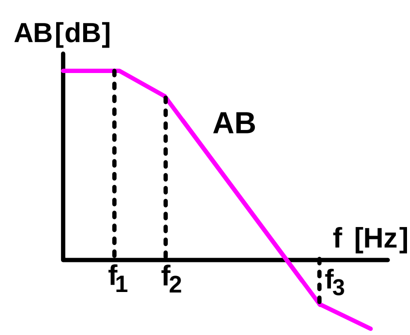
Bode plot
Phase margin



$$\varphi_m = \varphi_{|\beta A|=1} - (-180^\circ) = \varphi_{|\beta A|=1} + 180^\circ$$

Graphical representation of βA_{OL}
conventional method



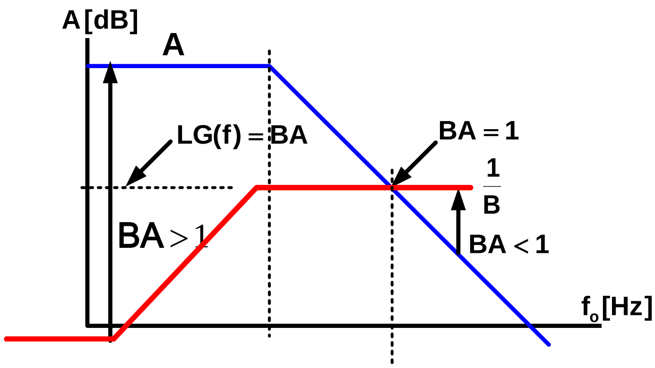


- Tedious – need to re-plot BA
- Analysis (not design) oriented
- Requires iterations

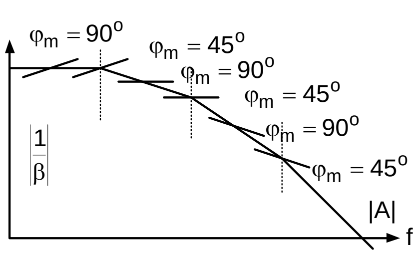
Graphical Representation of βA_{OL}

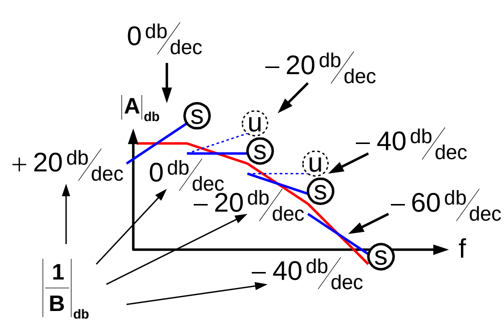
$$20\log A - 20\log\frac{1}{B} = 20\log(BA)$$

$$20\log A = 20\log\frac{1}{B} \Rightarrow B\cdot A = 1$$

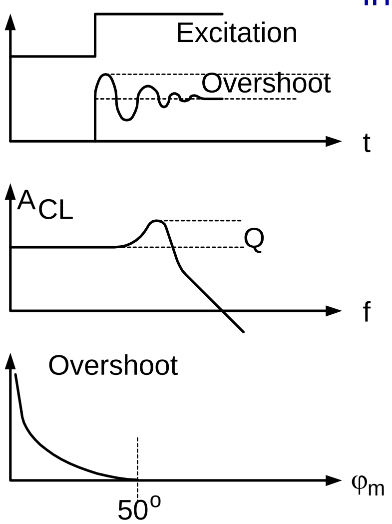


Possible compensations
Rate of Closure (ROC)





Overshoot and Q in Closed Loop in Response to step in S_{in}



$$Q \cong \frac{\sqrt{\cos\varphi_m}}{\sin\varphi_m} \quad \text{for} \quad \varphi_m < 50^o$$

Design target $\varphi_m \geq 45^o$