# A Novel Soft switching ZVS, Sinusoidal Input Boundary Current Mode Control of 6-switch Three Phase 2-level Boost Rectifier for Active and Active + Reactive Power Generation

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***Abstract*— Recent advancements in semiconductor technology and the commercial availability of low on resistance and parasitic capacitors wide bandgap devices (SiC & GaN) has led power electronics systems to achieve efficiency as high as 99% for three phase boost PFC rectifier systems. However, this high efficiency is attainable only for rectifiers running at low switching frequencies (<70 kHz) as these converters operate in hard switching continuous conduction mode (CCM). Turn-on losses become dominant for high switching frequency operation with CCM. The trend for increasing switching frequency is driven by the fact that high switching frequency operation leads to significant reduction in filter size but high switching frequency operation is only feasible with soft switching ZVS turn-on control. Critical conduction mode (CRM) with ZVS turn-on has considerably high efficiency for single phase boost PFC at very high switching frequencies (>1 MHz). However, conventional boundary conduction mode (BCM)/CRM for three phase rectifier systems, does not generate sinusoidal average input current. A Zero Voltage Switching (ZVS) BCM control with sinusoidal input current for three phase 2-level converter is presented in this paper. This paper covers unity power factor (u.p.f.) operation, active + reactive power and also purely reactive power generation cases. The control scheme is presented in detail and ZVS turn-on operation is also discussed. The simulation and experimental results are discussed in the end. For a 1.2 KW converter, power density achieved by >500 kHz switching frequency operation is ~80 W/in$^3$ and with soft switching, 99 % efficiency is maintained.**

**Keywords— Boundary Conduction Mode (BCM), Critical Conduction Mode (CRM), Triangular Current Mode (TCM), Discontinuous Conduction Mode (DCM), Zero Voltage Switching (ZVS), Sinusoidal Input Current, 6-Switch Three Phase 2-Level Converter, Unity Power Factor (u.p.f.), Active + Reactive Power, Purely Reactive Power, Sinusoidal Input Current Control (S.I.C.C)**

## I. INTRODUCTION

The switching frequency of three phase boost type rectifier (shown in Fig. 1) systems in continuous conduction mode (CCM) is limited by the switching loss of devices. The major contribution to these switching losses is from turn-on losses as turn-off losses of wide bandgap devices (SiC and GaN) are significantly lower [3]. Though in discontinuous conduction mode (DCM), the transistor can be turned on at zero current, but in general no zero voltage turn-on is present. Also, in DCM, if the duty cycle is constant in a line cycle, the average value of the inductor current in a line cycle is not sinusoidal. However, varying the switching frequency so that converter always operates on the boundary of CCM and DCM, also referred to as boundary conduction mode (BCM) or critical conduction mode (CRM) leads to lower input current harmonic distortion and also ZVS turn-on can be achieved by driving current to a small negative value, such that it is enough to discharge the transistors output capacitors. ZVS turn-on is achieved in BCM by making the body diode conduct before the device is turned on, thus it is necessary to have a bidirectional current in one switching cycle.

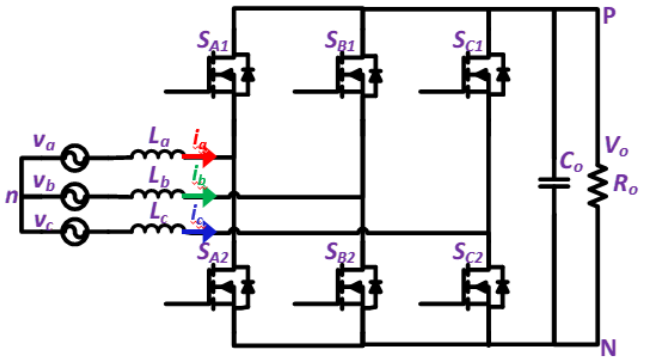



Fig. 1. Circuit Schematic of Three phase 6-switch 2-level boost converter

Conventional CRM for a three phase single switch boost PFC does not generate sinusoidal average input current as is discussed in [1] and [2]. The detailed basic operation of conventional CRM and its issues are discussed in section II. This issue is addressed in [2] for a Vienna Rectifier (VR) operating as PFC and it is shown that sinusoidal average input current can be achieved by adding one more switching state in between three switching states of conventional CRM. The three phase 6-switch boost converter has lesser semiconductors and hence lower losses as compared to VR. However, the above

modulation cannot be directly applied to a three phase 6-switch 2-level boost converter as it has more transistors to control and also the current slopes are entirely different for the two topologies.

A new BCM/TCM control with different switching states, complete ZVS turn-on and sinusoidal average input current for three phase 6-switch 2-level boost PFC is presented in this paper. The detailed operation and switching states are discussed in section II. This modulation is further extended for varying power factors, two cases- active + reactive power and purely reactive power, are elaborated in section III. The hardware implementation of the control schemes presented is discussed in Section IV.

## II. Unity Power Factor Theory

### A. Conventional CRM

The conventional CRM operation for three phase rectifier is discussed in detail in [1]. The line cycle can be divided into 12 sectors as shown in Fig. 2(a), where in each sector, the voltage direction and relative magnitude of the three phase input voltage is same. The input voltages are given by:

$$v_a = V_m \sin(\omega t) \quad (1a)$$

$$v_b = V_m \sin(\omega t - 2\pi/3) \quad (1b)$$

$$v_c = V_m \sin(\omega t + 2\pi/3) \quad (1c)$$

One switching cycle waveform in sector I ($0<\omega t<\pi/6$) is shown in Fig. 2(b). Each switching cycle can be divided into 3 intervals. The input voltages are assumed to be constant for one switching cycle as the switching frequency ($f_{sw}$) >> line cycle frequency.

(1) *Switching Mode* 1 (0-$T_1$)

During switching mode 1, $S_{A1}$, $S_{B1}$, $S_{C1}$ conduct and the phase currents increase directly proportional to respective phase voltages. The equivalent circuit is shown in Fig. 2(c), the phase currents' slopes are given by:

$$di_a/dt = v_a/L \quad (2a)$$

$$di_b/dt = v_b/L \quad (2b)$$

$$di_c/dt = v_c/L \quad (2c)$$

After $i_b$ reaches peak current $i_{bp1}$, $S_{B1}$ is turned off, resonance occurs between $L_b$ and devices' capacitors, $V_{dsB2}$ reaches zero and $S_{B2}$ is turned on at 0 V $V_{ds}$.

(2) *Switching Mode* 2 ($T_1$-$T_1$+$T_2$)

During switching mode 2, $S_{A1}$, $S_{B2}$ and $S_{C1}$ are on, the equivalent circuit is shown in Fig. 2(d). The phase currents' slopes are given by:

$$di_a/dt = (v_a - V_o/3)/L \quad (3a)$$

$$di_b/dt = (v_b + 2V_o/3)/L \quad (3b)$$

$$di_c/dt = (v_c - V_o/3)/L \quad (3c)$$

This mode ends when $i_a$ reaches zero as $v_a$ is minimum in magnitude in sector I. $S_{A2}$ is turned off at the end of *Mode* 2.

(3) *Switching Mode* 3 ($T_1$+$T_2$-$T_1$+$T_2$+$T_3$)

In this mode, $S_{B2}$ and $S_{C1}$ conduct, the equivalent circuit is shown in Fig. 2(d). The phase currents' slopes are given by:

$$di_b/dt = -di_c/dt = (V_o + v_b - v_c)/2L \quad (4)$$

This mode ends when $i_c$ and $i_b$ reach zero. After $i_b$ reaches zero, $S_{B2}$ is turned off, resonance occurs between $L_B$ and output source capacitors of devices such that $V_{dSB1}$ reaches 0 and $S_{B1}$ is turned on at 0 V $V_{ds}$. This marks the beginning of a new switching cycle.

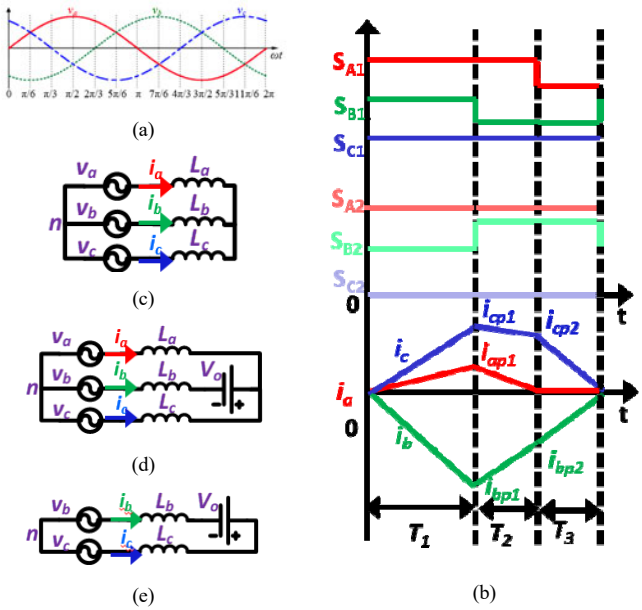



Fig. 2 (a) Line cycle divided into 12 sectors (b) Switching cycle waveform in Sector I (c) Equivalent circuit in switching mode 1 (d) Equivalent circuit in switching mode 2 (e) Equivalent circuit in switching mode 3

$T_2$ and $T_3$ can be obtained in terms of $T_1$ from volts sec balance of $i_a$ and $i_c$. Average phase currents can be calculated from area integral of the current waveforms and the calculated average currents are equated to the sinusoidal currents required given by:

$$i_a = I_m \sin(\omega t) = k_1 v_a \quad (5a)$$

$$i_b = I_m \sin(\omega t - 2\pi/3) = k_1 v_b \quad (5b)$$

$$i_c = I_m \sin(\omega t + 2\pi/3) = k_1 v_c \quad (5c)$$

where

$$k_1 = I_m / V_m \quad (6)$$

Since there is only one control variable ($T_1$) in conventional CRM, only one phase current can be controlled for sinusoidal average values, thus resulting in a distortion in average currents with a distortion factor of 0.97. Hence it is required to insert another switching mode in one switching cycle as is proposed in [2] for Vienna rectifier.

### B. S.I.C.C. CRM/TCM

Conventional CRM can be modified to achieve sinusoidal currents by inserting one more switching mode such that it

gives us two control variables to control two average currents, since the sum of all the three phase currents is always zero, the third phase average current also becomes sinusoidal. Each switching cycle can be divided into 9 intervals as shown in Fig. 3(a).

*Interval* I (0-$T_1$)

During interval 1, $S_{A2}$, $S_{B2}$, $S_{C2}$ conduct, the equivalent circuit is shown in Fig. 3(b), the phase currents' slopes are given by:

$$di_a / dt = v_a / L \quad (7a)$$

$$di_b / dt = v_b / L \quad (7b)$$

$$di_c / dt = v_c / L \quad (7c)$$

After $i_c$ reaches $i_{cp1}$, $S_{C2}$ is turned off as shown in Fig. 3(a).

*Interval* II ($T_1$-$T_1$+$t_{d1}$)

After $S_{C2}$ is turned off, resonance occurs in between phase C devices' output source capacitors ($C_{oss}$) and $L_c$ as shown in Fig. 4(a). By the end of this interval, $V_{dsC2}$ reaches $V_o$ and $V_{dsC1}$ reaches 0 (as shown in Fig. 3(a)), the body diode of $S_{C1}$ starts conducting and the switch can be turned on at 0 V.

*Interval* III ($T_1$+$t_{d1}$-$T_1$+$t_{d1}$+$T_2$)

At the beginning of interval III, $S_{C1}$ is turned on, the equivalent circuit is shown in Fig. 3(c), the phase currents' slopes are given by:

$$di_a / dt = (v_a + V_o / 3) / L \quad (8a)$$

$$di_b / dt = (v_b + V_o / 3) / L \quad (8b)$$

$$di_c / dt = (v_c - 2V_o / 3) / L \quad (8c)$$

After $i_a$ reaches $i_{ap2}$, $S_{A2}$ is turned off as shown in Fig. 3(a).

*Interval* IV ($T_1$+$t_{d1}$+$T_2$- $T_1$+$t_{d1}$+$T_2$+$t_{d2}$)

After $S_{A2}$ is turned off, resonance occurs in between phase A devices' output source capacitors and $L_a$ as shown in Fig. 4(b). By the end of this interval, $V_{dsA2}$ reaches $V_o$ and $V_{dsA1}$ reaches 0 (as shown in Fig. 3(a)), the body diode of $S_{A1}$ starts conducting and the switch can be turned on at 0 V.

*Interval* V ($T_1$+$t_{d1}$+$T_2$+$t_{d2}$- $T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$)

At the beginning of interval V, $S_{A1}$ is turned on, the equivalent circuit is shown in Fig. 3(d), the phase currents' slopes are given by:

$$di_a / dt = (v_a - V_o / 3) / L \quad (9a)$$

$$di_b / dt = (v_b + 2V_o / 3) / L \quad (9b)$$

$$di_c / dt = (v_c - V_o / 3) / L \quad (9c)$$

This interval ends when $i_a$ reaches zero, $S_{A1}$ is turned off at the end of *Interval* V.

*Interval* VI ($T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$- $T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$)

In this mode, $S_{B2}$ and $S_{C1}$ conduct, the equivalent circuit is shown in Fig. 3(e). The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (V_o + v_b - v_c) / 2L \quad (10)$$

This mode ends when $i_c$ and $i_b$ reach zero.

*Interval* VII ($T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$- $T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$+$T_5$)

After $i_c$ reaches 0, $S_{C1}$ is allowed to conduct for a little more time till $i_c$ reaches a negative value $I_R$ which is enough to discharge the phase C devices' output source capacitors for ZVS turn-on of $S_{C2}$. The equivalent circuit is the same as in Interval VI. At the end of this interval, $S_{C1}$ is turned off.

*Interval* VIII ($T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$+$T_5$- $T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$+$T_5$+$t_{d3}$)

After $S_{C1}$ is turned off, resonance occurs in between phase C devices' output source capacitors and $L_c$ as shown in Fig. 4(c). By the end of this interval, $V_{dsC1}$ reaches $V_o$ and $V_{dsC2}$ reaches 0 (as shown in Fig. 3(a)), the body diode of $S_{C2}$ starts conducting (as $i_c$<0) and the switch can be turned on at 0 V.

*Interval* XI ($T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$+$T_5$+$t_{d3}$- $T_1$+$t_{d1}$+$T_2$+$t_{d2}$+$T_3$+$T_4$+$T_5$+$t_{d3}$+$T_6$)

At the beginning of Interval XI, $S_{C2}$ is turned on (as shown in Fig. 3(a)), the equivalent circuit is shown in Fig. 3(f). The phase currents' slopes are given by:

$$di_b / dt = -di_c / dt = (v_b - v_c) / 2L \quad (11)$$

This interval continues till $i_c$ and $i_b$ reach 0 and a new switching cycle starts once the currents hit zero again. As the switching cycle times depend on phase voltages which vary during line cycle, the switching frequency varies in CRM. Although this variation is very small as is shown below in Fig. 5(b).

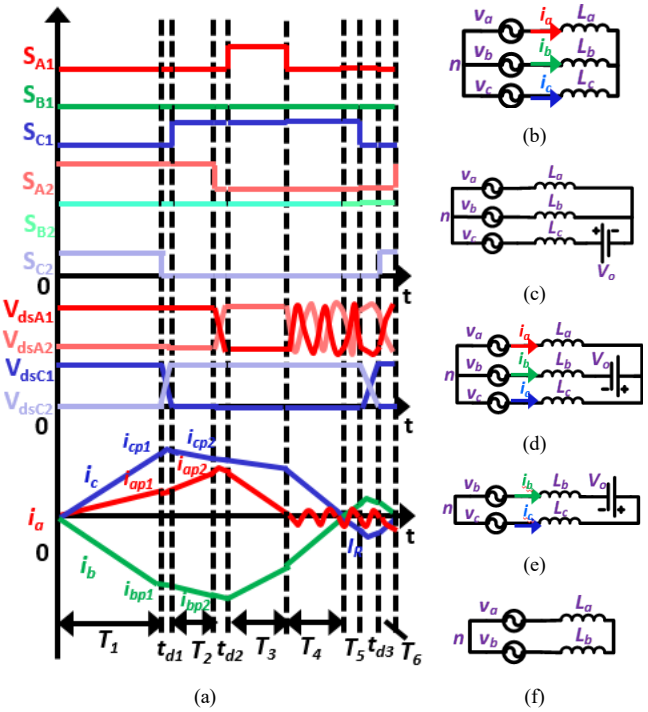
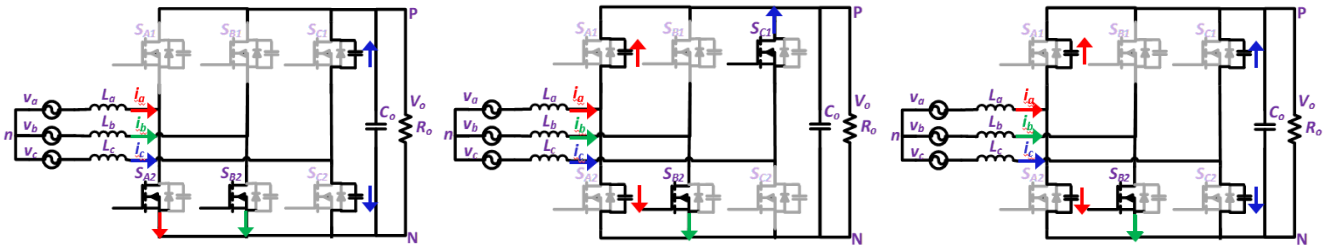



Fig.3 (a) One switching cycle waveform for S.I.C.C. CRM in Sector I (b) Equivalent circuit in Interval I (c) Equivalent circuit in Interval III (d) Equivalent circuit in Interval V (e) Equivalent circuit in Interval VI (f) Equivalent circuit in Interval XI



(a) (b) (c)

Fig. 4 Resonannce between device output source capacitors and inductors during (a) Interval II (b) Interval IV (c) Interval VIII

While calculating the switching times, ideal devices are considered, dead times are neglected for average current calculation as they are very small. The current ripple caused by parasitic capacitors is also neglected for switching times calculation. The effect of capacitors is considered in Section IV. $T_1$, $T_2$, $T_3$, $T_4$, $T_5$ and $T_6$ are derived from the following equations:

$$i_{ap2} + \frac{1}{L}(v_a - V_o/3)T_3 = 0 \quad (12a)$$

$$i_{bp3} + \frac{1}{L}\frac{(V_o + v_b - v_c)}{2}T_4 = 0 \quad (12b)$$

where

$$i_{ap2} = i_{ap1} + \frac{1}{L}(v_a + V_o/3)T_2 \quad (13a)$$

$$i_{ap1} = v_a T_1 / L \quad (13b)$$

$$i_{bp2} = i_{bp1} + \frac{1}{L}(v_b + V_o/3)T_2 \quad (13c)$$

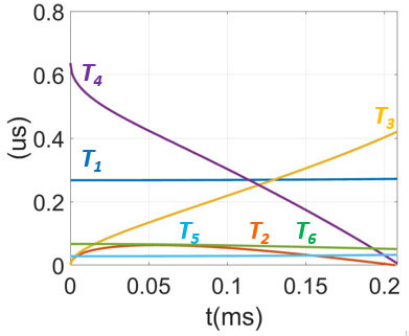
$$i_{bp1} = v_b T_1 / L \quad (13d)$$

$$i_{aavg} = \frac{i_{ap1}\frac{T_1}{2} + (i_{ap1} + i_{ap2})\frac{T_2}{2} + i_{ap2}\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} = k_1 v_a \quad (14a)$$

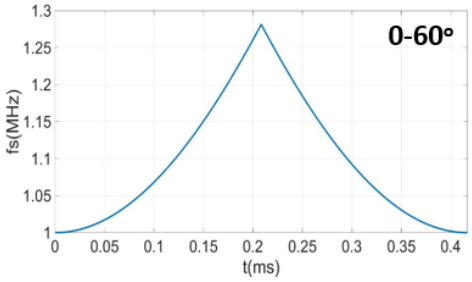
$$i_{bavg} = \frac{i_{bp1}\frac{T_1}{2} + (i_{bp1} + i_{bp2})\frac{T_2}{2} + (i_{bp2} + i_{bp3})\frac{T_3}{2}}{\sum_{i\in 1-6} T_i} \quad (14b)$$

$$+ \frac{i_{bp3}\frac{T_4}{2} - I_R\left(\frac{T_5 + T_6}{2}\right)}{\sum_{i\in 1-6} T_i} = k_1 v_b$$

The switching times are shown in Fig. 5(a) for a 1.2 kW, 400 V $V_o$, 115 $V_{inrms}$, $f_s$~ 1MHz, L= 4 µH. The inductance is chosen to obtain the desired minimum switching frequency. Minimum $I_R$ for ZVS turn-on is calculated as -1 A. The switching frequency variation from 0-60° is shown in Fig. 5(b). The full line cycle control is shown in Fig. 6(a), it can be seen that the operation is symmetric after every 30°. It is to be noted that the phase with highest average and switching current is always clamped thus minimizing the switching losses and the phase with minimum average current is in DCM. Simulated $i_a$ for ideal devices (no $C_{oss}$) is shown in Fig. 6(b), the average current is completely sinusoidal.

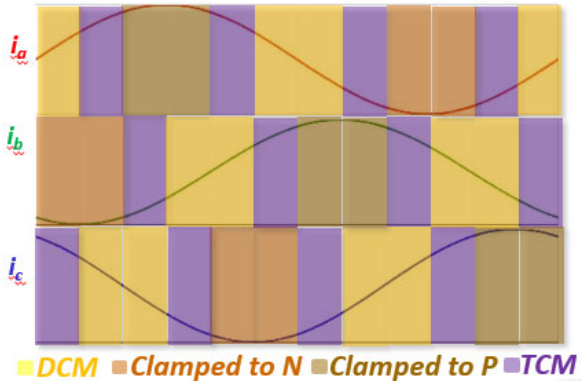



(a)

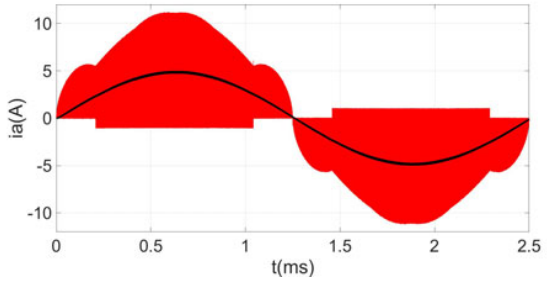



(b)

Fig. 5(a) Switching times and (b) Switching frequnecy variation for 1.2 KW $P_o$, 400 V $V_o$, L~ 4 µH




(a)




(b)

Fig. 6(a) Full line cycle control showing control symetry after every 30°. (b) Simulated $i_a$ waveform with sinusoidal average current

## III. ACTIVE + REACTIVE POWER GENERATION

For a rectifier, u.p.f. operation in TCM is not enough as the system can have reactive power requirements too. Also, for the case of PFC, EMI filter introduces a phase lag between input phase voltages and boost inductor currents which is necessary to be considered in TCM operation.

### A. Theory

As discussed above, in the case of u.p.f., the average phase current can be expressed as directly proportional to the phase voltages. For active +reactive power or purely reactive power generation, the average phase current phasor can be expressed as the vector addiction of two voltage phasors as shown in Fig. 7(b). The average currents are given by:

$$i_a = I_m \sin(\omega t - \phi) = k_1 v_a + k_2 v_b \quad (15a)$$

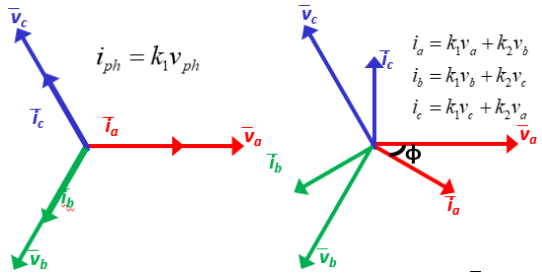
$$i_b = I_m \sin(\omega t - 2\pi/3 - \phi) = k_1 v_b + k_2 v_c \quad (15b)$$

$$i_c = I_m \sin(\omega t + 2\pi/3 - \phi) = k_1 v_c + k_2 v_a \quad (15c)$$

where

$$k_1 = (\cos\phi + \sin\phi/\sqrt{3}) I_m / V_m \quad (16a)$$

$$k_2 = (2\sin\phi/\sqrt{3}) I_m / V_m \quad (16b)$$




(a) (b)

Fig. 7. Average currents (a) directly proportional to phase voltages for unity power factor case (b) expressed as sum of two phase voltages for active + reactive power generation

In this paper, two cases are discussed in detail- 30° & 90° phase lag, it is also shown how one solution can be generalized from -30°-30° and another for phase lags beyond that.

#### 1) 30° Phase Lag

The average currents for 30° phase lag are shown in Fig. 8. It can be seen that the challenge is to generate average currents that are not directly proportional to input voltages thus generating zero average current when the voltage is not zero and vice versa. Also, when there is a phase lag, it is possible that the currents and voltages do not have full circular symmetry as the voltages are symmetric around a different phase angle and the currents are symmetric around a different phase angle. It can be seen in Fig. 8 that for 30° lag, currents and voltages are not symmetric after every 30° but the three phase symmetry still holds after every 60°. Hence, two sectors' operation are discussed in detail for this case.

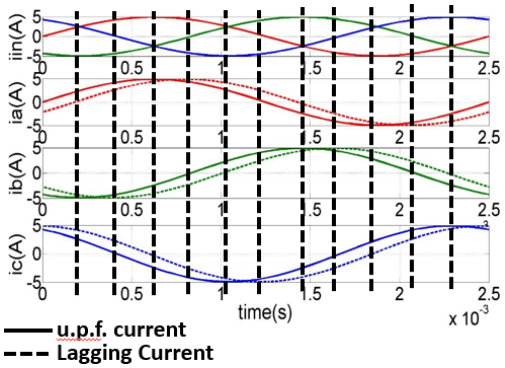



Fig. 8. Average currents for u.p.f. and 30° lagging cases

*a) Sector I (0<ωt<π/6)*

Each switching cycle can be divided into 6 switching intervals (the dead times are not included as operation during dead time is very similar to u.p.f. case) as shown in Fig. 9(a). The gating signals are also included to show the switching sequence. As can be seen in Fig. 8, average phase A current ($i_{aavg}$) is negative, hence $i_a$ ripple should be negative as opposed to u.p.f. case, also A phase (phase in DCM) is only allowed to conduct for two switching intervals as in the end of sector I, average $i_a$ is zero with positive phase voltage, hence times $T_2$ and $T_3$ should be zero at end of sector I as shown in Fig. 10(a). The detailed equations are not discussed for the sake of brevity.

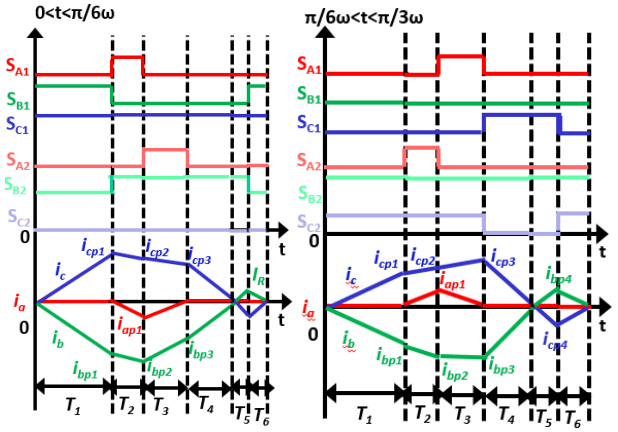
*b) Sector II (π/6<ωt<π/3)*

From Fig. 8, it can be seen that phase currents and voltages are in the same direction now. While the magnitude of phase A average current is minimum, the corresponding phase voltage is much higher posing a challenge for the choice of switching states. The switching waveform for one switching cycle is shown in Fig. 9(b). The solution for the switching times (for sector I & II) for a 1.2 kVA, 400 V $V_o$, 115 $V_{inrms}$, L= 4 μH, 30° phase lag is shown in Fig. 10(a). $I_R$ has to be increased in this case to -3 A as it can be seen from the solutions that $T_1$ approaches zero at the end of sector II, thus a minimum $I_R$ is required to get acceptable switching times' solutions.

This is because the only switching state that leads to a negative slope for $i_a$ in sector II is when $S_{A1}$, $S_{B2}$ & $S_{C2}$ (from Fig. 9(b)) conduct leading to a high increase in ripple in C phase by the time $i_a$ reaches zero, thus making it necessary to compensate for the high gain by giving a higher negative current. The switching frequency variation is shown in Fig.

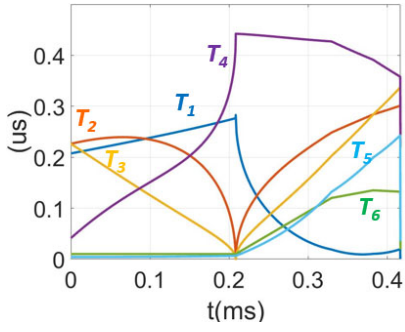
10(b) (which is still a very small variation), it is to be noted that it is not symmetric after every 30° as opposed to u.p.f. case, the reason has been discussed above.

The full line cycle control is shown in Fig. 10(c). It can be seen that the control is symmetric after every 60°, the phase with highest average current and switching current magnitude is still clamped. It is to be noted that as compared to u.p.f. full line cycle control (Fig. 6(a)), the control is just shifted by a phase of -30° in Fig. 10(c). Thus, it can be concluded that the same control can be used for the range of -30°-30° phase shift with equal phase shift applied to the control too. Simulated $i_a$ (for ideal devices) is shown in Fig. 10(d).

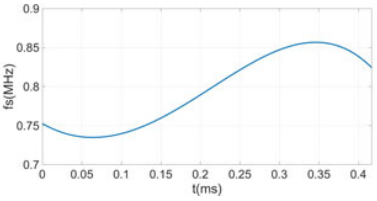



(a) (b)

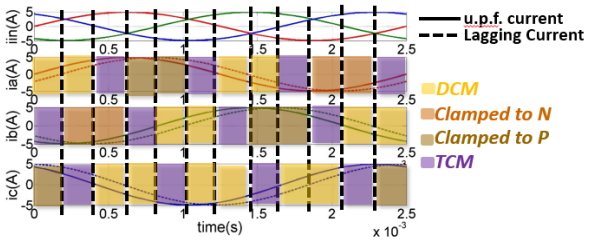
Fig. 9. One switching cycle waveform for 30º phase lag in (a) Sector I (b) Sector II



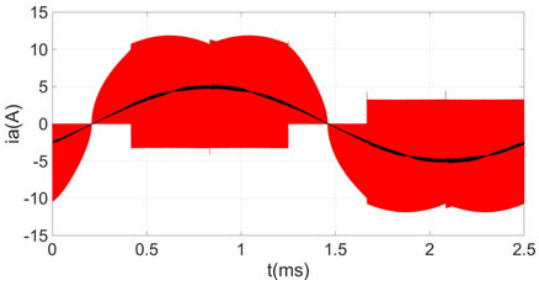

(a)




(b)




(c)



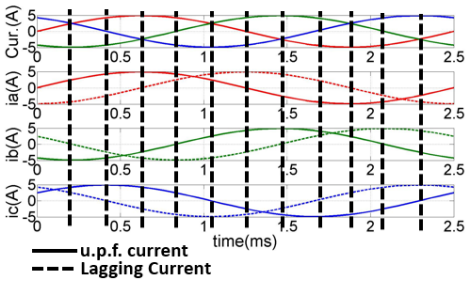

(d)

Fig. 10. 30° phase lag 1.2 kVA, 400 V $V_o$, 115 $V_{inrms}$, L= 4 µH (a) Switching times solution assuming ideal devices for sector I & II (b) Switching frequency variation from 0-60° (c) Full line cycle control showing phase shift of -30° in control (d) Simulated $i_a$ waveform

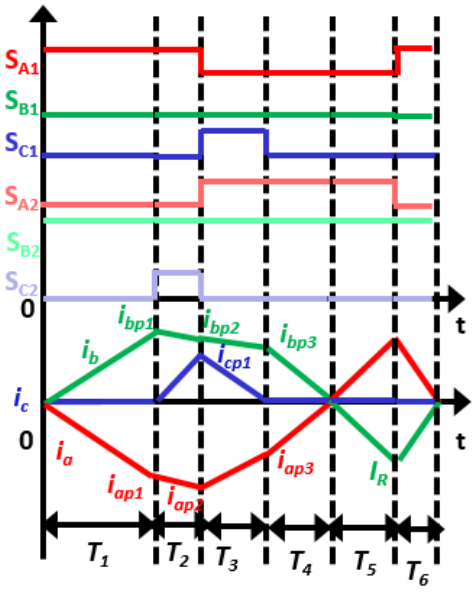
*2) 90° Phase Lag*

The average currents for 90° phase lag are shown in Fig. 11(a). It can be seen that in this case, the phase with maximum voltage has the minimum average phase current requirement. This will start happening beyond 30° phase shift. Hence, now the phase with maximum average current cannot be clamped. It instead operates in TCM with ZVS turn-on. In this paper, only 90° operation is discussed for the sake of brevity. The general solution for all phase shifts will be presented in future publications.

It can be seen in Fig. 11(a) that the case of 90° phase lag has full circular symmetry, thus operation in only one sector is discussed in detail. The switching waveform with gating signals for one switching cycle in sector I is shown in Fig. 11(b). It can be seen (from Fig. 11(a), 11(b) & 13(a)) that the phase with highest average and switching current operates in TCM while the phase with minimum average current but higher switching current is clamped (phase B in sector I), thus still saving on switching losses. The solution for switching times (for sector I & II) for a 1.2 kVA, 400 V $V_o$, 115 $V_{inrms}$, L= 4 µH, 90° phase lag is shown in Fig. 12(a). $I_R$ has to be increased to -9 A to obtain acceptable solutions for the complete range of time. The switching frequency variation is shown in Fig. 12(b). Simulated $i_a$ (for ideal devices) is shown in Fig. 13(b).

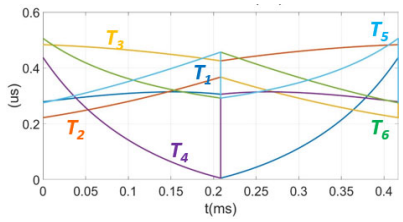



(a)

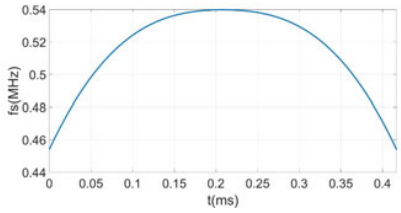



(b)

Fig. 11(a) Average currents for u.p.f. and 90° lagging cases (b) One switching cycle waveform for 90° phase lag in Sector I

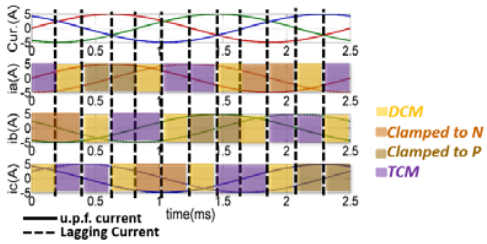



(a)

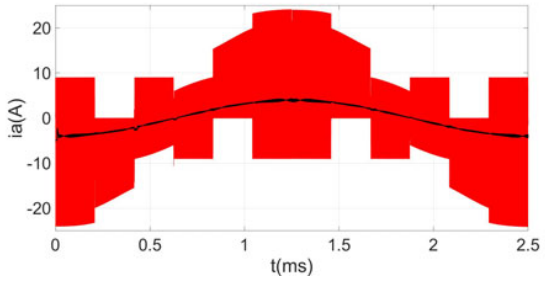



(b)

Fig. 12. 90° phase lag 1.2 kVA, 400 V $V_o$, 115 $V_{inrms}$, L= 4 µH (a) Switching times solution assuming ideal devices for sector I & II (b) Switching frequency variation from 0-60°




(a)




(b)

Fig. 13. 90° phase lag 1.2 kVA, 400 V $V_o$, 115 $V_{inrms}$, L= 4 µH (a) Full line cycle control (d) Simulated $i_a$ waveform

## IV. HARDWARE IMPLEMENTATION

The times shown above are calculated for ideal devices (neglecting the effect of $C_{oss}$ & $L$ resonance ripple on average current). This causes distortion in average current when the above switching times are used with device parasitics. To solve this issue, average current controllers can be used like in [6] and [7]. Here, the average current controller compensates for the current ripple produced by resonance. The controller block diagram is shown in Fig. 14. This block diagram is valid for u.p.f. case from 0-30°, as the line cycle progresses, voltages change and so does the phases operating in DCM and TCM change as discussed above. This is implemented with a microcontroller. The timing state diagram for controller and the corresponding switching states for u.p.f. are shown in Fig. 15. The implementation will be similar for active + reactive power generation also as only the corresponding switching states change when power factor is changed.

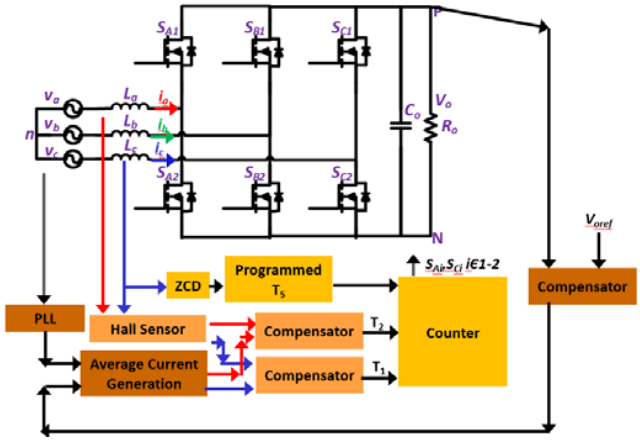
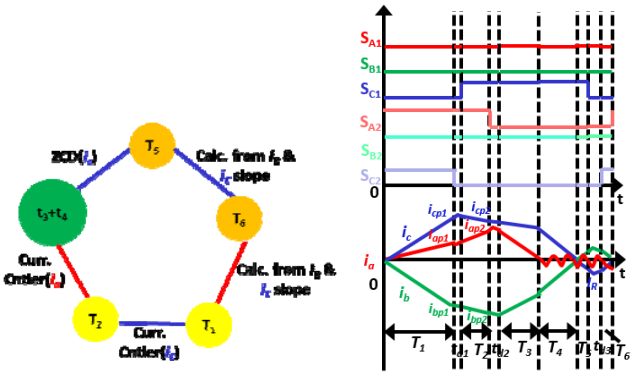


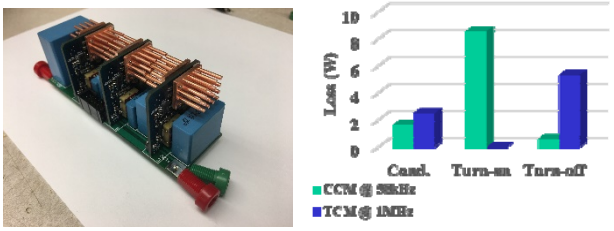

Fig. 14. Digital controller block diagram for average current control from 0-30°




(a) (b)

Fig. 15. (a) Timing state diagram of controller (b) Corresponding states in Sector I for u.p.f.

The above control schemes will be tested on GaN converter shown in Fig. 16(a). With soft switching, the switching frequency can be pushed upto 1 MHz while maintaining ~99% efficiency. The loss breakdown comparison with CCM for u.p.f. case is shown in Fig. 16(b). As compared to state-of the-art Si three phase converters operating in CCM at ~50 kHz, there is a ~2.5 times increase in power density as the filter size is reduced by 60 %. This design achieves the high density of >80 W/in$^3$ while maintaining the same efficiency. Due to limited time, the detailed design and controller implementation will be shown in future publications.




(a) (b)

Fig. 16. (a) GaN converter with ultra low inductance vertical power loop (b) Loss Breakdown Comparison of CCM at 50 kHz and TCM+DCM+Clamped at 1 MHz

## V. Conclusion and Future Work

It can be concluded that conventional soft switching variable frequency CRM for three phase PFC does not generate sinusoidal average inductor currents but it can be modified to achieve sinusoidal currents. The modulation for the same is presented in this paper for three phase 6-switch 2-level converter. It is shown that ZVS turn-on can be achieved in TCM by allowing a very small negative current to discharge the transistor parasitic capacitors. TCM is variable switching frequency control but the switching frequency variation is very small. The modulation is then extended to active + reactive and purely reactive power generation cases. It is shown with correct combination of switching states, ZVS turn-on and sinusoidal average input current can be achieved for any power factor. It is shown that TCM greatly reduces the filter size of the converter by maintaining high efficiency at high switching frequency operation.

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