An Adaptive Selection of Intermediate Bus Voltage to Optimize Efficiency in a Universal Input Three-Phase Power Factor Correction Circuit

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***Abstract*— This paper proposes an adaptive intermediate bus voltage solution to optimize efficiency in a universal three-phase AC input (200 - 480 V) cascaded buck-follows-boost power factor corrected (PFC) converter with a 400 V DC output voltage. With this application and architecture, the output voltage of the boost converter needs to be higher than the peak AC input to maintain PFC and regulation. Thus, at 480 V AC input, taking into consideration allowable overvoltage and margin for regulation, typically a bus voltage near 800 V DC is used between the boost and buck stages. This work proposes to adaptively change the bus voltage between the boost and buck stages based on the value of the AC input in order to maximize efficiency. A loss analysis is included to show the significant loss savings and efficiency improvement using the proposed method. Experimental results are presented for a 5 kW silicon carbide based prototype. The results show up to 4.4 percentage point improvement in efficiency at low AC line input compared to the conventional PFC approach with an 800 V DC intermediate bus voltage. The total loss savings in this case is 220 W, which is 4.4 % of total output power.**

Keywords—universal input three phase PFC; DC bus optimization; three-phase boost-buck; intermediate bus voltage optimization; 400V DC bus; SiC

I. INTRODUCTION

Universal input, three phase input, and 400 V DC output are desirable specifications for kilowatt level power factor corrected (PFC) converters. Universal AC input reduces product development costs by avoiding two or more converter designs for different global AC mains voltages. Three phase input reduces the cost of mains wiring for end users as compared to single-phase operation [1],[2]. Use of a 400 V DC output is common for front-end PFC stages in power supplies and battery chargers, typically followed by an isolated DC-DC converter using 650 V rated silicon devices [3], as illustrated in Fig. 1. Studies have shown that a 400 V DC distribution system is favorable in data center applications and has been adopted for other industrial applications[4],[5]. Accordingly, the focus of this work is on the first block in Fig. 1, i.e. a universal three-phase AC input PFC with 400 V output.

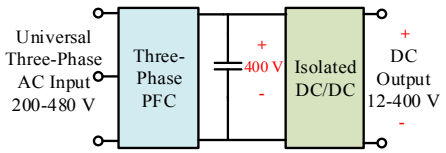

Fig. 1. Block diagram of a typical three-phase kW level PFC rectifier with 400 V DC bus voltage and application-specific nominal DC output voltage typically between 12 V and 400 V

TABLE I. TYPICAL GLOBAL NOMINAL AC VOLTAGES

Geographical Region	Line to Neutral Voltage [V_{LN}]	Line to Line Voltage [V_{LL}]
Japan	100	200
North America	120	208
Asia and Europe	230	400
North America	277	480

A universal input three-phase PFC with 400 V DC output requires a converter topology with step up/down capability to maintain output voltage regulation over the global nominal three-phase input voltage range of 200-480 V [6]. Table I provides a summary of typical line to neutral and line to line voltages by global region.

A three phase six-switch boost converter followed by a synchronous buck is a proven, industry standard topology that can serve as a step up/down converter. This architecture also allows bidirectional operation, making it suitable for applications such as battery chargers with V2G and G2V capability. For high line three-phase AC input, the intermediate bus voltage (i.e. between the boost and buck stages) must be at least 747 V DC (i.e. 480 V_{LL} rms + 10% overvoltage tolerance = 528 V rms = 747 V_{PK}). The conventional solution, as shown in Fig. 2, would fix the bus voltage at near 800 V DC so that the converter has margin for regulation at high line input. However,

a variable bus can help to improve the overall efficiency at lower mains voltages and is the focus of this paper.

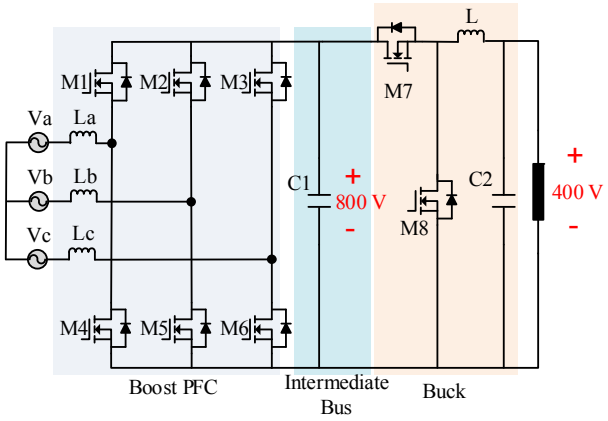

Fig. 2. Conventional three-phase universal AC input cascaded boost followed by buck architecture with fixed 800 V intermediate bus and 400 V DC output

Optimizing efficiency using a variable DC bus has been proposed for a wide range of power conversion applications. Notable works include the following. An optimum DC bus approach for an inverter motor drive application was proposed in [7]. Use of a variable DC bus voltage to optimize efficiency in a high power silicon carbide (SiC) based electric vehicle charger was presented in [8] . The influence of the DC link bus voltage on power losses and thermal characteristics in a bidirectional two-level DC-AC inverter was presented in [9]. A method to optimize efficiency by adjusting the DC bus voltage in a hybrid photovoltaic-grid power system was introduced in [10]. Finally, a variable bus voltage optimal operating point tracking technique for an LLC converter coupled with a universal input SEPIC PFC was presented in [11] and [12].

Coupling the advantages of the two-stage buck follows boost three-phase universal PFC architecture and the variable/adaptive DC bus optimization strategy, this paper proposes a novel strategy to improve and optimize efficiency compared to a conventional 800 V DC intermediate bus benchmark. The proposed adaptive intermediate bus approach is presented in section II. A detailed loss analysis is presented in section III and experimental results are presented in section IV. The conclusions are presented in section V.

II. Proposed Adaptive Intermediate Bus

The minimum intermediate bus voltage between the boost and buck stages in a three-phase cascaded buck-follows-boost front-end must be greater than the peak of the line-to-line input voltage to ensure output voltage regulation and PFC [13], as noted by (1).

$$V_{out\_boost} > \sqrt{2}V_{in_{LL}} \qquad (1)$$

For the universal AC input voltage, with a conventional non-adaptive system, the boost PFC output intermediate bus voltage must be at least 747 V, so it is typically controlled to 800 V so that the converter maintains output regulation and PFC. The proposed adaptive intermediate bus voltage system is illustrated in Fig. 3. The system includes a three-phase boost PFC input stage, followed by a second stage buck converter and a relay. The output of the system is regulated to 400 V. This system uses control to sense the input voltage and then optimizes the boost PFC output voltage to a value less than, or equal to 800 V in order to maximize the system efficiency. The algorithm allows voltage boosting to be minimized, reducing losses in both the boost and the buck converters by reducing losses in the active and passive components. Furthermore, the system includes a relay in order to completely bypass (and disable) the buck converter stage when the AC line is low, such that the optimized boost PFC voltage is regulated to 400 V directly, further improving efficiency for low AC input line conditions.

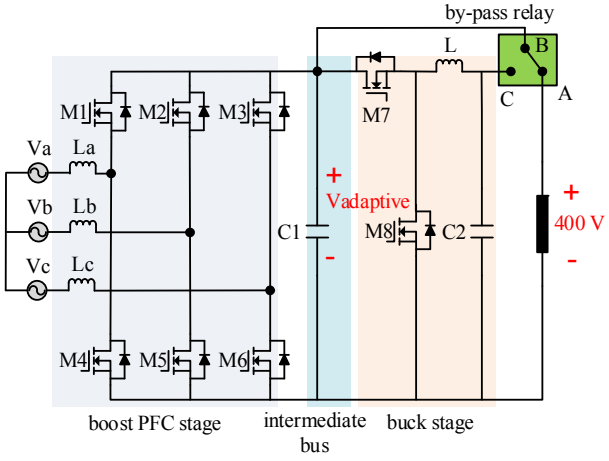

Fig. 3. Proposed three-phase universal AC input cascaded boost followed by buck architecture with adaptive intermediate bus and buck bypass relay

An alternate approach for low AC line voltages (i.e. when the peak voltage is less than 400 V) is to leave the buck stage on with 100% duty cycle. This would save the cost of the relay and its coil driver circuitry, but would incur higher conduction losses in the buck converter's series MOSFET and inductor. By using a bypass relay with a few milliohms of contact resistance, the conduction loss is negligible, resulting in higher efficiency. In this paper our focus is efficiency, so the bypass relay solution is discussed and presented experimentally.

A plot of the allowable boost PFC output voltage as a function of the AC mains voltage is provided in Fig. 4 . With conventional non-adaptive control, the boost stage output voltage is always 800 V as shown by the upper horizontal blue line. However, with adaptive control for varying AC input voltage, the boost PFC stage output should be regulated along the red line. Accordingly, with proper selection of the relay state in Fig. 3 and adaptive selection of intermediate bus voltage, the efficiency of the two-stage converter is optimized using two strategies. For AC input mains voltages with a peak value of less than 400 V, the second stage is by-passed (i.e. state A-B) and the output of the boost converter is set to 400 V DC. On the other hand, if the input voltage peak is above 400 V, the relay is switched to state A-C and the intermediate bus voltage is set equal to the peak of the input.

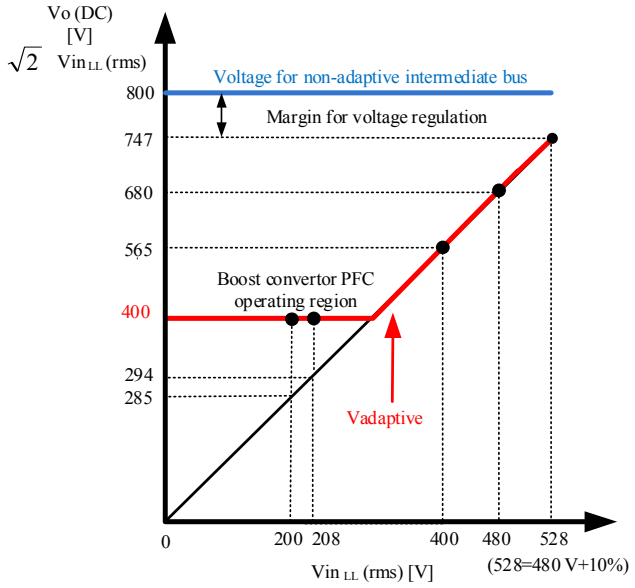

Fig. 4. Allowable boost PFC output voltage as a function of AC mains input voltage for the non-adaptive 800 V PFC bus and adaptive PFC bus

III. Loss Analysis

To show the impact of the proposed adaptive intermediate bus voltage technique, the total loss of the two-stage PFC as a function of intermediate bus voltage, is analyzed in this section. Table II summarizes example specifications and components used in a two-stage 5 kW SiC-based PFC prototype design.

TABLE II. Specifications and Components

Specification/ Component	Value	Quantity
Rated power	5 kW	N/A
Mains line-line voltage (nominal)	200-480 V	N/A
AC line frequency	50-60 Hz	
Switching frequency	50 kHz	N/A
Six-switch boost inductors (La,Lb,Lc)	500 µH / 20 A	3
Buck stage output inductor (L)	500 µH / 20 A	1
Intermediate bus capacitance (Co1)	900 µF	2x150 µF (series sets) x 12 (parallel)
Buck stage output capacitance (Co2)	660 µF	2x330 µF
Boost switches (M1-M6, D1-D6)	CCS020M12CM2	6-pack module
Buck switches (M7, M8)	C2M0080120D	2

The boost PFC stage modulation technique has an impact on the efficiency since the number of switching transitions can vary between different techniques. The boost PFC converter can be driven either by carrier based pulse width modulation (CBPWM) or space vector modulation (SVM). SVM is more popular due to its simplicity [13], and was selected for this work. For the buck stage, voltage mode control with soft-start was used [14].

Active losses (i.e. MOSFET and diode conduction and switching) and passive losses (i.e. inductors and capacitors) comprise the total losses for the set up under test. Numerical methods are used for calculation of losses using component datasheet information. A summary of fixed component loss parameters is provided in Table III. PSIM and Mathcad were used to calculate operating condition values, e.g. rms currents

TABLE III. Loss Calculation Parameter Values

Parameter [unit]	Boost Stage	Buck Stage
R_{DS} [mΩ]	200 (CCS020M12CM2)	43 (C2M0025120D)
R_D [mΩ]	120	107
V_f[V]	0.75	0.766
R_{Gext} [Ω]	Turn on = 10 Turn off = 5	Turn on = 10 Turn off = 5
T_j [°C]	125	125
R_{DC} [Ω]	0.078	0.078
R_{ac} [Ω]	0.148	0.148
ESR [Ω]	0.1	0.29

A. Active Losses

For the converter, the conduction loss in each switch, P_{cond_sw}, can be calculated using (2), and the conduction loss in each diode,P_{cond_D}, can be calculated using (3), where R_{DS} is the drain-source resistance, R_D is the diode dynamic resistance, V_f is the diode forward voltage drop, I_{rms} is the rms switch current, I_{D_rms} is the rms diode current and I_{D_DC} is the average diode current.

$$P_{cond\_sw} = {I_{rms}}^2 R_{DS} \quad (2)$$

$$P_{cond\_D} = {I_{D\_rms}}^2 R_D + V_f I_{D\_DC} \quad (3)$$

The calculations were completed using the datasheet information provided in Table III, at a junction temperature T_j of 125°C.

Switching turn on/off energy information for SiC MOSFETs can be obtained from from data sheets [15]. The switching energy, E is a function of switch current, I_{DS}, drain to source voltage, V_{DS}, gate resistance, R_{Gext} and temperature T_j. For a converter, the value of R_{Gext} is constant. Assuming V_{DS} is known, and T_j is constant for a given operating point and steady state cooling, the switching energy curves from the datasheets can be rescaled to provide values of switching energy at different currents.The rescaled data can then be described by a second order polynomial using curve fitting techniques. The switching energy $E_i(I_{DS})$in every switching cycle can be described by(4), where i denotes switching cycle number in a mains period, and T_{Sw} is the switching period.

$$E_i(I_{DS}) = k_0 + k_1 I_{DS}(iT_{sw}) + k_2 {I^2}_{DS}(iT_{sw}) \quad (4)$$

For an accurate prediction of switching losses, the total

switching loss energy in an AC line period can be calculated each switching cycle using curves of turn-on switching energy, $E_{ion}(I_{DS})$, and turn off switching energy, $E_{ioff}(I_{DS})$. This data is then summed to give the total energy loss, and then is averaged over an AC line period, T, to give the switching power loss in each switch as given by (5). The switch current waveform is determined using PSIM simulation. This data along with (4) and (5) are used to calculate the switching loss for each of the boost and buck stages using Mathcad.

$$P_{sw} = \frac{1}{T}\sum_{i=0}^{\frac{T}{T_{sw}}-1} E_{ion}(I_{DS}(T_{sw}\mathrm{i})) + E_{ioff}(I_{DS}(T_{sw}\mathrm{i})) \qquad (5)$$

Total active losses are then determined by summing the active device switching and conduction losses for the converter, as shown in Fig. 5. As expected, it can be observed that for any given AC line voltage, the total active losses are minimized by minimizing the intermediate bus voltage.

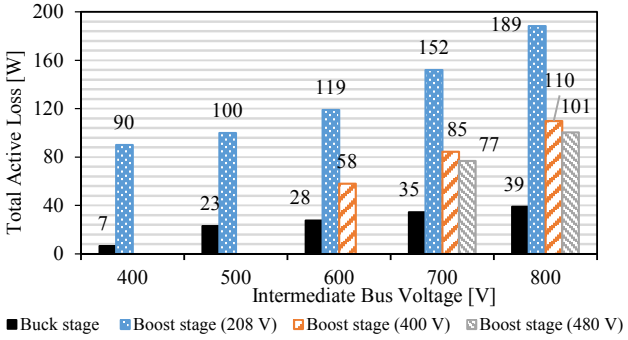

Fig. 5. Active losses as a function of intermediate bus voltage

B. Passive Losses

The passive losses of the converter consist of losses in the inductors and capacitors. The next two sub-sections focus on these components, separately.

1) Inductor Losses

The core loss density, p_L, as a function of flux amplitude and frequency [16] is given by (6), where α, β, γ are constants typically provided in magnetic core material datasheets.

$$p_L = \alpha {B_{pk}}^{\beta} {f_{sw}}^{\gamma} \qquad (6)$$

Flux density is a non-linear function of magnetizing field, i.e. $B = B(H)$ $B = B(H)$. Curve fitting equations are often available in the datasheets as well. For the buck stage, B_{pk} is constant and can be used for core loss calculations. However, for the boost inductors, B_{pk} varies with the line cycle. Therefore, to achieve an accurate core loss calculation, B_{pk} can be calculated each switching cycle, then the results of the instantaneous core loss densities should be averaged over an AC line period to give the effective core loss density. The density multiplied by the core volume, V_c, gives the total effective core loss P_{L_eff}.

$$P_{L\_eff} = V_c \frac{1}{i}\sum_{i=0}^{\frac{T}{Tsw}-1} \alpha \left|{B_{pk}}^{\beta} i T_{sw}\right| {f_{sw}}^{\gamma} \qquad (7)$$

The current waveform consists of high (i.e. switching frequency and harmonics) frequency, I_{high_freq}, and low (i.e. ac line) frequency, I_{low_freq}, components. At high frequencies, the skin effect (ac resistance) needs to be included in the loss analysis [17]. Fast Fourier Transform (FFT) data from simulation is used to calculate the high and low frequency current components. The inductor conduction loss, P_{L_cond}, is given by (8).

$$P_{L\_cond} = {I^2}_{low\_freq} R_{DC} + {I^2}_{high\_freq} R_{ac} \qquad (8)$$

2) Capacitor Loss

The loss in the DC bus capacitors can be calculated using (9) with the equivalent series resistance (ESR), obtained from the capacitance datasheet, and the RMS capacitor current obtained via PSIM simulation.

$$P_{cap} = {I_{rms}}^2 ESR \qquad (9)$$

Using the specifications from Table II, parameter values from Table III, PSIM simulations and Mathcad analysis, the total passive losses (i.e. $P_{L\_eff} + P_{L\_cond} + P_{cap}$) are provided in Fig. 6 as a function of intermediate bus voltage for three AC line conditions, specifically 208 V, 400 V and 480 V. It is clear that passive losses increase with bus voltage. The increase can be attributed to higher ripple current in the boost and buck inductors, which increases the core loss due to higher B_{pk}, and also increased ac resistance copper losses.

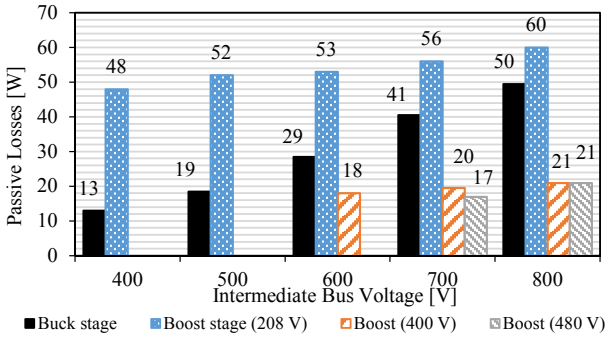

Fig. 6. Passive losses as a function of intermediate bus voltage

C. Total losses

Combining all loss values from sub-sections A and B, the total estimated losses of the two stage PFC as a function of intermediate bus voltage were calculated at 208 V, 400 V and 480 V AC line input, as shown in Fig. 7. It is clear that the minimum loss, and hence highest efficiency, occurs at the minimum bus voltage. However, the bus voltage must also be the minimum value required to allow power factor correction, accordingly low bus voltages, e.g. 400 V cannot be used for high line AC input conditions, e.g. 480 V. The proposed adaptive algorithm measures the three-phase AC input, and sets the intermediate bus voltage to the minimum value in order to

achieve PFC and maximize efficiency.

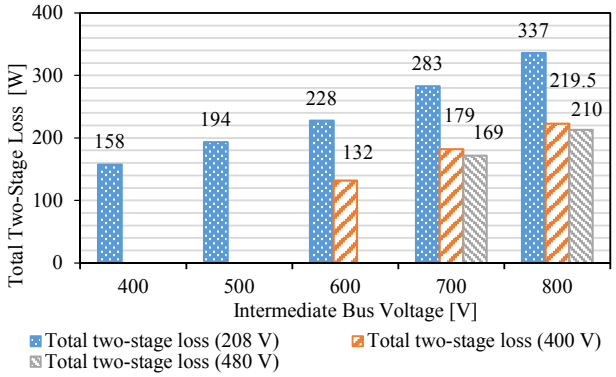

Fig. 7. Total converter loss as a function of intermediate bus voltage

A summary of the estimated total losses for the proposed adaptive and non-adaptive (i.e. 800 V bus) solutions is provided in Table IV. It is noted that for low AC line voltages, e.g. 208 V, since the peak of the voltage is less than 400 V, it is possible to either bypass the buck stage with a relay, or leave the buck stage on with 100% duty cycle. Including a relay potentially increases system cost, but reduces total loss by approximately 20 W (i.e. 199 W – 179.5 W). Finally, the analysis demonstrates a potential loss reduction of 59 % at low AC input line compared to the non-adaptive, 800 V bus solution.

TABLE IV. COMPARISON OF THE ADAPTIVE AND CONVENTIONAL 800 V BUS ARCHITECTURES

Input Voltage [V]	800 V Bus Loss [W]	Adaptive Bus Loss [W]	Loss Reduction [W]	Loss Reduction [%]
208	337	138 (buck stage bypass relay)	199	59
208	337	158 (no buck stage bypass relay)	180	53
400	220	132	88	40
480	210	169	41	20

IV. EXPERIMENTAL RESULTS

A prototype of the universal three-phase AC input cascaded boost and buck PFC system was built using the 1200 V SiC semiconductors and additional specifications and parameter values listed in Table II. The purpose was to validate the proposed adaptive bus method, illustrated in Fig. 3, in comparison to a conventional fixed 800 V intermediate bus, illustrated in Fig. 2. A TMS320F28335 DSP was used for the control. A six channel Cree CGD15FB45P gate driver was used for the boost PFC switches and a Cree CRD8FF1217P driver was used for the buck switches. A photo of the prototype is provided in Fig. 8.

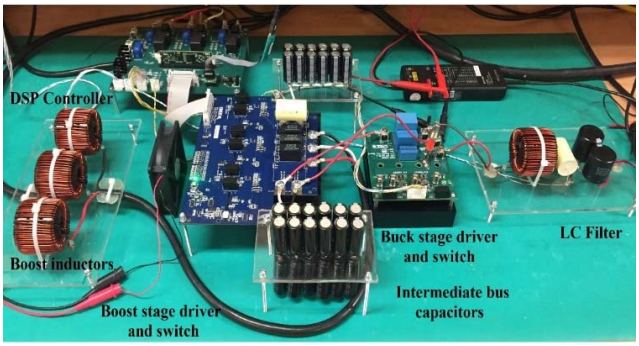

Fig. 8. Photo of the 5 kW SiC-based digitally controlled three-phase cascaded boost-buck PFC prototype

Curves of the total loss of cascaded boost-buck PFC as a function of intermediate bus voltage are provided in Fig. 9 at 208 V, 400 V and 480 V AC (line-to-line) input. Efficiency curves are provided in Fig. 10. Losses are lowest in all cases when the lowest intermediate bus voltage is selected. At 208 V low line input, a 400 V intermediate bus can be used, enabling the losses to be minimized to 160 W with the buck stage at 100% duty cycle, or 140 W with the bypass relay on to eliminate the buck stage conduction losses. This represents up to a 61 % loss reduction or 4.4 percentage point efficiency improvement (97.2 % vs. 92.8 %) compared with the conventional fixed 800 V bus solution, which has 360 W of losses. In addition, it is noted that by selecting the minimum loss points, noted by solid circles, the total converter power loss profile becomes significantly flatter, enabling the converter to operate at full power over the universal input range with potentially not having to overdesign the cooling system.

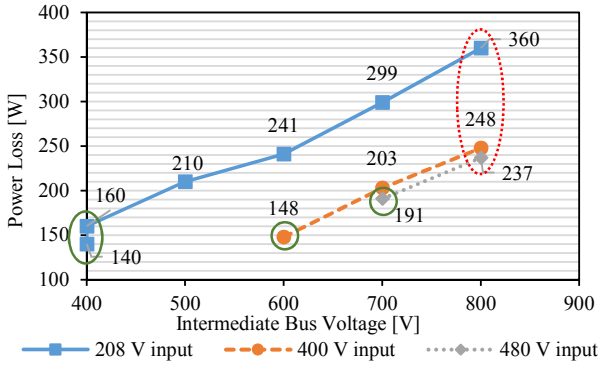

Fig. 9. Total loss as a function of intermediate bus voltage with fixed 800 V bus operating points circled red and adaptive voltage points circled green

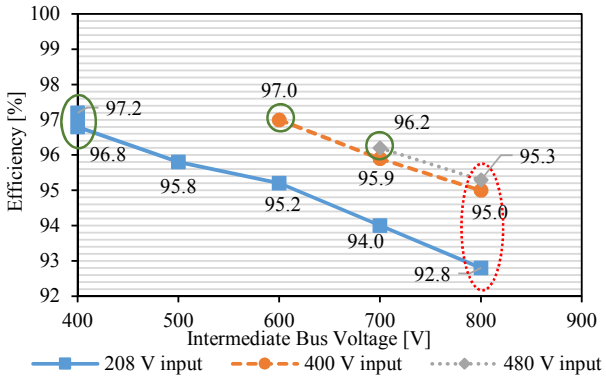

Fig. 10. Efficiency as a function of intermediate bus voltage with fixed 800 V bus operating points circled red and adaptive voltage points circled green

Results comparing the conventional fixed 800 V bus non-adaptive solution and the proposed adaptive bus solution are provided in Table V. The "Percentage Loss Reduction" column clearly illustrates the very significant loss savings in using the proposed adaptive bus solution.

TABLE V. COMPARISON OF MEASURED LOSSES FOR ADAPTIVE AND NON-ADAPTIVE CONTROL AT 5 KW

Input Voltage [V]	800 V Bus Loss [W]	Adaptive Bus Loss [W]	Loss Reduction [W]	Loss Reduction [%]
208	360	140 (buck stage bypass relay)	220	61
208	360	160 (no buck stage bypass relay)	200	56
400	248	148	100	40
480	237	191	46	24

V. CONCLUSIONS

An adaptive intermediate bus voltage control method was presented for a universal AC three-phase input 400 V DC output cascaded buck follows boost PFC. In the proposed method, supervision of the input voltage is used to select the optimal intermediate DC bus voltage before the buck converter, improving efficiency compared to an unsupervised solution using a fixed 800 V DC bus voltage. A loss analysis was performed to illustrate the potential benefit of the proposed method. A 5 kW SiC-based prototype was built and experimental results were presented. It was demonstrated experimentally that the two-stage losses could be reduced by up to 61% (efficiency improvement of 4.4%) at low AC line with the proposed method. Additionally, for the design of a product, the proposed approach would enable simplified thermal design, reducing the size of heatsinks and thus the overall cost.

VI. ACKNOWLEDGMENT

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