Analysis of One Phase Loss Operation of Three-Phase Isolated Buck Matrix-Type Rectifier with a Boost Switch

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***Abstract*— In this paper, the one phase loss operation of the three-phase isolated buck matrix-type rectifier with integrated boost output stage is analyzed. During normal operation (three-phase operation) the boost switch is disabled and during one phase loss is enabled. The analysis of one phase loss with combination of buck and boost (buck+boost) operation shows that the converter is able to deliver two-third of rated power and regulate the output voltage with maximum output voltage drop less than 4% of nominal output voltage with significantly smaller output capacitor comparing with conventional buck matrix-type rectifier. The performance of the converter in buck and buck+boost operation is evaluated and verified by simulations and experiments on a 5 kW prototype.**

***Keywords*— Three-phase, one-phase loss, Buck/Boost, isolated rectifier,**

I. INTRODUCTION

It is shown that buck matrix-type PFC rectifier topologies, as shown in Fig. 1, offer the advantage of performing PFC functionality and galvanic isolation in a single-stage conversion [1-3]. The three-phase buck-type rectifiers provide a wide output-voltage control range down to low voltages while maintaining PFC capability at the input. The three-phase buck matrix-type rectifier design concept is not limited to applications in the 380V DC data centers. It can be also leveraged to other types of applications e.g. electric vehicle (EV) charging stations and on board three-phase EV charger, where the output voltage needs to be changed widely (200 V to 450 V DC) [4]. One possible reason for their limited utilization is the complex modulation scheme required simultaneously to perform PFC and isolated dc-dc conversion over the entire load and input range especially under abnormal grid conditions. In here the example of power supply operation in data center and telecom are chosen because of the stringent requirement of delivering two-third of rated power to the output load and regulating the output voltage during one phase loss operation. This specification requirement can be easily fulfilled with two-stage power supply due to the large intermediate storage energy on the output of first-stage ac-dc converter and second-stage dc-dc converter for isolation and tight output voltage regulation. The significant advantage of two-stage power conversion should be highlighted in here is

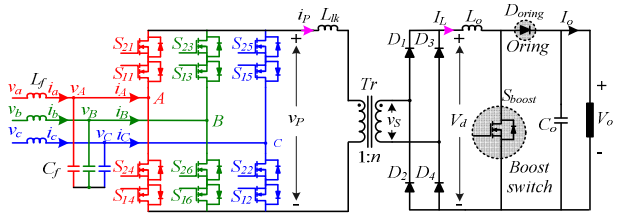

Fig. 1. Three-phase isolated buck matrix-type rectifier with a boost switch.

the capability of delivering two-third of rated power to the load with tight output voltage regulation during fault condition of one phase loss operation [5, 6, 7]. Though, all the functions are realized in the two-stage scheme can be also achieved in a single-stage converter without performance compromise as reported in [8]. However, with the buck matrix-type rectifier it is challenge to satisfy this requirement due to the lack of intermediate storage energy and being buck-type (incapacity to step-up input voltages during main failures such as loss of one phase or short-circuit). In [9], a new PWM scheme and commutation method is proposed for one phase loss operation of the three-phase isolated buck matrix-type rectifier which allows the continuous and safe operation of the converter to deliver two-third of rated power and regulate the output voltage with maximum output voltage drop less than 5% of nominal output voltage. When one phase is lost or shorted with the conventional buck matrix rectifier operation [9], the output voltage V_o drops during the intervals where the output voltage of the bridge rectifier V_d is lower than V_o, since the converter doesn't have any boost capability. As a result, a relatively large value of output capacitance is required to bear the output voltage drop within 5% of nominal output voltage. As shown in Fig. 1, integrating the boost switch in the output stage of the isolated buck matrix rectifier permits the converter to operate in buck+boost mode during intervals of $V_d < V_o$ which results in significantly smaller output voltage drop. Normally, in mission-critical applications, multiple power supplies equipped with oring are connected in parallel to achieve a redundant power supply configuration. In this case, the boost output stage can be realized by adding a boost switch only and efficiency of the power supply during normal operation will not be jeopardized by this added boost stage since the boost switch is deactivated. With the integrated boost output stage, the output capacitors can be substantially reduced if the output voltage drop is kept the same as that of

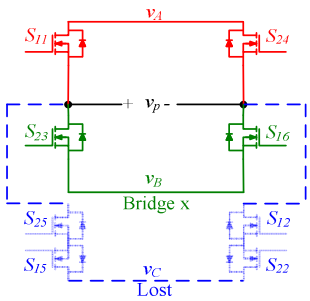

Fig. 2. Three-phase converter redrawn as a ZVS full-bridge dc-dc converters when one phase is lost ("phase *C*") [9].

conventional buck matrix-type rectifier which renders to higher overall power density of the converter and compact size. The main objective of this paper thus lies in the analysis and performance evaluation of the three-phase isolated buck matrix-type rectifier with integrated boost output stage during one phase loss operation. The rest of this paper is organized as follows. Analysis of the one phase loss operation of the converter in pure buck mode and buck+boost is described in Section II. Simulation and experimental results are presented in Section III and IV, followed by the conclusion and future works in Section V.

II. Analysis of The One Phase Loss Operaion of The Converter

For the converter in Fig. 1, there are two operation modes: buck mode and buck+boost mode. During buck mode, the boost output stage is deactivated and the converter operates as a conventional buck matrix-type rectifier. During buck+boost mode, the boost stage is additionally activated and the buck stage is operating at maximum duty cycle. During normal operation the converter switches are operated according to the space vector modulation (SVM) presented in [10]. When "phase *C*" is lost, as shown in Fig. 2, the switches of this phase leg (in dash-line) are not gating and the phase "leg *A*" and "leg *B*" continue operating in the same way as a phase-shift full bridge [11].

A. Analysis of Pure Buck Mode Operation [9]

The detail analysis of this section has been presented in [9]. When the boost switch in Fig. 1 is disabled, the converter operates in the same manner as the conventional buck matrix-type rectifier. The circuit principal waveforms within one gird side cycle with excessively increased switching period of PWM when phase voltage v_c is shorted can be observed in Fig. 3. When the magnitude of v_{AB} becomes low such that the magnitude of V_d is lower than V_o as shown in Fig. 3 (c) the duty cycle of the buck rectifier reaches to maximum and the output voltage V_o starts losing regulation. It is important to be noted that, a large output ripple is generated since the output voltage is only sustained by the output capacitors during the interval of T_{off} where the output voltage V_o loses regulation. The voltage drop ΔV_o is the function of T_{off}, output capacitance C_o, and load current I_o, and can be derived as

$$\Delta V_o = \frac{I_o T_{off}}{C_o} \quad . \tag{1}$$

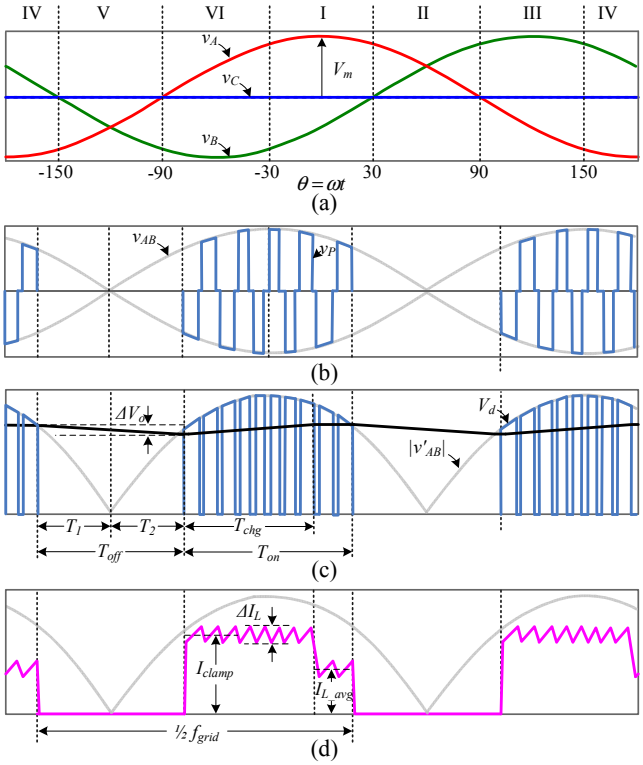

Fig. 3. Three-phase buck matrix rectifier during one phase loss operation [9].

The envelope of V_d is the absolute value of v_{AB} with respect to the secondary side and can be expressed as

$$|v'_{AB}| = n\sqrt{3}V_m \sin(\omega t) \tag{2}$$

where n is the transformer turns ratio.

The output voltage can be expressed as

$$V_o = \frac{3}{2} n V_m m_a \tag{3}$$

where m_a is the modulation index. T_{off} is the distance between the two adjacent crossing points when $|v'_{AB}|$ is lower than V_o. Assuming the duty cycle loss of the buck matrix converter is very small and can be neglected, the location of these two adjacent crossing points where $|v'_{AB}|$ is equal to V_o can be found by equaling (2) and (3).

Then, the T_{off} can be estimated as:

$$T_{off} = \frac{\sin^{-1}(\frac{\sqrt{3}}{2} m_a)}{\pi f_{grid}} \tag{4}$$

where f_{grid} is the grid frequency.

The voltage drop ΔV_o can be derived by substituting T_{off} with (4) into (1):

$$\Delta V_o = \frac{I_o \sin^{-1}(\frac{\sqrt{3}}{2} m_a)}{C_o \pi f_{grid}} \, . \tag{5}$$

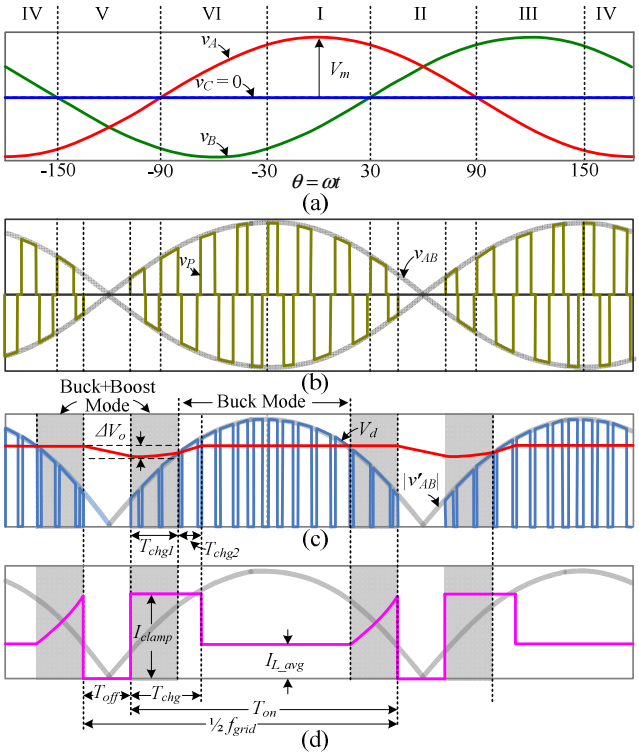

Fig. 4. Three-phase buck matrix rectifier with integrated boost output stage during one phase loss operation, the converter has also two operation modes buck and buck+boost (neglected inductor current ripple).

As shown in (5), the ripple voltage ΔV_o is the function of m_a, output capacitance C_o, and load current I_o. For a given output capacitance C_o, the worst case of the ripple voltage ΔV_o happened at maximum m_a and maximum load (two-third of rated power).

Current stress is another important consideration when converter is operating during one phase lost. The inductor current should be clamped at a maximum allowable value. However, this value should be high enough in order to be able to regulate the output voltage. Since the output capacitor is discharged by I_o during T_{off} and based on the current-second balance of the output capacitor, considering the maximum load current of one phase loss operation at $I_o = 2/3 I_{rated}$, I_{clamp_min} can be described as

$$I_{clamp\_\min} = \frac{\frac{2}{3} I_{rated}}{1 - \frac{2}{\pi} \sin^{-1}(\frac{\sqrt{3}}{2} m_a)}. \quad (6)$$

B. *Analysis Of Buck+Boost Mode Operation (Boost Switch Activated)*

The circuit principal waveforms within one gird side cycle with excessively increased switching period of PWM when the boost switch is enabled during one phase loss operation can be observed in Fig. 4. As shown in Fig. 4, during interval (highlighted) where $|v'_{AB}|$ is lower than V_o, the boost switch is enabled to regulate V_o and the primary of the matrix converter is operating at maximum duty cycle. Therefore, with the boost stage of the converter activated, the interval of T_{off} is greatly reduced compared with the pure buck mode operation in Fig. 3 which results in significantly smaller voltage drop in the output voltage.

However, when $|v'_{AB}|$ is very low, the output voltage V_o starts losing regulation since the output inductor current is clamped at the upper limit by the controller and the duty cycle of boost switch reaches to maximum. As shown in Fig. 4 (d), the output inductor current rises rapidly until it reaches to the maximum value of I_{clamp} when $|v'_{AB}|$ goes down. If $|v'_{AB}|$ further goes down, very limited energy can be delivered to the secondary side due to the small value of $|v'_{AB}|$ and the substantially reduced effective duty cycle of V_d since the duty cycle loss cannot be neglected when $|v'_{AB}|$ becomes very low. Therefore, both the primary switches and the boost switch can stop switching to reduce the losses when $|v'_{AB}|$ is very low. The limit of maximum output inductor current I_{clamp} expressed in (7) can be applied to both buck and buck+boost mode control since the same inductor is involved in both buck and buck+boost mode operation.

$$I_{clamp} = kI_{rated} \quad (7)$$

where k is the over current racial and I_{rated} is the inductor current in nominal condition.

Assuming the duty cycle loss of the buck converter is very small as it is mentioned earlier, the minimum value of $|v'_{AB}|$ required to regulate the output voltage V_o at $I_o = \frac{2}{3} I_{rated}$ (2/3 of nominal power) can be derived as

$$|v'_{AB}|_{\min} = \frac{\frac{2}{3} I_{rated}}{I_{clamp}} V_o \quad (8)$$

By substituting V_o with (3) and I_{clamp} with (7) into (8), we get

$$|v'_{AB}|_{\min} = \frac{1}{\sqrt{3k}} m_a \quad (9)$$

The interval of T_{off} with the boost stage activated can be derived by combining (2) and (9)

$$T_{off} = \frac{\sin^{-1}(\frac{1}{\sqrt{3k}} m_a)}{\pi f_{grid}}. \quad (10)$$

Neglecting the energy delivered from primary to secondary during T_{off}, the voltage drop ΔV_o with the boost stage activated can be derived by substituting T_{off} with (10) into (1)

$$\Delta Vo = \frac{I_o \sin^{-1}(\frac{1}{\sqrt{3k}} m_a)}{\pi f_{grid} C_o}. \quad (11)$$

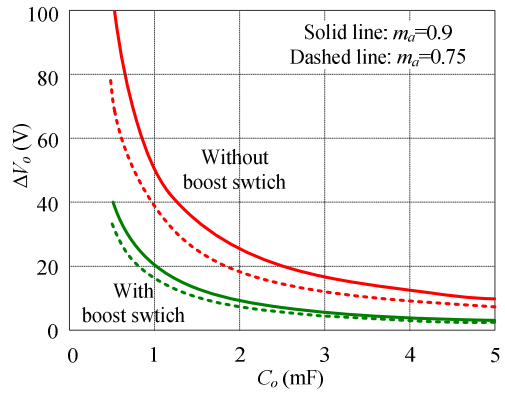

Fig. 5. The output voltage drop ΔV_o versus C_o in one phase loss operation with and without boost switch at $I_o = 2/3 I_{rated}$, f_{grid} = 50 Hz, k = 1.4 with boost switch and k = 1.7 without boost switch.

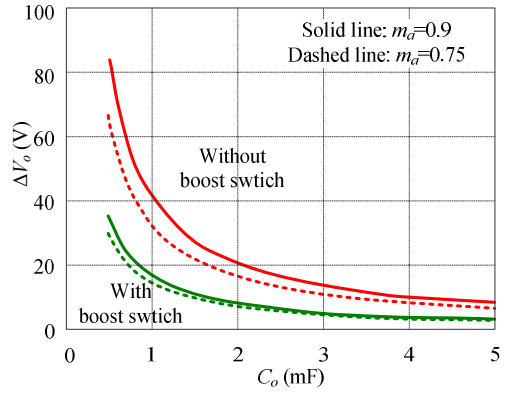

Fig. 6. The output voltage drop ΔV_o versus C_o in one phase loss operation with and without boost switch at f_{grid} = 60 Hz , k = 1.4 with boost switch and k = 1.7 without boost switch.

Fig. 5 and Fig. 6 show the comparison of the voltage drop ΔVo versus C_o at 50 Hz and 60 Hz respectively with and without boost switch operation using equation (5) and (11). Both cases are plotted at the nominal condition v_{LL} = 480 V and v_{LL} = 400 V where m_a = 0.75 and m_a = 0.9 respectively. All the cases are at the same conditions of I_o = 2/3 I_{rated} (k = 1.4 with boost switch and k = 1.7 without boost switch operation). Compared with the conventional buck matrix rectifier (without boost switch), the voltage drop with the boost switch activated is significantly smaller. Alternatively, the output capacitance can be substantially reduced with boost mode operation if the voltage drop is kept the same as that of without boost operation. The m_a and grid frequency also play very important role in determining the voltage drop. Either higher m_a or lower grid frequency will result in higher voltage drop.

Since the boost capability is achieved by only adding a boost switch, the impact on the power density of the converter is very small. In addition, the boost switch is only operating during small interval (highlighted interval) in Fig. 4 (c) and (d) when $|v'_{AB}|$ is lower than V_o. Therefore, the high current through the boost switch won't cause a high thermal stress on the boost switch.

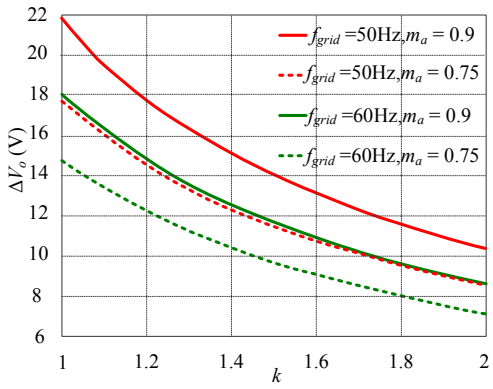

Fig. 7. The output voltage drop ΔV_o versus the over current racial k in one phase loss operation with boost switch at m_a = 0.75 and 0.9 respectively with C_o = 1.4 mF.

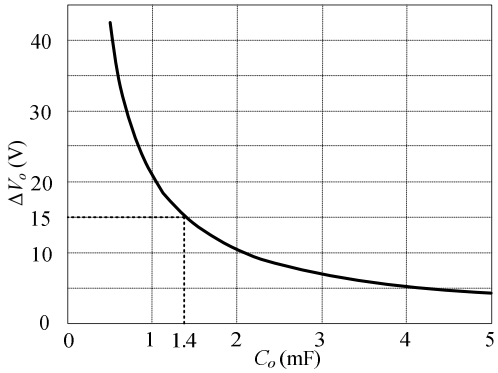

Fig. 8. The output voltage drop ΔV_o versus output capacitance C_o in one phase loss operation with boost switch at m_a = 0.9, k = 1.4 and f_{grid} = 50 Hz.

C. *Design Guidelines with Buck+Boost Mode Operation*

From (11), we can conclude that higher over current racial k (higher I_{clamp}) will result in lower ΔV_o . Fig. 7 shows curve of ΔV_o versus the over current racial k with different m_a and different grid frequency. However, constrains need to be applied to k. The most important constraint for selecting I_{clamp} is the maximum allowable inductor current. The maximum inductor current is designed based on the worst case in normal operation.

It is a popular case that the power supply should be able to deliver full power in the output voltage rang of 270 V - 380 V. In this case the maximum output inductor current should be at least 1.4I_{rated} plus some margin for transient. Then it's safe to set I_{clamp} as 1.4I_{rated}.

The next step is to decide the output capacitance to satisfy the required ripple voltage ΔV_o. Since the worst case for ΔV_o happens at the highest m_a and the lowest grid frequency, case of m_a = 0.9 and f_{grid} = 50 Hz is selected to draw the curve of the voltage drop ΔV_o versus C_o at $I_{clamp} = 1.4 I_{rated}$ as shown in Fig. 8. Finally, capacitance of 1.4 mF is selected as a compromise between the output voltage ripple and power density of the converter. With 1.4 mF output capacitance, the output voltage drop ΔV_o is less than 4% of nominal output voltage during one phase lost operation.

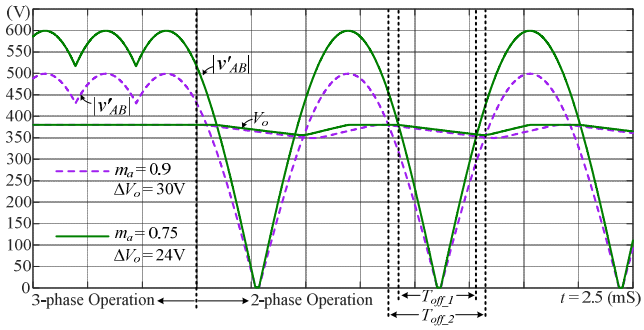

Fig. 9. Comparison of output voltage drop ΔV_o for conventional buck rectifier (without boost switch) at $m_a = 0.75$ and $m_a = 0.9$ with $f_{grid} = 60$ Hz.

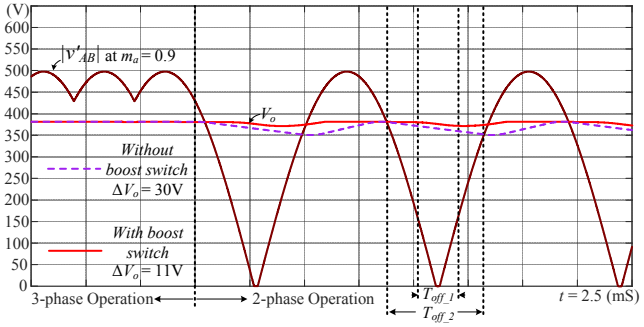

Fig. 10. Comparison of output voltage drop ΔV_o for conventional buck rectifier and buck rectifier with boost switch at $m_a = 0.9$ and $f_{grid} = 60$ Hz.

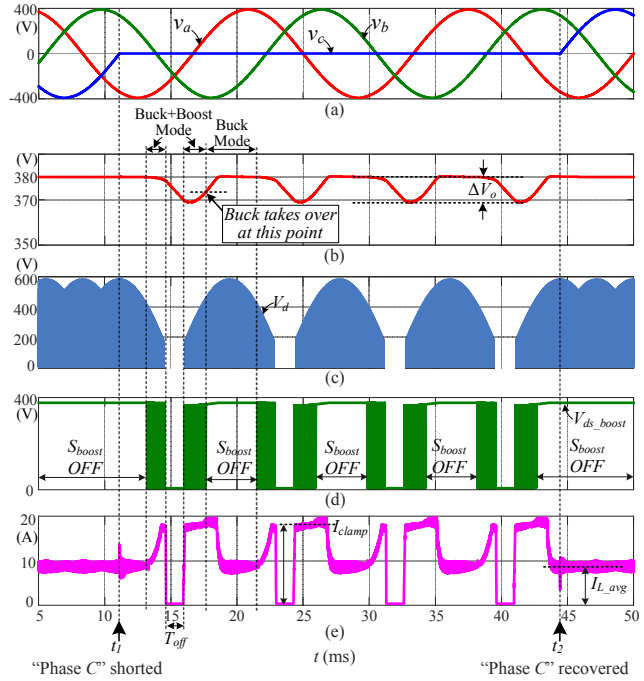

Fig. 11. Simulated waveforms for buck matrix rectifier with boost switch activated: v_{LL} = 480 V (at $m_a = 0.75$), f_{grid} = 60 Hz, k =1.4 and 2/3Po_max when "phase C" is sorted and recovered.

III. Simulation Results

To verify the analysis of one phase loss operation of the converter, a simulation model is built and tested at two-third of rated power. In the simulation, the output voltage drop ΔV_o of the conventional buck converter (without boost switch) under different m_a is studied first and followed by the comparison between operation with and without the boost stage activated. In addition, the key simulation waveforms for the converter with the boost stage activated is provided.

The upper limit of the average output inductor current with buck+boost mode operation, I_{clamp}, is set at 18.5 A (1.4I_{rated}) and the output storage energy C_o = 1.4 mF is selected based on the analysis in section. II. It should be noted that the minimum required I_{clamp} for the operation without boost switch at m_a = 0.9 is 20.4 A based on (6) in section. II. Considering some margin to account for the duty cycle loss, I_{clamp} is set at 22 A (1.7I_{rated}). The minimum required I_{clamp} for the pure buck mode operation (without the boost switch) during one phase loss operation has been discussed in [9]. However, the I_{clamp} given in [9] is chosen based on the nominal condition where m_a is equal to 0.75. If consider the worst case analysis at m_a = 1, then I_{clamp} = 26.3 A (2I_{rated}) should be selected.

A. Discussion of Output Voltage Regulation

Fig. 9 and Fig. 10 show the output voltage, V_o and the absolute value of v_{AB} with respect to the secondary side $|v'_{AB}|$ of the converter during normal operation and one phase loss operation. Fig. 9 shows the comparison of the output voltage drop, ΔV_o at m_a = 0.75 and m_a = 0.9 for conventional buck rectifier (without boost switch). The output voltage drop is larger when the converter operates at higher m_a. This is due to the longer off time at higher m_a during which the output voltage only sustains by the output capacitor. As shown in Fig. 8, T_{off_2} associated with the case of m_a = 0.9 is longer than T_{off_1} associated with the case of m_a = 0.75 which results in relatively larger ΔV_o.

Fig. 10 shows the comparison of the output voltage drop at m_a = 0.9 for conventional buck rectifier (without boost switch) and buck rectifier with boost switch enabled. As it is noticeable from the waveform, the interval of output voltage regulation is longer and the output voltage drop is significantly smaller with boost operation. This is due to the reduced off time intervals of T_{off_1} compared with T_{off_2} of without boost switch operation.

In summary, the maximum output voltage drop ΔV_o and the required current clamping to deliver the output power during one phase loss happen at maximum m_a and minimum grid frequency. Therefore, for the given ΔV_o and output power, the output capacitor and current clamping should be selected at maximum m_a and minimum grid frequency.

B. Key Simulation Waveforms of Buck Matrix Rectifier with Boost Switch Activated

As shown in Fig. 11, at t_1, the "phase C" is shorted and at t_2 is recovered. Boost switch is enabled during one phase lost operation when V_d is lower than V_o. The maximum inductor current is clamped at 18.5 A by the controller during one phase lost operation. At steady state, I_{L_avg} is around 8.77 A to

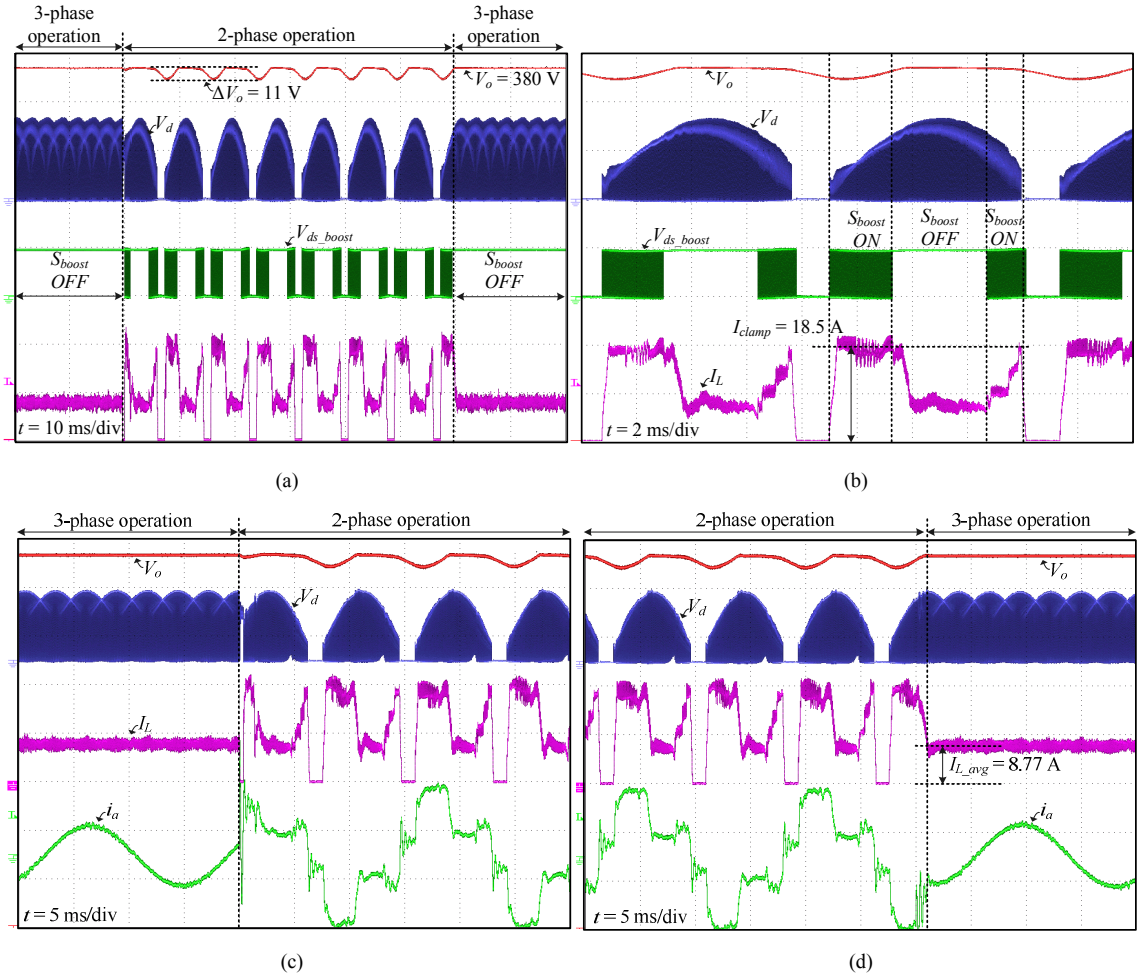

Fig. 12. Experimental waveforms of the converter with a boost switch for 2/3Po_max , v_{LL} = 480 V (at m_a = 0.75), f_{grid} = 60 Hz: (a) voltage waveforms of V_o (50 V/div), V_d (400 V/div), V_{ds_boost} (400 V/div), and I_L (10 A/div) (b) Zoom in waveformes of (a) during 2-phase operation (c) Waveforms from 3-phase operation to 2-phase operation , i_a (10 A/div) (d) Waveforms from 2-phase operation to 3-phase operation.

deliver two-third of rated power. The output voltage drop ΔV_o is around 11 V. Smooth transition between buck+boost mode operation and buck mode operation can be observed from the output inductor current, since both the primary switches of buck matrix rectifier and the boost switch are controlled by the same controller.

IV. Experimental Results

Experimental test is conducted on a 5kW matrix converter. Test condition is: 2/3 rated power, V_{LL} = 480 V, f_{grid} = 60 Hz, m_a = 0.75 and k = 1.4 . Detail experimental system parameters are listed in Table. I.

As shown in Fig. 12(a), the output voltage ripple ΔV_o is 11 V which is well within 4% of nominal output voltage. Waveform of V_{ds_boost} shows that the boost switch is enabled when V_d is lower than V_o. The zoom in waveforms in Fig. 12 (b) shows that the inductor current I_L is clamped at 18.5 A. The current shape is consistent with the analysis in Fig. 4(d) and simulated waveform in Fig. 11(e). Transitions between buck mode and buck+boost mode operation exhibit some disturbance on inductor current due to some limitations on the test setup. The boost switch is implemented by adding a separate modified boost converter to the conventional matrix converter.

TABLE I
Experimental Prototype Parameters

Prototype Parameter	Value
C_f	5μF
L_f	110 μH
$v_{LL,rms}$	400/480 V
f_{grid}	50/60 Hz
C_o	1.4 mF
L_o	315 μH
V_o	380 V
L_{lk}	16.5 μH
S_{11}-S_{26}	SCT3080KL
S_{boost}	IPW60R041P6
D_1-D_4	SCS215KG
2 x D_{oring}	C3D16065A
n	0.86
T_r	Ferrite core (ZP47313TC)
f_{sw}	50 kHz

Therefore, the boost switch and the buck switches are controlled by different controllers. In real application, the boost switch should be designed in a same converter and controlled by the same controller such that smooth transition can be easily achieved.

The current stair case during buck+boost mode operation is caused by the quantization error of the ADC for voltage sensing in boost controller. Higher resolution of the ADC can help to mitigate this problem. During T_{off} interval, both the primary switches and the boost switch stop operating to reduce the losses since V_d is too low to regulate the output voltage.

Grid side current i_a as shown in Fig. 12(c) and (d) is highly distorted due to the large variation of output inductor current in order to regulate the output voltage during 2-phase operation. This is the main drawback of the proposed boost mode operation and remains as a future work to be improved.

It should be noted that the PWM scheme of the isolated buck matrix-type rectifier during 2-phase operation is different from those PWM schemes derived for normal operation and summarized in [10]. A new PWM scheme for 2-phase operation (one phase loss) of isolated buck matrix-type rectifier has been derived and discussed in [9]. A special care needs to be taken for the commutation scheme in order to achieve safe transition between the 3-phase operation and 2-phase operation as it is discussed in [9].

V. Conclusion and Future Works

In this paper, the operation and performance of three phase isolated buck matrix-type rectifier with an additional switch for boosting the output voltage during one phase loss operation is presented. The boost switch is only enabled in one phase loss operation during the intervals in which the output voltage of bridge rectifier is lower than the output voltage and is kept OFF during the normal operation. Therefore, the associated losses and heatsink size of this switch is very small. The three-phase isolated buck matrix-type rectifier with integrated boost output stage exhibits longer intervals of output voltage regulation and smaller output voltage drop for the duration of one phase loss.

In addition, the value of output capacitance can be substantially reduced with buck+boost operation if the output voltage drop is kept the same as that of conventional buck matrix-type rectifier, rendering to high overall power density of the converter.

It is also important to mention that the conventional buck matrix-type rectifier requires significantly larger output inductor current (current clamping) in one phase loss operation comparing with the converter with integrated boost output stage under the same given output power and m_a. Reduced output inductor current clamping can reduce the current stress of the converter during one phase loss operation and the inductor can be designed with smaller size and lower cost.

It should be noted that for simplicity the analysis of converter in this paper is based on the assumption that the duty cycle loss of the buck rectifier is very small and can be neglected during buck mode and buck+boost mode operation. In addition, it is assumed the duty cycle loss is very large if converter operates during T_{off} such that very little power can be delivered from the primary side to the secondary side. These assumptions will affect the accuracy of the analysis. Study of the impact of duty cycle loss on the operation of the converter in buck+boost mode will be considered as one of the future works.

The input currents THD obtained during one phase loss operation is relatively high, which is the main drawback of the proposed control scheme. It may not be acceptable for the system that might even run for days when one phase is lost (2-phase operation). Therefore, how to improve the THD during one phase loss operation is considered as important topic of the future work. In particular, input currents being in phase with the mains voltages have to be guaranteed also in case of mains phase failure such as one phase lost or shorted.

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