Switched Tank Converters

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***Abstract*— This paper presents a new class of Switched Tank Converters (abbreviated as STCs) for high efficiency high density non-isolated DC-DC application where large voltage step down (up) ratios are required. Distinguished from switched capacitor converters, the STCs uniquely employ LC resonant tanks to partially replace the flying capacitors for energy transfer. Full soft charging, soft switching and minimal device voltage stresses are achieved under all operating conditions. The STCs feature very high efficiency, density and robustness against component non-idealities over a wide range. Furthermore, thanks to the full resonant operation, multiple STCs can operate in parallel with inherent droop current sharing, offering the best scalability and control simplicity. These attributes of STC make it a disruptive and robust technology viable for industry's high volume adoption. A novel equivalent DCX building block principle is introduced to simplify the analysis of STC. A 98.92% efficiency STC product evaluation board (4-to-1, 650W) has been developed and demonstrated for the next-gen 48V bus conversion on data center server boards.**

Keywords*— *Switched tank converters, switched capacitor converters, soft charging, soft switching, DCX

I. INTRODUCTION

Recent advancement of semiconductor power devices including both wide-band-gap devices (GaN and SiC) and silicon devices (Trench MOS, LDMOS, etc.) has been pushing power conversion to higher efficiency and density, due to the continuous improvement of the device Figure of Merits (FOM). In the meantime, however, passive components including capacitors and magnetics do not obey Moore's law. Particularly in many modern power electronics applications, magnetic components are becoming bottlenecks in terms of further efficiency and density improvement. For instance, in telecom and data center motherboards where high ratio DC-DC bus conversion is often required, transformer based topologies such as active-clamp forward, full bridge and LLC resonant converters are prevailing regardless of galvanic isolation requirement. Transformer design and integration for these topologies have become the greatest challenge for system optimization as it heavily dictates the overall system efficiency and density. On the other side, the huge customization effort associated with transformers has been hindering some critical business considerations such as scalability, cost, manufacturing risks, and time to market as well [1].

Switched capacitor converters (SCCs) have been widely investigated in both academia and industry for many years, covering a variety of applications from mW level to kW level, from point-of-load PMICs to electrical vehicle power systems [2]-[14]. Instead of using bulky magnetics to achieve voltage step down (up), SCCs primarily rely on switches and capacitors to do the similar job by stacking voltages. The inherent nature of high density and magnetic-less with SCCs becomes compelling from the system design perspective. However, a critical fundamental limit of SCCs is well known as the charge retribution loss mechanism [15]. Whenever a low-impedance switch is closed between two capacitors, the voltage mismatch between capacitors leads to a current inrush and charge redistribution. To minimize the energy loss associated with this charge redistribution, larger capacitors and higher switching frequency are usually required than what they are ideally wanted to be. Hence, either power density or efficiency needs to be sacrificed which offsets the benefit of being magnetic-less.

To address the charge redistribution loss problem of traditional SCCs, many derivative architectures have been proposed and investigated [17]-[21]. The key concept is to introduce some inductive elements into the SCCs such that the charging and discharging of the SCC flying capacitors are essentially lossless. Depending upon the specific topology and PWM control approach, one can achieve soft charging (current-source-like inductive charging) [19], [21], [22] or soft switching (ZVS/ZCS) or both. A merged two-stage SCC-buck architecture incorporating the soft-charging concept was first presented in 2008 [17]. Later on, a start-up company named "Arctic Sand" was founded based on this architectural concept. It offers high efficiency high integration backlight LED drivers and point-of-load voltage regulators for mobile applications. In brief, this merged two-stage architecture elegantly couples the buck inductor to the first SCC stage to softly charge and discharge the flying capacitors. Even though this merged two-stage approach is promising for end-to-end conversion, it is less convenient in applications where independent general-purpose bus converters are more desirable. Another solution to achieve soft charging is to incorporate inductors in the SCC itself. Multiple approaches have been reported in the existing literatures. First, certain number of inductors are aggregated at specific circuit nodes of an SCC topology regardless of the switch and capacitor count [23]-[27]. Each of the inductors can be coupled to multiple flying capacitor networks during each switching state. The inductor current can be either a pure AC or a DC plus some AC ripples, depending upon the specific inductor locations in the circuit. One example of SCC using an aggregated inductor is given in Figure 1a. Second, inductors can be distributed in an SCC topology as well [20], [28], [29]. The inductor count increases along with switch and capacitor count. In certain circumstances, stray inductors can be used. One example of SCC with distributed inductors is shown in Figure 1b. Regardless of

using aggregated inductors or distributed inductors in SCCs, multiple ways of PWM control are available to achieve not only soft charging but also resonant soft switching (ZVS [30]-[33] or ZCS [20], [23]-[26], [28], [29], [34]-[36]).

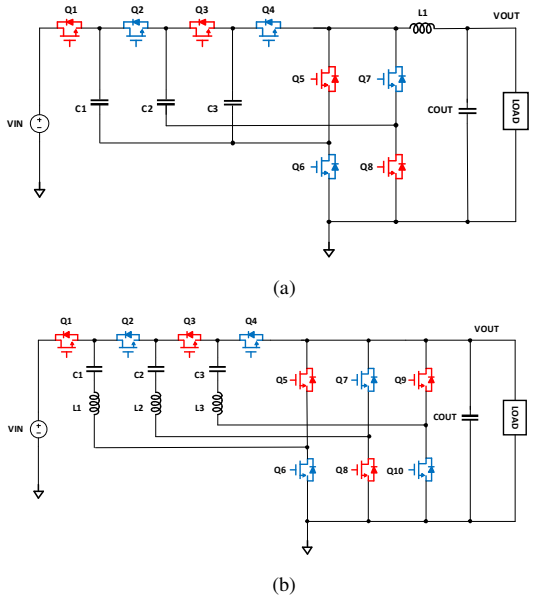


Figure 1. Examples of prior SCC derivative topologies with inductors. (a) 4-to-1 Dickson SCC with one aggregated inductor. (b) 4-to-1 "Multi-level Modular" SCC with distributed inductors.

From the above-mentioned, it seems plenty of SCC derivative solutions are available and ready for the industry to adopt for high volume use. However, in order to make any of these SCC based solutions viable for mass production design, a lot more hidden challenges behind the scene are something that industry can't get around and must be addressed.

Immunity to Component Non-idealities

Most of the above-mentioned topologies are using Class II ceramic capacitors (X7R, X7S, X5R, etc.), which inherently have a very wide tolerance band over temperature (e.g., up to +/-22% for X7S), DC bias (e.g., a 100V Class II MLCC can derate by 70% with 50V bias) and part-to-part variation (> +/-10%). However, these topologies often rely on precisely determined flying capacitors to either satisfy full soft charging requirement [21] or match the switching frequency to LC resonance for soft switching. In addition, the parasitic loop inductances can't be ignored in high current applications. Therefore, the electrical characteristics consistency among different products can hardly be guaranteed once the volume goes high. Undesirable corner cases tend to show up from Monte Carlo or worst case analysis. In some other cases, topologies with distributed inductors, for instance, the one shown in Figure 1(b), create a lot of challenges to designing with low voltage switches. All possible inductor current commutation paths during dead time must be considered with LC tolerances and control timing mismatches. A converter topology whose electrical characteristics vary heavily with component mismatches, large tolerances, or loop parastics is not viable for industry productization.

Capacitor Material Consideration

In most SCC topologies, the electrical characteristics (operation modes, current waveforms, output impedance, losses, etc.) are often associated with flying capacitor values. While Class II ceramic capacitors with large variations are mostly seen in existing literatures, Class I ceramic capacitors are rarely evaluated and used in SCC topologies. Class I ceramic capacitors (C0G, U2J, etc.) use very low dielectric constant and low loss factor dielectric material to offer very stable capacitance, low tolerance (< +/-5%) and low ESRs across all operating conditions. They are ideal capacitor candidates for SCCs that require tight capacitor matching, resonant operation and high current. However, due to the very low dielectric constant and small capacitance, Class I ceramic capacitors usually carry much higher AC voltage ripples than Class II ceramic capacitors in power conversion. It becomes undesirable if switching MOSFETs can see these ripples across drain to source. Therefore, how to appropriately apply Class I ceramic capacitors to SCC based topologies and fully leverage their superior electrical performance remains a challenge.

Worst Case Voltage Stress of MOSFETs

One of the key enablers for high efficiency high density of SCC based topologies is the opportunity to use low voltage rating MOSFETs with better FOMs. For example, in a step-down Dickson and its derivative SCC topologies, all switching devices are only seeing either VOUT or 2*VOUT during normal operation regardless of the high side VIN. However, in order to reliably use low voltage devices, the voltage stress of these devices should never exceed their absolute max rating under all worst case circumstances. The simplest question to ask is whether the drain-to-source voltage of each device can always be clamped to a minimal DC-like voltage by a capacitor or capacitor network in the OFF state even considering loop parasitic inductances, transient events, and worst case component variations. Apparently, the FETs (Q1-Q4) in Figure 1(b) are not desirably clamped and thus can go over stress easily during switching transitions.

Scalability

In high current application, there are two main aspects that must be considered for scalability: 1) the scalability of the topology itself to different conversion ratios and power ratings; 2) the scalability of the control/driver circuitry. For the first part, it's needed to examine how the circuit electrical characteristics change according to different conversion ratios, how easy to accommodate those changes, whether multiple converters can be connected in parallel with good current sharing, and so on. For the second part, it is desirable to have a simple uniform central controller and a scalable driver circuit that supports all topology configurations. In some cases, additional voltage sensing across floating flying capacitors are required to achieve 100% soft charging [27]. This type of complication also affects the scalability of control.

Minimum RMS Current

In applications where conduction losses are often dominant at heavy load, minimizing RMS current of each component becomes critical. In order to achieve this goal, it is ideal to control an SCC based topology with or close to two symmetric

switching states at near 50% duty cycle. And in each switching state, current waveform should be definitive with least influence from parasitic ringings due to component non-idealities. Hence, current can be evenly delivered with minimum RMS. In some resonant SCC topologies using aggregated inductors, the same inductor may resonate with different capacitor banks in different switching states such that asymmetric duty cycle must be used to accommodate multiple resonant frequencies. In these cases, RMS current is not minimized.

Thermal Performance

It is always desirable to have even temperature distribution within the converter without having hot spots. This allows the converter to be capable of delivering maximum power under a given thermal environment. In other words, a good SCC topology needs to have the power stresses distributed among the devices as evenly as possible.

By carefully considering all these practical challenges discussed above, a disruptive new class of Switched Tank Converters (STCs) are proposed in this paper. The key attributes of STCs will be elaborated in the following. A new equivalent DC transformer (DCX) building block principle is introduced to simplify the analysis of STC. One STC topology has been selected for the 48V data center bus converter application. A fully functional 650W 4-to-1 STC product evaluation board has been developed. Experimental performance data will be demonstrated.

II. SWITCHED TANK CONVERTER TOPOLOGIES

In this chapter, the key electrical attributes of the proposed STC topologies are described. Some examples of STC topologies are shown in Figure 2- Figure 5.

A. Key Electrical Attributes of STC

In terms of the current flow direction in the switches, all the switches can be divided into two categories: main switches and synchronous-rectifier (SR) switches. Taking N-Channel MOSFET as an example, a main switch has its current flow from drain to source in normal operations, vice versa, an SR switch normally has its current flow from source to drain. In certain applications, SR switches can be replaced by diodes.

In a step-down STC, all the switches are normally blocking either VOUT or 2*VOUT in their OFF state. Therefore, low voltage devices with superior FOMs can be used to achieve smaller losses, which is the key enabler for both high efficiency and high density. It is often a good practice to design the topology with evenly shared current stresses so that temperature becomes equally distributed, and circuit layout becomes more convenient.

To have the simplest PWM control logic, all the switches can be equally divided into two switch groups. The first switch group share the same PWM control logic (S1), and the second switch group share a 180 deg phase shifted PWM (S2) in respect to the first group with the same duty cycle. It is ideal to control the duty cycle of S1 and S2 near 50% during normal operation such that minimum RMS current can be obtained for each power component.

The flying capacitors in STCs are divided into two categories: resonant capacitors (CR) and DC filtering capacitors (CF). Each resonant capacitor is in series connection with a resonant inductor to essentially form an LC resonant tank. The LC resonant tank can also be potentially replaced by a 2-terminal multi-resonant LC network with the combination of multiple L and C, which is not in the scope of this paper. Multiple (>=2) LC tanks that share the same resonant frequency are incorporated in an STC to partially replace the original DC flying capacitors in SCCs. Therefore, instead of switching and transferring energy between flying capacitors like traditional SCCs, in an STC, the energy is always being transferred between one LC tank and another LC tank or a DC filtering capacitor during switching. This unique characteristic defines the topology name “Switched Tank Converters.”

High performance Class-I (e.g., C0G, U2J) MLCC capacitors can be used as resonant capacitors in an STC. Their tight tolerance (+/-5%) and low ESR (dissipation factor <0.1%) over a wide voltage and temperature range are perfectly suitable for resonant operation. Class-II (e.g., X7R, X6S, etc.) MLCC capacitors that offer much higher capacitance than Class-I capacitors are used as DC filtering capacitors, which serve for the DC filtering function. Because a DC filtering capacitor works almost like a DC voltage source with very minimal AC ripples, it has negligible impact to the resonant operation of STC. This makes the STC operation very insensitive to the large tolerances of the Class-II MLCC capacitors. In some topology configurations, a DC filtering capacitor can be significantly reduced if its ripple current is cancelled out and negligible.

Benefiting from the resonant operation of the LC tanks, all the switches in an STC can be controlled to turn on and off upon current reaching zero. This zero current switching (ZCS) feature allows an STC to be almost free of switching losses, particularly in low voltage applications where MOSFET Coss charge losses are much less significant. Hence, an STC can inherently achieve very high efficiency. As the resonant capacitors are Class-I ceramics with +/-5% tolerance, using matched resonant inductors to get a uniform resonant frequency within all the LC tanks becomes viable. Simple zero current detection (ZCD) techniques can be applied as well to adaptively control the ON time for each resonant tank such that the LC resonant frequency and the ZCS operation is always in track. For example, in Figure 2-Figure 5, S1 and S2 can be further divided into sub groups of S1A, S1B, S2A, S2B, etc.

One of the most critical features of an STC is that every individual current conduction sub-circuit loop sees at least one LC resonant tank with inductive impedance at high frequency. Therefore, every flying capacitor is always being softly charged and discharged during operation. This key characteristic fundamentally eliminates inrush current or charge redistribution losses associated with traditional SCCs. Compared to the previously mentioned topologies that incorporate aggregated inductors for soft charging, the soft charging of STC is 100% guaranteed regardless of flying capacitor matchings and tolerances.

In order to reliably leverage the superior FOMs of low voltage rating MOSFETs, all switch drain-to-source voltages must be always clamped to desired DC levels by DC capacitors

or capacitor networks. The DC filtering flying capacitors in STC naturally serve for this purpose. Even though multiple inductors are employed in an STC, none of the switches will see them in series at the OFF state. Instead, at any switching state, all the OFF switches are always clamped at either VOUT or 2*VOUT by the DC flying capacitors and input/output capacitors. This ensures the reliable use of low voltage rating devices with minimal voltage stresses.

Enabled by the definitive output impedance, same STCs can be connected in parallel to operate in multi-phase or multi-cell manners. The PWM clocks among paralleled phases or cells can be synchronized with or without phase interleaving, or even non-synchronized. Inherent droop current balancing among phases or cells is achieved by using the same MOSFETs and LC tanks. This feature provides a great scalability of STCs to higher current and higher power.

From the previously discussed, Table I here summarizes the comparisons of the most critical attributes of STCs and existing SCC topologies.

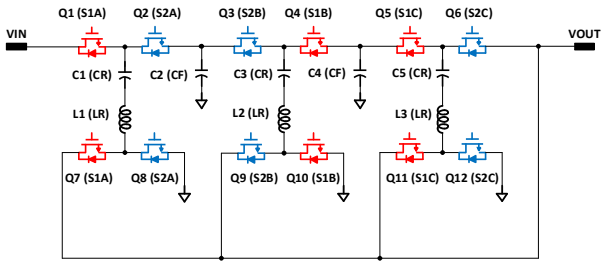


Figure 2. 4-to-1 STC (1-phase, all switches clamped by VOUT).

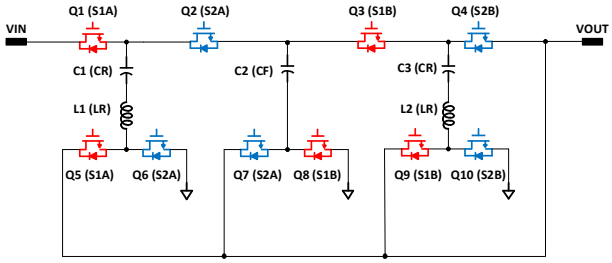


Figure 3. 4-to-1 STC (1-phase, all switches clamped by VOUT and 2*VOUT).

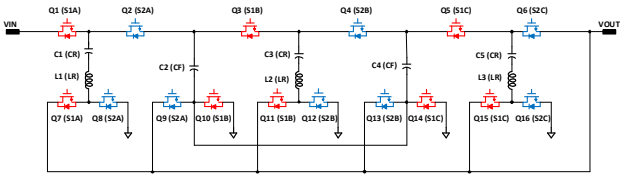


Figure 4. 6-to-1 STC (1-phase, all switches clamped by VOUT and 2*VOUT).

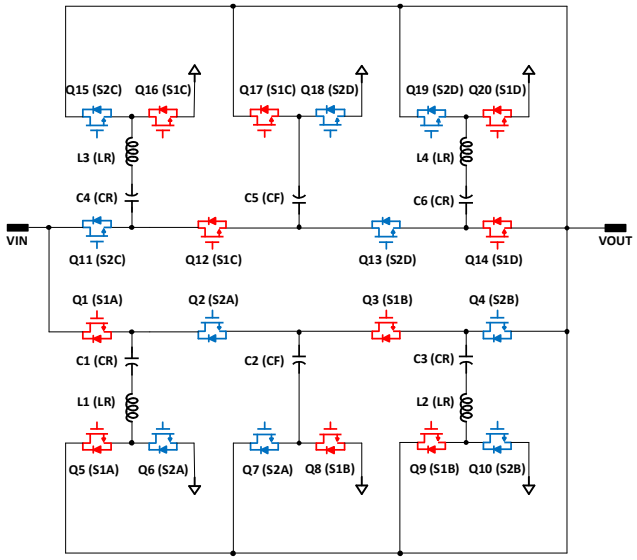


Figure 5. 4-to-1 STC (2-phase, all switches clamped by VOUT and 2*VOUT).

TABLE I. KEY ATTRIBUTES COMPARISONS OF TOPOLOGIES

	Conventional SCCs	**SCCs with aggregated inductors**	**SCCs with full distributed inductors**	**STCs**
Soft charging	No	Partial	Full	Full
Soft switching capability	No	Yes	Yes	Yes
Immunity to component non-idealities	Poor	Medium	Very poor	Good
Device voltage clamp	Clamped, low stress	Case by case	No clamp, very high stress	Clamped, low stress
Scalability	Poor	Medium	Very good	Very good

B. STC Topology Examples

Figure 2 shows a 1-phase 4-to-1 STC with all switches clamped by VOUT. Q1-Q6 are the main switches, Q7-Q12 are the SR switches. L1-C1, L2-C3, and L3-C5 constitute the three LC resonant tanks. C2 and C4 are the DC filtering flying capacitors with much lower voltage ripples (cancelled out) than the resonant capacitors C1, C3 and C5. In this topology, the flying capacitors are biased by different DC voltages (VOUT, 2*VOUT, and 3*VOUT) during normal operation. Normally, identical PWM logic S1 (S2) can be applied to S1A (S2A), S1B (S2B) and S1C (S2C) if LC tanks are well matched.

A 1-phase 4-to-1 STC with all switches clamped by VOUT and 2*VOUT is shown in Figure 3. In this topology, Q2-Q3 and Q4-Q5 in Figure 2 are merged to a single switch with double voltage rating, respectively. DC filtering capacitors and

resonant tanks are re-arranged. Figure 4 shows a 1-phase 6-to-1 STC which is scaled up from Figure 3. C2 and C4 are connected together at one side here to provide a shortest clamping loop for Q3 and Q4. In Figure 3 and Figure 4, Class II ceramic capacitors are selected for CF with much higher capacitance than the Class I resonant capacitor CR. This allows the resonant frequency to be determined pretty much only by LR and CR with very tight tolerance. Because of the better utilization of switches and LC tanks in the topology of Figure 3 and Figure 4, this topology becomes very compelling particularly in low voltage (e.g., 48V) high current applications. The conversion ratio of this topology can be conveniently scaled up and down to even integers.

As discussed earlier, STCs can support parallel operation for higher power by using multi-phase or multi-cell configurations. Figure 5 shows the 2-phase 4-to-1 STC topology derived from Figure 3. 180 deg phase interleaving allows to minimize input current ripple and decoupling capacitors.

III. EQUIVALENT DCX BUILDING BLOCK PRINCIPLE

In this chapter, a new equivalent DCX building block principle is introduced to make the circuit analysis of STC very simple and intuitive.

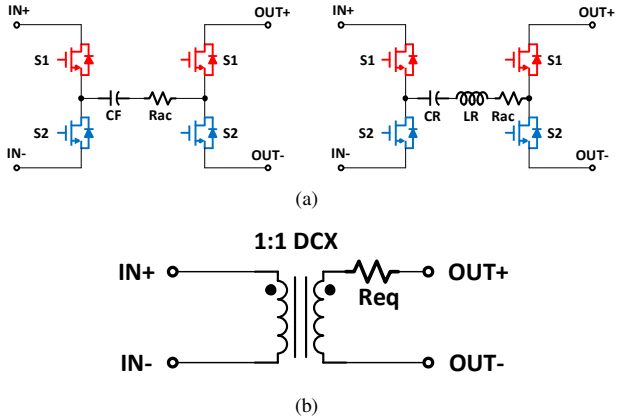


Figure 6. (a) Two fundamental building blocks of an STC topology. (b) Equivalent DCX building block for (a).

An STC topology (illustrated in Figure 2-Figure 5) is constructed based on one or two of the fundamental building blocks shown in Figure 6a. The one on the left of Figure 6a always pairs with the one on the right to essentially form a resonant operation. Each of these two STC building blocks can be modeled as a 1:1 DCX building block, as shown in Figure 6b. In Figure 6a, either the DC filtering capacitor CF or the resonant capacitor CR can block the common-mode voltage difference between input and output. Rac is the lumped resistance in the resonant AC link, which includes MOSFET Rds_on, PCB trace resistance, capacitor and inductor ESRs, etc. Obviously, neither of these two building blocks can work alone. They both need an additional common mode current path between input and output in order to function correctly. For example, IN- can be tied to a DC source while OUT- is tied to reference ground.

The typical waveforms of S1, S2 switching logic, switch current and resonant inductor current are illustrated in Figure 7. ZCS ON and OFF can be achieved if the ON time is matched to a half of the resonant period.

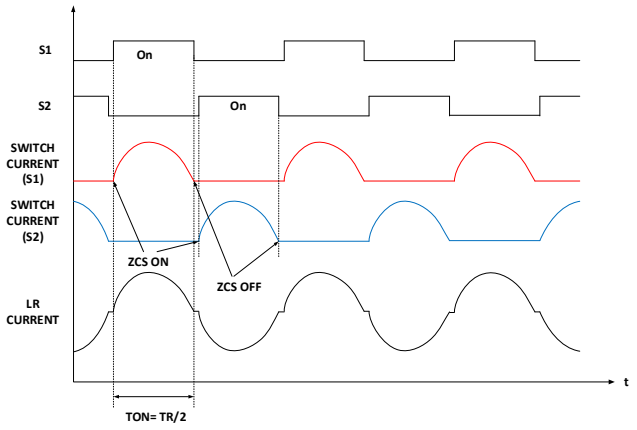


Figure 7. Typical waveforms of the two STC building blocks in Figure 6a.

Due to the resonant operation, the equivalent resistance seen at the DCX block output can be expressed by (1). TR is the LC resonant period, Tsw is the switching period, and (Tsw-TR) is the dead time. Normally, Tsw is very close to TR.

$$R_{eq} = \frac{\pi^2 T_{sw}}{2T_R} R_{ac} \quad (1)$$

Taking the STC topology in Figure 3 as an example, Q2 and Q3 can each be split to two switches as shown in Figure 8. Therefore, the 4-to-1 STC topology can be modeled by a matrix configuration of 3 DCX building blocks. Here, the DCX input terminals are connected in series and the outputs are connected in parallel. Each DCX block processes ¼ of the total power. The IN- terminal of the 3rd DCX block is connected to VOUT such that the last ¼ power is simply bypassed to the output. Likewise, the other STC topologies can be modeled by the matrix DCX equivalent circuit in the same manner.

By extending the matrix DCX model in Figure 8 to N-to-1 conversion, the STC output resistance can be derived as (2). Assuming Tsw is sufficiently close to TR, Rout is then only determined by Rac of each STC building block. Eq.(2) indicates that multiple STCs can operate in parallel with inherent droop current balancing. The Rac mismatch between STCs is reasonably small such that good current balancing accuracy can be achieved (e.g., 10%).

$$R_{out} = \frac{1}{N^2}\sum_{i=1}^{N-1} R_{eq(i)} = \frac{\pi^2 T_{sw}}{2N^2}\sum_{i=1}^{N-1} \frac{1}{T_{R(i)}} R_{ac(i)} \quad (2)$$

Applying the same principle based on the matrix DCX circuit model, many other interesting circuits can be derived potentially. For example, by reconnecting the IN- terminal of the 3rd DCX block in Figure 8 to a 4-switch buck-boost regulator's input and connecting this buck-boost output in parallel with the STC output, a high efficiency partial power STC-buck-boost topology with voltage regulation capability can be obtained. The DCX building block principle can be used as a simple and effective analytical tool as well to model many other SCC based topologies. Further investigation will be discussed in other papers.

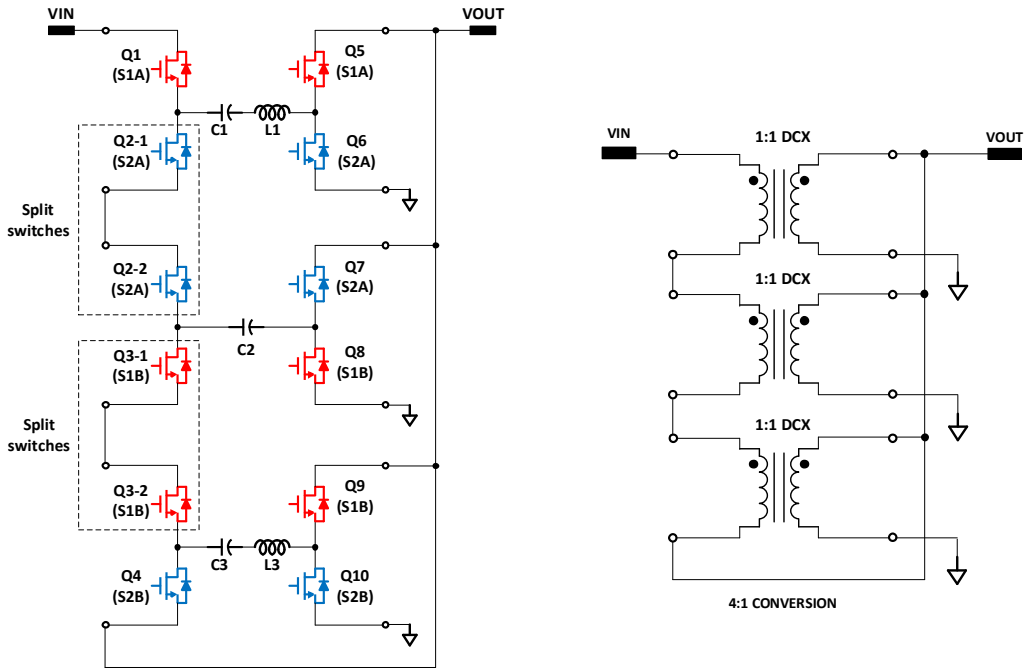


Figure 8. STC topology modeled by a matrix configuration of DCX building blocks.

IV. STC Application in Data Center

Benefiting from all the unique electrical characteristics discussed above, the proposed STC topologies can extraordinarily address the SCC technical challenges described in Chapter I. This makes the adoption of STCs for industry's mass production design much easier. The proposed STCs are widely applicable to high ratio DC-DC bus conversions where galvanic isolation is not a requirement. 48V data center power system is one of the emerging applications that can very well leverage the advantages of STC.

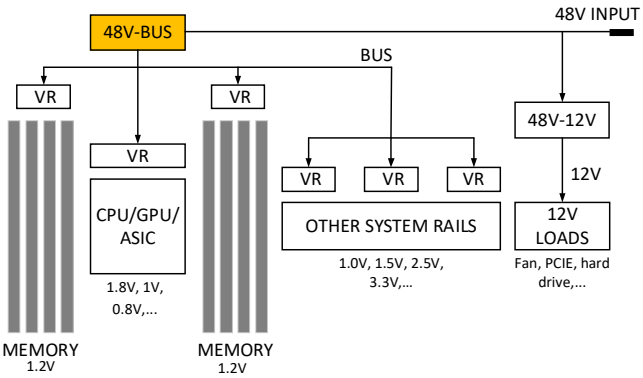


Figure 9. Proposed power system architecture for 48V data center server board.

Figure 9 shows the proposed power system architecture for a typical 48V server board in data center. A two-stage conversion approach is adopted here for the micro-processor (CPU, GPU, ASIC, etc.) core rails, memory rails and other system house-keeping rails. The first stage bus converter uses an STC to step down the input 48V bus to an intermediate bus. Single-phase or multi-phase buck regulators are used for the second stage point-of-load power conversions. The intermediate bus voltage can be optimally selected to achieve the best overall performance in terms of efficiency, density and cost.

Figure 10 shows a 4-to-1 STC bus converter architecture implemented with the control and driving system. A simple and scalable charge pump circuit is designed to generate bias power for each gate driver. A front-end buck converter is incorporated for STC start-up and protections. Upon startup, the STC controller generates PWM signals first to the STC power train and then enables the buck converter to ramp up. At steady state, the buck converter operates with 100% duty cycle to offer a > 99.9% efficiency. Meanwhile, the buck inductor serves as the input filter for STC. When the STC controller detects a fault event, it immediately shuts down the buck converter such that every voltage in the downstream of the buck can be safely discharged. Detailed circuit design and operations are not in the scope of this paper.

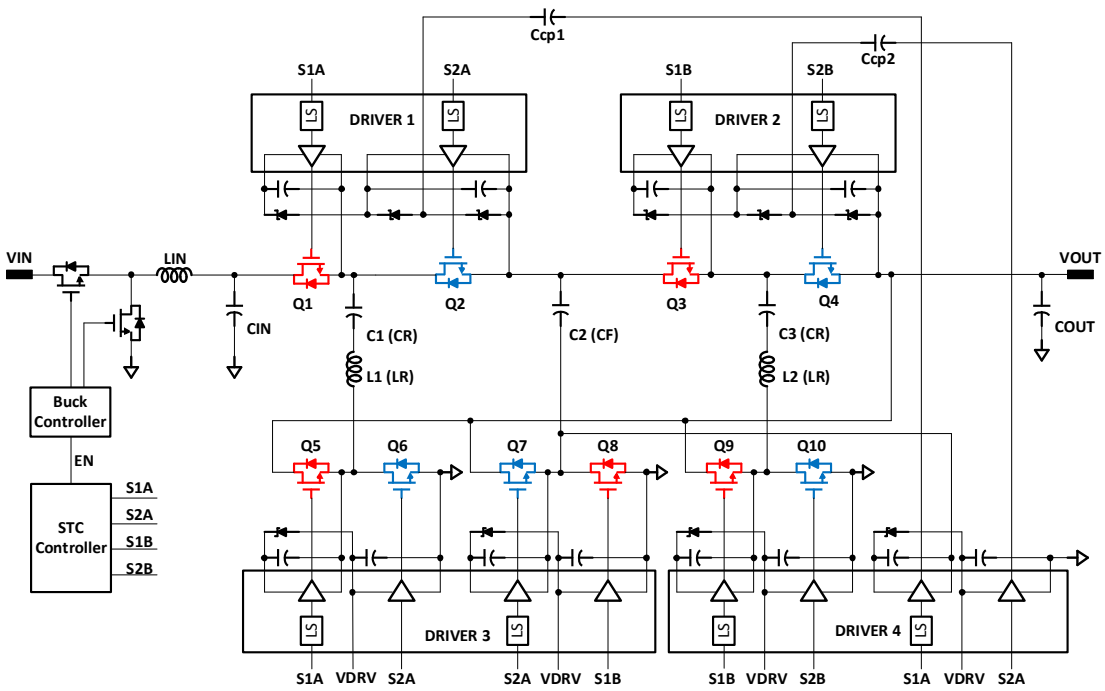


Figure 10. 4-to-1 STC architecture with the control and driving system.

V. Experimental Results

A 650W 4-to-1 STC product evaluation board shown in Figure 11 has been designed for the data center 48V bus conversion. The key parameters and components are listed in Table II. To avoid confusion, the 48V bus specifications here are based on Google data center power rack. As seen in Figure 11, even though components are loosely populated to meet Google's data center DFM requirements, a very high power density of 500W/inch^2 is still achieved for the STC power train. The driver and control circuitries can be potentially integrated by semiconductor manufacturers to offer an overall compact solution.

TABLE II. Key Parameters and Components of the STC Design

VIN	40V-60V, 54V nominal
VOUT	9.5V-15V, 13.5V nominal
IOUT	50A
C1, C3	3.8uF (0.47uF, 50V, U2J, +/-5%, 8pcs, Kemet)
L1, L2	58nH (PA5013, +/-4nH, Pulse)
C2	60uF (10uF, 100V, X7S, 12pcs, Murata)
Q1-Q4	BSZ025N04LS (40V, 2.5mOhm)
Q5-Q10	BSZ013NE2LS5I (25V, 1.3mOhm)
Switching frequency	320kHz
STC controller	STNRG328A (STMicro)
Gate driver	STRG04 (STMicro)
Buck controller	LTC7801 (Linear Tech)

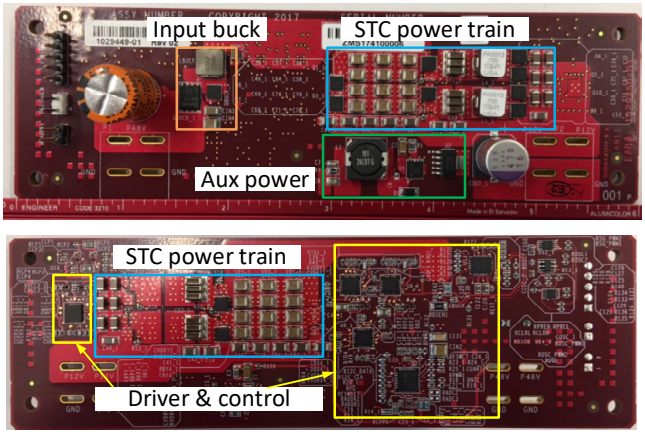
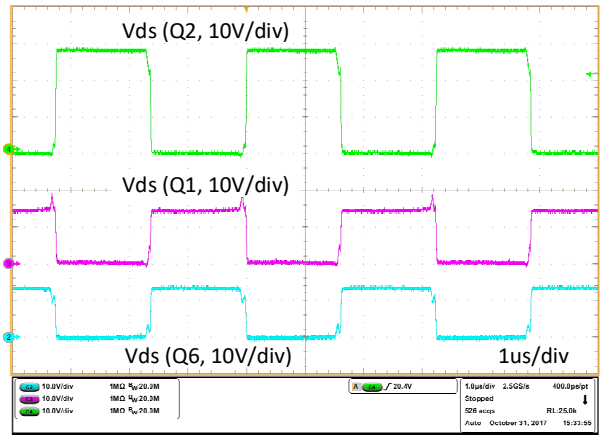
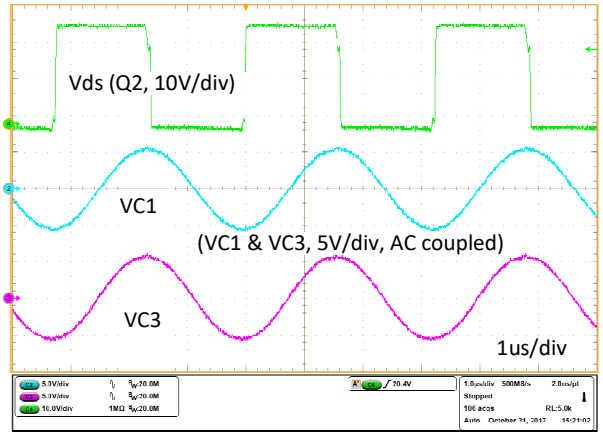


Figure 11. 650W 4-to-1 STC product evaluation board.

Figure 12a shows the steady state waveforms of the drain-to-source voltages across Q1, Q2 and Q8. In this 4-to-1 STC, the maximum voltage stress for Q1-Q4 is 2*VOUT. However, for Q1 and Q4, the nominal blocking voltage is VOUT; during the dead time (100ns in this design), the voltage stress may increase up to 2*VOUT due to switching timing mismatches. All the output SR FETs (Q5 - Q10) have the maximum voltage stress of VOUT. Benefiting from zero current switching, switching spikes can barely be seen with each FET. In Figure 12b, the sine-wave voltage ripples across capacitor C1 and C3 are shown. The peak and valley are both aligned with the switching edges to achieve ZCS. Due to the charge balance principle, the currents in both resonant tanks are automatically balanced.

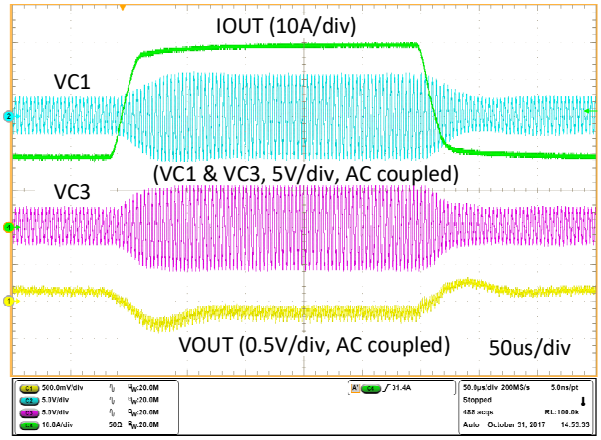


(a)

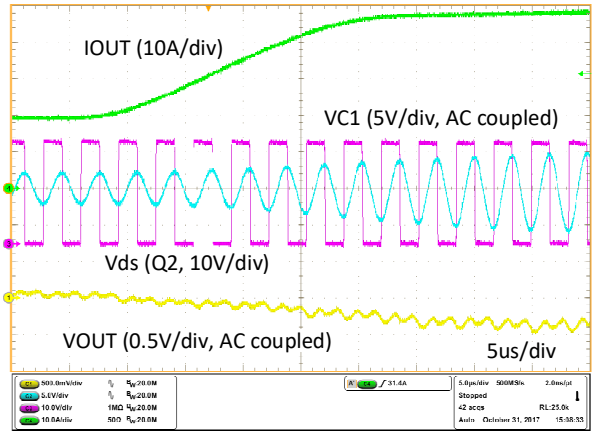


(b)

Figure 12. STC Steady state waveforms (VIN=54V, IOUT=50A).



(a)



(b)

Figure 13. STC load transient waveforms (VIN=54V, IOUT=20A-50A).

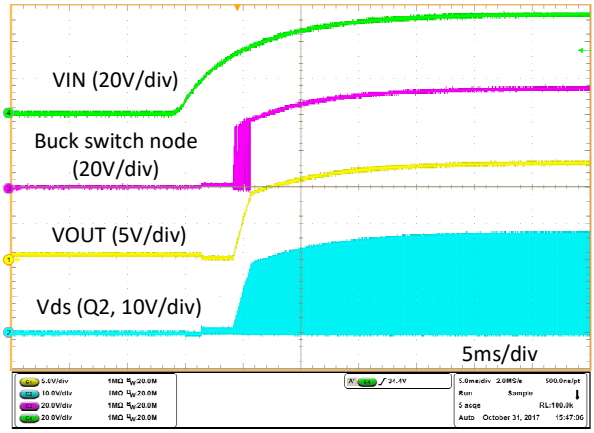


Figure 14. STC startup waveforms (VIN=54V, IOUT=0).

Shown on Figure 13 are the waveforms during the load step transients. The STC demonstrates an intrinsically fast response as there are very little energy storage components in the topology. Figure 14 shows the startup waveforms of STC. Upon startup, the bias power becomes available first when VIN reaches around 15V. At the same time, the STC controller generates switching signals to the STC power train. After a short delay (~3ms), the STC controller issues an enable signal to the input buck for ramp up. The buck converter eventually enters bypass mode (100% duty cycle) once its output voltage reaches the input.

The STC output voltage droop characteristics has been measured and shown in Figure 15. It verifies the STC output resistance model predicted by Eq.(2). And this droop characteristic allows multiple STCs for parallel operation when their internal AC resistances are well matched.

Figure 16 demonstrates the superior efficiency performance of the STC topology. The 4-to-1 STC evaluation board achieves a very high peak efficiency of 98.92% excluding bias power and 98.61% with bias power. At full load, 97.51% without bias and 97.41% with bias are still maintained.

It should be noted that the STC resonant inductors have not been optimized for AC losses yet. Using a dual-phase coupled structure and taking better care of winding ACRs may further improve the full load efficiency. Shown on Figure 17 is the thermal image of the STC board with fan cooling only at full load and room temperature. It shows an extraordinary thermal performance without any heat sink, which significantly

simplifies the thermal management in data center server board designs.

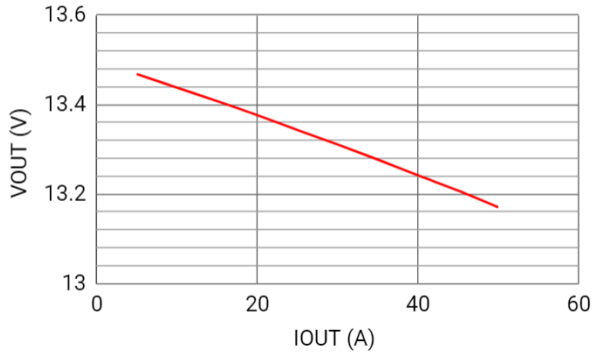


Figure 15. STC output voltage v.s. output current (VIN=54V).

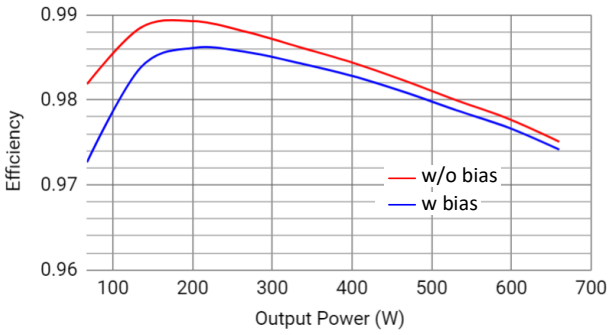


Figure 16. STC efficiency with and without bias power (VIN=54V).

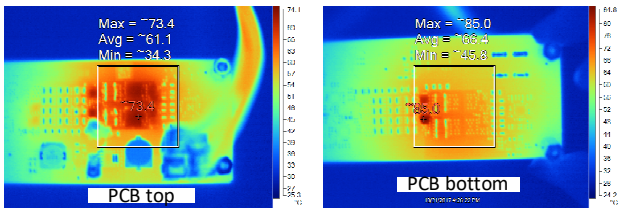


Figure 17. STC thermal performance with fan cooling only (VIN=54V, IOUT=50A, Ta=25C).

VI. CONCLUSION

This paper has presented a new class of Switched Tank Converters for very high efficiency high density DC-DC power conversion where high conversion ratio is required. The STCs uniquely employ LC resonant tanks to partially replace the DC flying capacitors in traditional switched capacitor converters, thus providing complete soft charging, soft switching and minimal device voltage stresses under all operating conditions. The proposed STC topologies overcome the fundamental technical barriers of existing SCC derivative topologies by offering strong robustness against component non-idealities, control simplicity, and extraordinary scalability. Therefore, all these features of STCs have expedited the technology maturity for industry's high volume adoption. In addition to the proposal of the STC topology, an equivalent DCX building block principle has been introduced as a simple and effective analytical tool to better understand the STCs. The same principle can also be applied to analyze other SCC based topologies or derive new topologies.

This paper focuses on one of the emerging applications-48V data center server board power delivery. A 650W 4-to-1 STC evaluation board was designed for the 48V bus converter. Experimental results have been presented to demonstrate the STC operation principles, electrical characteristics, and superior performance (efficiency, density, thermal, etc.).

It should be noted that STCs can be applied to a very broad range of power conversion. Due to the scope limit, many implementation details such as gate driver design, fault protections, input buck design, component integrations, layout considerations, adaptive PWM control schemes and so on are not discussed in this paper.

REFERENCES

[1] X. Li and S. Jiang, "Google 48V power architecture," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, Keynotes presentation.

[2] J. S. Brugler, "Theoretical performance of voltage multiplier circuits," in *IEEE Journal of Solid-State Circuits*, vol. 6, no. 3, pp. 132-135, June 1971.

[3] J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," in *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374-378, June 1976.

[4] F. Ueno, T. Inoue, I. Oota and I. Harada, "Emergency power supply for small computer systems," *1991., IEEE International Symposium on Circuits and Systems*, 1991, pp. 1065-1068 vol.2.

[5] K. D. T. Ngo and R. Webster, "Steady-state analysis and design of a switched-capacitor DC-DC converter," in *IEEE Transactions on Aerospace and Electronic Systems*, vol. 30, no. 1, pp. 92-101, Jan 1994.

[6] S. V. Cheong, H. Chung and A. Ioinovici, "Inductorless DC-to-DC converter with high power density," in *IEEE Transactions on Industrial Electronics*, vol. 41, no. 2, pp. 208-215, Apr 1994.

[7] M. S. Makowski and D. Maksimovic, "Performance limits of switched-capacitor DC-DC converters," *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE*, Atlanta, GA, 1995, pp. 1215-1221 vol.2.

[8] M. Xu, J. Sun and F. C. Lee, "Voltage divider and its application in the two-stage power architecture," *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06.*, Dallas, TX, 2006.

[9] Y. K. Ramadass and A. P. Chandrakasan, "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications," *2007 IEEE Power Electronics Specialists Conference*, Orlando, FL, 2007, pp. 2353-2359.

[10] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841-851, March 2008.

[11] V. W. Ng and S. R. Sanders, "A High-Efficiency Wide-Input-Voltage Range Switched Capacitor Point-of-Load DC–DC Converter," in *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4335-4341, Sept. 2013.

[12] M. Chen, K. K. Afridi and D. J. Perreault, "Stacked Switched Capacitor Energy Buffer Architecture," in *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5183-5195, Nov. 2013.

[13] F. Z. Peng, F. Zhang and Z. Qian, "A magnetic-less DC-DC converter for dual-voltage automotive systems," in *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 511-518, Mar/Apr 2003.

[14] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor-Clamped DC–DC Converter," in *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1628-1638, Nov.-dec. 2007.

[15] C. K. Tse, S. C. Wong and M. H. L. Chow, "On lossless switched-capacitor power converters," in *IEEE Transactions on Power Electronics*, vol. 10, no. 3, pp. 286-291, May 1995.

[16] S. R. Sanders, E. Alon, H. P. Le, M. D. Seeman, M. John and V. W. Ng, "The Road to Fully Integrated DC–DC Conversion via the Switched-Capacitor Approach," in *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146-4155, Sept. 2013.

[17] R. C. N. Pilawa-Podgurski, D. M. Giuliano and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 4008-4015.

[18] D. M. Giuliano, M. E. D'Asaro, J. Zwart and D. J. Perreault, "Miniaturized Low-Voltage Power Converters With Fast Dynamic Response," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 395-405, Sept. 2014.

[19] V. Yousefzadeh, E. Alarcon and D. Maksimovic, "Three-level buck converter for envelope tracking applications," in *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 549-552, March 2006.

[20] D. Cao and F. Z. Peng, "Zero-Current-Switching Multilevel Modular Switched-Capacitor DC–DC Converter," in *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2536-2544, Nov.-Dec. 2010.

[21] Y. Lei and R. C. N. Pilawa-Podgurski, "A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650-5664, Oct. 2015.

[22] P. S. Shenoy, M. Amaro, J. Morroni and D. Freeman, "Comparison of a Buck Converter and a Series Capacitor Buck Converter for High-Frequency, High-Conversion-Ratio Voltage Regulators," in *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7006-7015, Oct. 2016.

[23] O. Keiser, P. K. Steimer and J. W. Kolar, "High power resonant Switched-Capacitor step-down converter," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 2772-2777.

[24] D. Cao, X. Lyu and Y. Li, "Multilevel modular converter with reduced device count for hybrid and electric vehicle," *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, 2015, pp. 1-6.

[25] K. K. Law, K. W. E. Cheng and Y. P. B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 5, pp. 943-948, May 2005.

[26] K. Kesarwani, R. Sangwan and J. T. Stauth, "Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6966-6977, Dec. 2015.

[27] Y. Lei, R. May and R. Pilawa-Podgurski, "Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770-782, Jan. 2016.

[28] Y. Li, B. Curuvija, X. Lyu and D. Cao, "Multilevel Modular Switched-Capacitor Resonant Converter with Voltage Regulation," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 88-93.

[29] K. Zou, M. J. Scott and J. Wang, "A Switched-Capacitor Voltage Tripler With Automatic Interleaving Capability," in *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2857-2868, June 2012.

[30] K. Sano and H. Fujita, "Performance of a High-Efficiency Switched-Capacitor-Based Resonant Converter With Phase-Shift Control," in *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 344-354, Feb. 2011.

[31] M. Shen, "A zero voltage switching switched capacitor voltage doubler," *2012 IEEE International Symposium on Industrial Electronics*, Hangzhou, 2012, pp. 131-136.

[32] D. Cao, X. Lu, X. Yu and F. Z. Peng, "Zero voltage switching double-wing multilevel modular switched-capacitor DC-DC converter with voltage regulation," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2013, pp. 2029-2036.

[33] Y. Li, J. Chen, M. John, R. Liou and S. R. Sanders, "Resonant switched capacitor stacked topology enabling high DC-DC voltage conversion ratios and efficient wide range regulation," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-7.

[34] Y. P. B. Yeung, K. W. E. Cheng, S. L. Ho, K. K. Law and D. Sutanto, "Unified analysis of switched-capacitor resonant converters," in *IEEE Transactions on Industrial Electronics*, vol. 51, no. 4, pp. 864-873, Aug. 2004.

[35] J. T. Stauth, M. D. Seeman and K. Kesarwani, "Resonant Switched-Capacitor Converters for Sub-module Distributed Photovoltaic Power Management," in *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1189-1198, March 2013.

[36] A. Stillwell and R. C. N. Pilawa-Podgurski, "A resonant switched-capacitor converter with GaN transistors for series-stacked processors with 99.8% power delivery efficiency," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 563-570.