Design and Evaluation of Hybrid Switched Capacitor Converters for High Voltage, High Power Density Applications

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***Abstract*— This work investigates the use of hybrid switched capacitor converter (HSCC) topologies with wide bandgap devices to achieve high efficiency DC-DC power conversion with high gain, high voltage outputs. This class of converter may be useful for several applications that include a medium voltage bus, such as solar PV, electric aircraft, or even all-electric ship architectures. Three converter prototypes are considered and evaluated in hardware, including a basic (unipolar) HSCC and two bipolar HSCC variants. The converter operation is discussed, and the bipolar prototypes are demonstrated to achieve high-gain, high-voltage output. Finally, the latest bipolar switched capacitor prototype is demonstrated to boost 480 V to 10 kV (Gain > 20) with 97.9% efficiency at 4.96 kW output power.**

Keywords*— *WBG, High-gain DC-DC converters, MVDC applications, PV, switched capacitor

I. INTRODUCTION

The interest in medium voltage DC (MVDC) and high voltage DC (HVDC) systems has been investigated for various applications ranging from renewable energy sources such as photovoltaics (PV) and wind [1],[2], to electric warships [3],[4]. Traditionally, insulated gate bipolar transistors (IGBTs) have been used to meet high voltage, high power switching needs. Although an IGBT is capable of higher voltage operation than a MOSFET, they are restricted in operating frequency to limit their losses. This results in low power density due to large magnetics, large filter capacitors, and large heatsinks which are required for thermal management.

Wide-bandgap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN), offer higher temperature operation and breakdown voltage. Higher breakdown voltage coupled with lower specific on-resistance [5] and higher switching frequency make them ideal for power conversion allowing for large improvements in power density and a reduction in cost. Through experiment, SiC devices were shown to decrease filter component volume in a 3-phase inverter by 67%, reduce heatsink volume by 92%, and increase efficiency by 2.4% compared to the Si counterpart [5].

Although the boost converter is common in many applications, it is not feasible for MVDC power conversion. With practical limits on duty cycle of around 80%, its voltage gain is restricted to approximately 5 in practice [6]. A high gain converter was investigated in [7] using a DC-DC full-bridge. Although this topology traditionally uses a transformer and switches to achieve gain, two additional transformers were added to act as a snubber for each switch leg. This converter achieved a gain of 16.7, but at the cost of adding three large transformers.

Various researchers have proposed implementing WBG devices into future power converters to reduce their footprint by increasing the switching frequency and reducing passive component sizes. A 7-stage GaN-based flying-capacitor multilevel boost converter was proposed in [8]. A gain of over 9 was achieved by boosting 100 V to 914 V with 750 W output power and 92.7% efficiency. Although this circuit provided good gain and efficiency as well as high power density, the control was complex, requiring a total of 6 active switches. A high-gain switched capacitor topology controlled using only a single switch is discussed in [9]. This topology, referred to herein as the hybrid switched capacitor converter (HSCC), uses a single controlled switch, and several diodes and capacitors configured as a voltage multiplier. Three HSCC prototypes will be presented in this work. These conversion circuits take advantage of WBG devices to achieve high voltage operation, high frequency switching, and high efficiency.

The next section discusses the operation of the HSCC. Section III extends the development of the HSCC to a bipolar configuration (i.e. bipolar HSCC) and demonstrates operation to 10 kV output voltage. Section IV presents an alternative bipolar HSCC design that includes some circuit variation and employs a quasi-square wave (QSW) like control scheme [10]-[13]; this converter is referred to as the bipolar QSW HSCC. In Section V, the performance of the two bipolar HSCC variants is compared, and the impacts of various design features are discussed. Finally, conclusions and future work are discussed in Section VI.

II. HSCC THEORY OF OPERATION

The HSCC includes a boost converter on the front end with N additional stages of capacitor-diode cells connected between the switch node and the output. Each stage is intended to contribute to the gain of the circuit by acting as a voltage multiplier stage. In this section, we first consider a topology referred to herein as the *unipolar HSCC*. This terminology is selected to distinguish this circuit from the bipolar variant discussed later. A 2-stage (N=2) unipolar HSCC is shown in Fig. 1. The circuit in general has one controlled switch, $2N$+1 diodes and $2N$+2 capacitors including an output capacitor.

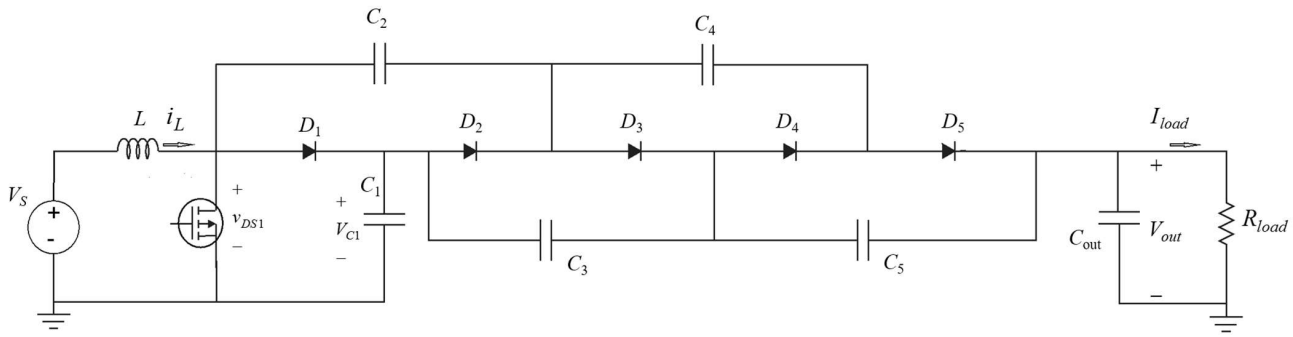

Fig. 1: Circuit schematic for 2-Stage unipolar HSCC

It may also be shown through simulation that the voltages across the capacitors are balanced; specifically, the output voltage appears to divide approximately equally across each stage. This assumes, however, that the capacitance values of all capacitors are approximately equal.

The capacitor-diode cells act as a charge pump. While the switch is on, even numbered diodes (see Figure 1) are forward biased and odd numbered diodes are reverse biased. This allows charge to be exchanged between capacitors on the upper and lower rail. When the switch is turned *off*, diode states reverse causing the inductor's stored energy to be transferred through the upper rail capacitors to the output.

The lower rail capacitors have a direct series connection from the output to ground allowing their node voltages to remain relatively fixed throughout switching transitions. Since the switch node connected to the upper rail capacitors switches between the inductor and ground, their node voltages alternate between node voltages shared by adjacent lower rail capacitors.

Converter operation depends on how the switching is controlled. Initially, a simple pulse width modulation (PWM) duty cycle control with fixed frequency was considered. As shown in [14], the gain of the circuit may be predicted assuming the input inductor current is greater than zero. This control approach is discussed in the next subsection. Hardware and simulation results are then presented.

A. Unipolar HSCC with Constant Duty Cycle and $I_L>0$

Assuming the inductor current remains positive, it is possible to predict the output voltage of the unipolar HSCC with resistive load. The ideal conventional boost converter voltage equation (1) can be combined with the ideal charge pump voltage equation (2) [15] to form the ideal unipolar HSCC voltage equation (3) where V_S is the steady-state input voltage, V_{out} is the steady-state output voltage(s), and D represents the steady-state duty cycle of the active switch.

$$V_{out,boost} = V_{C_1} = \frac{1}{1-D} V_s \tag{1}$$

$$V_{out,CP} = (N+1) V_s \tag{2}$$

$$V_{out,HSCC} = \frac{N+1}{1-D} V_s \tag{3}$$

In [14], equation (3) provided a good estimate of the converter gain when the inductor current was positive. In a conventional boost converter, when the switch turns *off*, inductor current decreases as a negative ramp. If the switch turns *on* before the inductor current reaches zero, it is said to be operating in CCM. Depending on the converter loading, duty cycle, and frequency, the HSCC may operate in a mode where the inductor current can go negative for some portion of the switching period. This is illustrated in a hardware prototype presented in the next subsection, and control in this mode is considered in a later section.

B. Unipolar HSCC Simulation and Hardware Results

Simulations were performed in support of the design of a 4-stage unipolar HSCC using detailed manufacturer SPICE models for a 650 V GaN Systems MOSFET (GS66508T-E02-MR), Rohm SiC diodes (SCS205KGC), 1 µF Kemet MLCC ceramic capacitors (C2220C105KCR2C), and 22 µF Vishay Dale inductor (IHLP6767GZER220M51). Since the capacitors were X7R dielectric, it was important to derate them based on manufacturer's data due to their strong negative C-V characteristic. Although they were rated for 500 VDC, with 125 VDC applied bias, they were effectively reduced from 1 µF to 772 nF (approximately 23%). The inductor SPICE model was also updated to use the measured equivalent series resistance (ESR) as opposed to the value provided by the manufacturer. The prototype was then constructed and tested.

Shown in Fig. 2 is the unipolar HSCC prototype connected to a 25 kΩ resistive load. The converter was built using the same components simulated to further validate the circuit's operational theory.

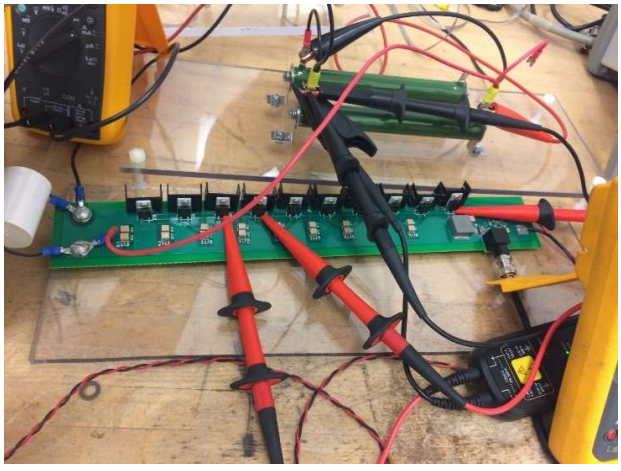

Fig. 2: 4-Stage unipolar HSCC test setup

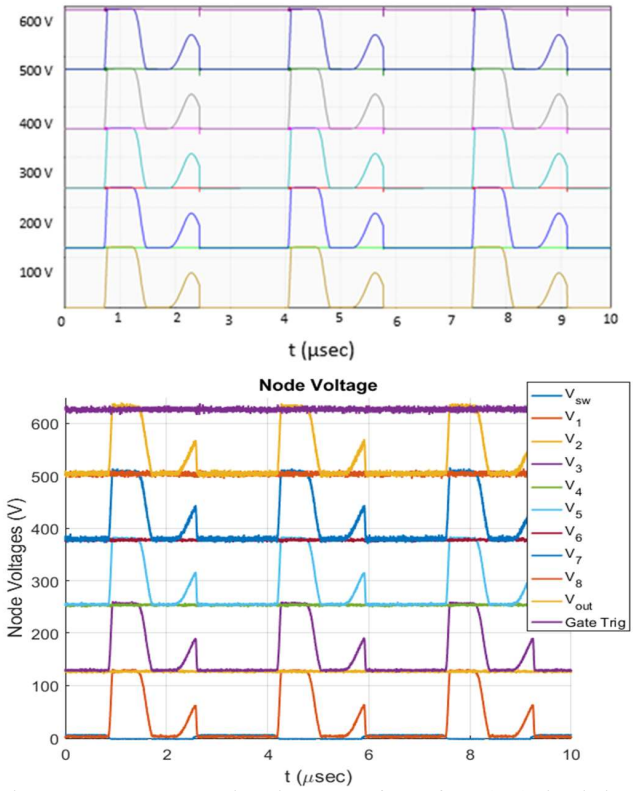

Fig. 3: 4-stage HSCC node voltage waveforms from (top) simulation using LTSPICE and (bottom) hardware measurement, operated using constant duty cycle PWM

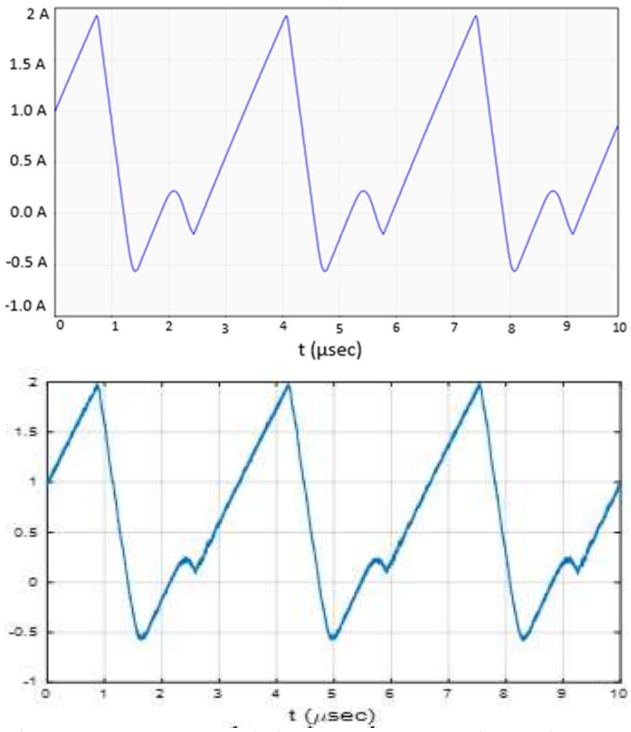

Fig. 4: 4-stage HSCC inductor current waveforms from (top) simulation using LTSPICE and (bottom) hardware measurement, operated using constant duty cycle PWM

Figs. 3 and 4 show results in simulation and hardware for the node voltages and inductor current respectively for an experiment wherein an input voltage of 28 V is boosted to 620 V (Gain > 22). In Fig. 3, V_2, V_4, V_6, and V_8 are rather static as they represent voltages at nodes along the capacitors on the bottom rail. Voltages V_1, V_3, V_5, and V_7 are node voltages along the top rail and are seen to leap from one rail to the other as the transistor switches, illustrating the change in diode conduction states. Simulation results matched closely with hardware, and this experiment yielded a maximum efficiency of 88.1%.

In the HSCC, diode bias states are reversed while the inductor current is negative due to the falling capacitor voltages, even though the switch remains *off*. This portion of time coincides with the sudden drop in top rail node voltages shown in Fig. 3. and with the portion of time the inductor current is negative in Fig. 4. These dynamics are considered in other prototypes, and a control is developed to increase circuit performance; this will be discussed further in Section IV.

III. High Voltage Bipolar HSCC

The bipolar HSCC includes two HSCCs providing positive and negative poles. Shown in Fig. 5 is an example 2-stage (i.e. N=2) bipolar configuration. The negative pole is connected between the negative power supply terminal and ground. Diodes are reversed on the negative pole to account for the opposite direction of current flow. The converter is operated such that the MOSFET switches for the positive and negative poles are switched *on* and *off* simultaneously. Contrasting the converters in Figs. 1 and 5, the naming convention labels both configurations as N=2 stage converters; however, the bipolar configuration has $2N$ total stages due to its positive and negative poles. However, the converter performance is best characterized by the number of stages in each pole; so, this is the preferred convention.

The motivation for the bipolar configuration is to enable higher gain converter applications without overstressing components or diminishing the converter efficiency. In general, as stages are added to the HSCC, the converter gain tends to increase; however, there are practical limits to the number of stages that can be added. Specifically, a modest voltage imbalance from stage-to-stage may result in large voltage differences between the first and last stage at higher power flow. This can result in large voltage stresses on the MOSFET and capacitor C_1, impacting efficiency and reliability. The bipolar design divides the input voltage across two synchronized circuits, improving voltage balance and reducing component stress in high gain applications. Thus, when N is large, it will likely be more efficient to deploy an N-stage bipolar converter rather than a $2N$-stage unipolar converter.

A. High Voltage Bipolar HSCC Hardware - Prototype 1

A prototype bipolar HSCC circuit capable of up to 10 kV output voltage was designed and constructed. Fig. 6 shows a photo of the circuit housed in a high-voltage enclosure. The prototype was designed to allow for a selectable number of output stages. The inductors were sized to allow testing over a range of switching frequencies, as low as 100 kHz. Table I lists the key components. The input to the bipolar HSCC prototype was connected to an Ametek / Sorenson SGI 600/8 power

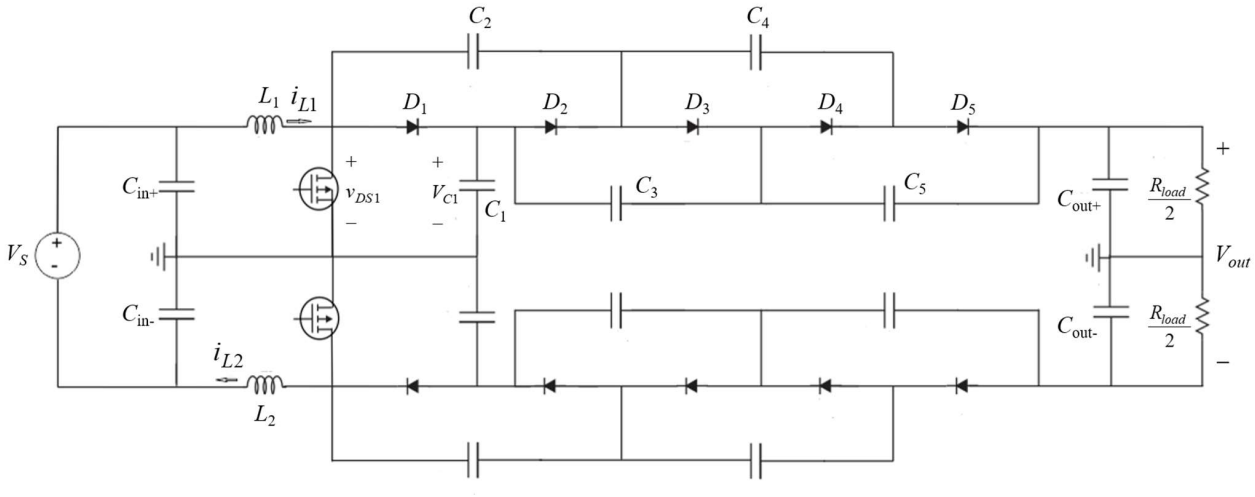

Fig. 5: Circuit schematic for 2-Stage bipolar HSCC

supply. The output was connected to a custom selectable 10 kW resistive load which was manufactured by *HVR Advanced Power Components*. This load provided nominal resistance values of 50 kΩ, 25 kΩ, 16.7 kΩ, 12.5 kΩ, and 10 kΩ. The RMS input and output voltages and currents were measured using Fluke digital multi-meters, and several signals were monitored by a Tektronix TDS 3054C oscilloscope.

The load was placed inside a custom enclosure to provide high-voltage isolation, and fans provided over 1,000 linear feet per minute (lfm) for heat dissipation. The test bed included interlocks for power supply and fan power, for protection of personnel.

For the testing described in this section, the converter was configured with N=4 stages per pole. The supply was configured to supply the prototype with +/- 300V input, and the gating signal driving both MOSFETs was switched at 140 kHz, 0.57 duty cycle. In steady state, the RMS output voltages summed to 10.055 kV at 2.57 kW delivered to the load. Fig. 7 shows the positive and negative pole voltages, the input inductor current for the positive pole, and the 0-5V gating signal delivered to both gate drivers. The output voltage is seen to be effectively +/-5 kV. It should be noted that the inductor current is seen to go slightly negative on the falling edge, exhibiting a similar characteristic as in the unipolar HSCC shown in the preceding section. It should also be noted that the voltage ripple on each pole was measured to be 477 Volts pk-pk average. This is due to the low output capacitance of the circuit and the relatively low switching frequency.

The efficiency at this operating point was measured to be 95.3%. Additional operating points were also tested and will be discussed in Section V.

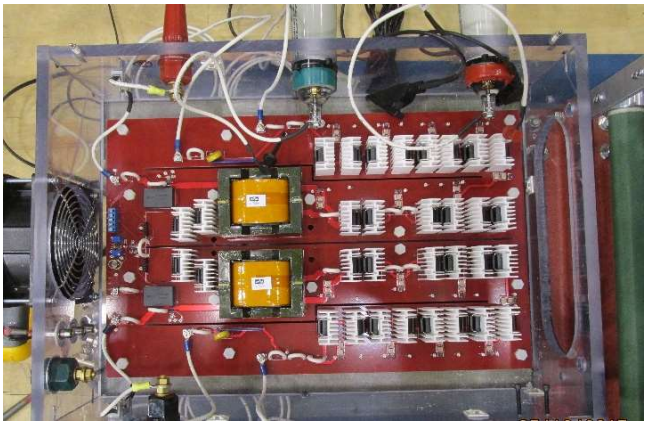

Fig. 6. Bipolar HSCC prototype converter

Table I: Key components used in bipolar HSCC Prototype 1

Component (see Fig. 5)	Description	Manufacturer / Part Number
D_1, D_2, …	SiC Diode, 1.7 kV	Wolfspeed C3D10170H
C_1, C_2, C_3, ...	MLCC, 0.1 µF, 2 kV	Knowles 2220Y2K00104-KXTWS2
sw+, sw-	SiC FET, 1.7 kV	Wolfspeed C2M0045170D
L_1, L_2	Inductor, 58.8 µH, 3.42 mΩ, 32 A rated	West Coast Magnetics 320-04
(not shown)	SiC Gate driver board	Wolfspeed CRD-001

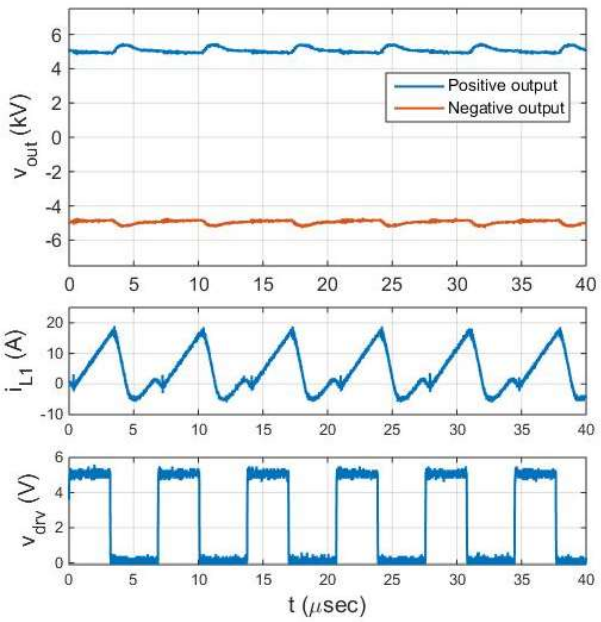

Fig. 7. Bipolar HSCC test data showing output voltages, input inductor current, and trigger signal sent to the gate drivers

IV. Alternate High Voltage Bipolar HSCC Design with QSW Control

A revised bipolar HSCC circuit/system was developed to achieve greater efficiency and higher power. Improvements were gained through the implementation of a new control scheme and through adjustment of the converter parameters.

A. QSW-like Control

In [16], a method to regulate the input power to the converter was developed while also mitigating switching loss. In this control scheme, the MOSFET switches *on* as the inductor current rises through the i_L=0 crossing (when the switch voltage is also near zero) and then switches *off* when a reference peak current is reached. It is assumed that the output voltage divides out approximately equally across each stage; for the bipolar HSCC with N stages on each pole, the steady-state average voltage of the capacitor proximal to diode D_1 is given as [16]

$$V_{C1} = \frac{V_{out}}{2(N+1)} \tag{4}$$

The proposed mode of control focuses on the regulation of the input current and results in characteristic waveforms for the inductor current and switch node voltage. Fig. 8 shows these waveforms for a circuit presented in the next section.

In Fig. 8, three modes of operation are illustrated with labels shown at the top of the figure that include: mode 1 wherein the switch is *on*, mode 2 wherein the switch is *off* and i_L>0, and mode 3 where in the switch is *off* and i_L<0 [16]. It can be shown that the input power is related to the reference peak inductor current according to the approximation:

$$P_{in} = \frac{L}{T_{sw}}\left(1+\frac{V_S(N+1)}{V_{out}-V_S(N+1)}\right)I_{L,pk}^2 + \frac{\tau_{CP}^{\,2}}{LT_{sw}}\left(0.6301\frac{V_S V_{out}}{(N+1)} - 0.4727\frac{V_{out}^{\,2}}{(N+1)^2}\right) \tag{5}$$

where $I_{L,pk}$ is the reference peak inductor current, T_{sw} is the switch period, and the τ_{CP} is a time constant associated with the charge pump on the output stage [16]. While the on time of the control is regulated to get the desired reference peak inductor

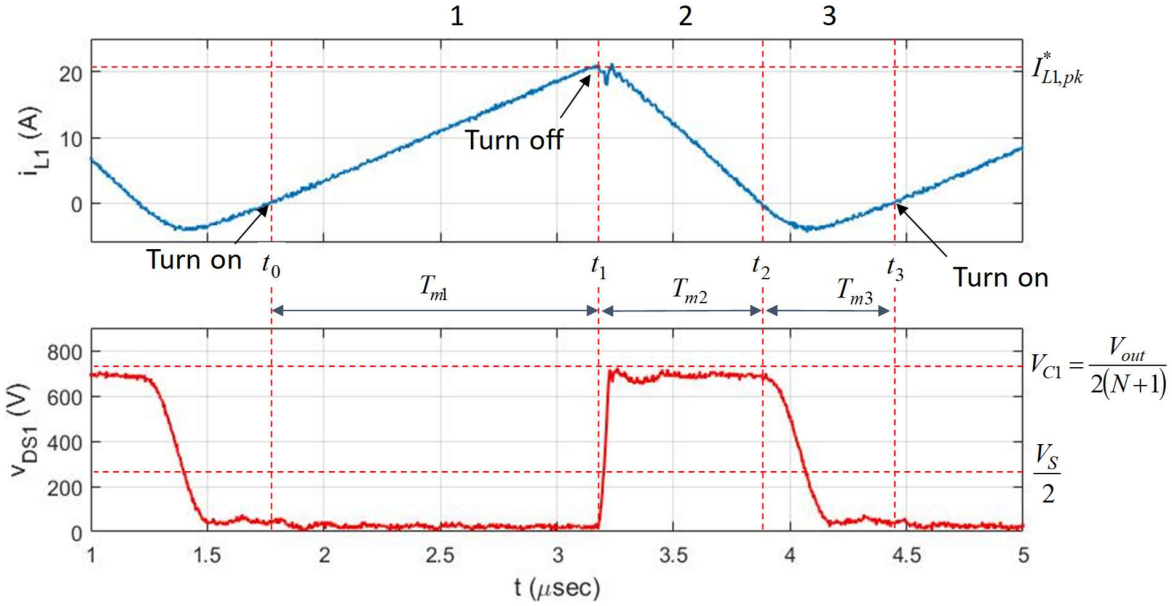

Fig. 8: Characteristic inductor current and drain-source voltage for top pole of 5-stage HSCC prototype; the modes of operation are labeled at the top [16].

current, the dynamic response of the inductor results in a variable off time, causing some variability in the switching frequency, which is shown in [16] to be given as

$$f_{sw} = \frac{1}{T_{sw}} = \frac{1}{\left(\frac{2L}{V_S} + \frac{2L(N+1)}{V_{out} - V_S(N+1)}\right) I_{L,pk} + \frac{1.375\tau_{CP}}{V_S(N+1)} V_{out}} \quad (6)$$

B. High Voltage Bipolar QSW HSCC Hardware - Prototype 2

The revised bipolar HSCC converter included revised values for input inductance and stage capacitance that were identified through simulation studies to provide improved converter efficiency. The stage capacitors were configured using film capacitors in parallel with ceramic X7R capacitors; this enabled good high-frequency response while adding capacitance and avoiding the negative C-V characteristic we'd expect if only ceramic X7R capacitors were used. Input inductance was also reduced, and the above described control was implemented. Fig. 8. shows a photo of the prototype configured with N=5 stages; key components are listed in Table II. The converter was tested using the same enclosure described above, but with an Ametek / Sorenson SGI 600/16 power supply as the source.

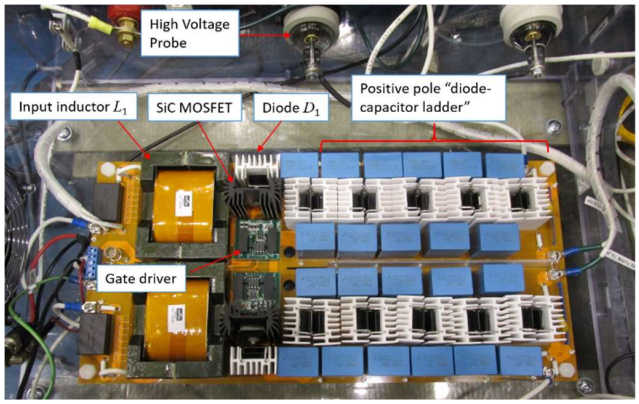

Fig. 9: 5-stage bipolar HSCC (Prototype 2); in this converter, both the positive and negative poles each have 5 stages

Table II: Key components used in Prototype 2

Description	**Manufacturer/ Part Number**
SiC Diode, 1.7 kV, 14.4 A	Wolfspeed C3D10170H
SiC FET, 1.7 kV, 72 A	Wolfspeed C2M0045170D
Film capacitor, 1 µF, 1.5 kV	EPCOS B32024A3105M000
MLCC, 0.1 µF, 2 kV	Knowles 2220Y2K00104-KXTWS2
Inductor, 16.2 µH, 1.03 mΩ, 56 A	West Coast Magnetics 320-07
SiC Gate driver board	Wolfspeed CRD-100
Load Resistor, R_{load}, 25 kΩ	HVR Advanced Power Comp

The switching frequency of Prototype 2 was higher than that of Prototype 1, ranging from approx. 310 kHz to 375 kHz, but closely matching the value predicted by (6) [16]. At full voltage, this bipolar HSCC design was demonstrated to boost 480 V to 10.0 kV (Gain > 20) with 97.9% efficiency at 4.96 kW output power. Additional test results are discussed next.

V. Bipolar HSCC Testing – Performance Comparison and Design Considerations

The bipolar HSCC prototypes were evaluated at many operating points using the load assembly described above. Prototype 1 was evaluated using nominal 25 kΩ and 50 kΩ loads. Prototype 2 was evaluated with N=4 stages using a 25 kΩ load and then evaluated with N=5 stages using 25 kΩ and 16.7 kΩ loads. It should be noted that while these resistance numbers were the nominal values, the resistance tended to drift with temperature. Thus, the output power was computed from measured steady-state load voltage and load current values taken on calibrated instruments.

Fig. 10 shows the converter output power as a function of output voltage and load, illustrating the measurements taken. Comparing the converter efficiencies provides some insight into design best practices. The conversion efficiencies are plotted versus the output power in Fig. 11. Therein, it should be noted that Prototype 1 efficiency is lowest with a steep downturn between 1 kW and 2 kW of output power. This downturn in efficiency is attributed to an insufficient stage capacitance and switching frequency. The impedance seen at the output stage is related to the product of stage capacitance and switching frequency, thus creating a limit to the power throughput before excessive voltage stresses appear on the upstream devices. This is best illustrated by observing the efficiency versus load current; see Fig. 12. Therein, a clear cross-over point appears at approximately 300 mA of output current. Beyond this point, the efficiency deteriorates, and power is implicitly limited by the circuit's ability to tolerate the additional electrical loss.

Prototype 2, configured as a 4-stage bipolar HSCC, was measured (with 25 kΩ load) to have a higher efficiency, and the efficiency appeared to be flat past the 2 kW (past 300 mA) stage. The improvement in efficiency in this range is mainly attributed to the QSW-like control approach which reduces the turn-on losses of the MOSFET switch. Some benefit may also be attributed to the lower resistance in the input inductor and to better balancing and lower ripple in the output stage due to larger capacitances. The fact that the efficiency is flat past the 2 kW point is attributed to the higher stage capacitance and higher switching frequency of Prototype 2.

Prototype 2, configured as a 5-stage bipolar HSCC shows further improvement in efficiency. This may be counter-intuitive since most would expect that the additional devices would result in more electrical losses. However, the additional stages reduce the peak voltage seen by the MOSFET (see equation (4)), reducing the transistor switching loss more than what is lost in the additional diode-capacitor stages. Considering for a moment just the tests done using the 25 kΩ load in the range (2 kV-7 kV), Prototype 1 was 96.5% efficient

on average, Prototype 2 (N=4) was 97.2 % efficient, and Prototype2 (N=5) was 97.6% efficient.

Prototype 2 with N=5 stages was tested over several operating points and is seen to have a very flat efficiency curve over its whole operating range. A peak power of 5.43 kW was achieved with V_s = 450V, V_{out} = 8.74 kV, achieving a gain of 19.4 with conversion efficiency of 97.4 %. For V_s = 480V, a peak output voltage of V_{out} = 10.0 kV (gain of 20.8) was achieved, with 4.96 kW output power and a conversion efficiency of 97.9%. The dimensions of Prototype 2 are approximately 15.7"x7.4"x2", for a volume of 232 in^3, with a demonstrated power density of about 23 W/in^3 based on peak power achieved.

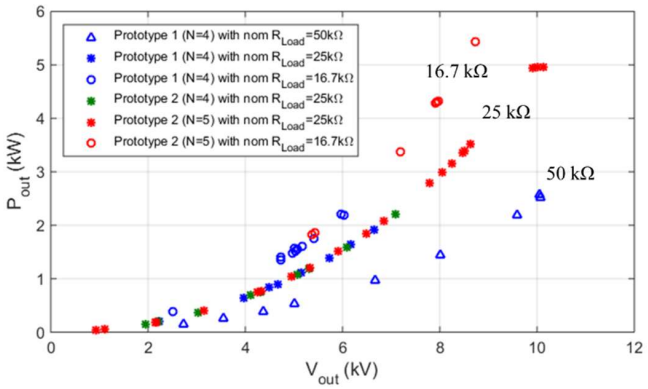

Fig. 10: Converter output power versus output voltage for three nominal loads

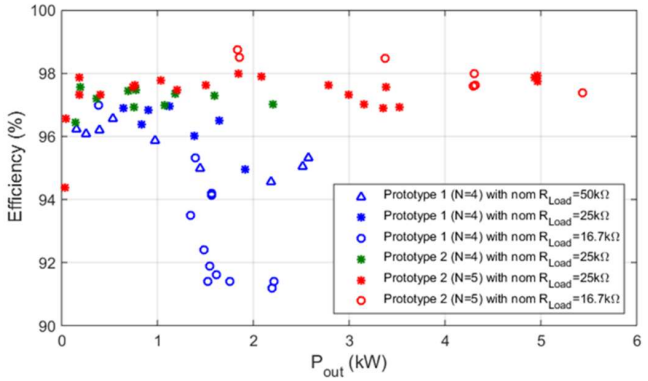

Fig. 11: Conversion Efficiency versus output power

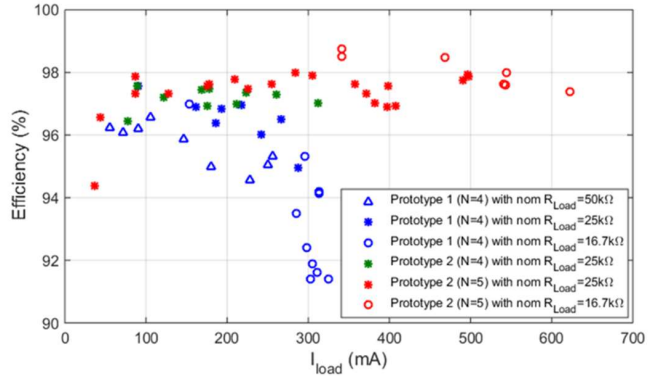

Fig. 12: Conversion Efficiency versus load current

VI. Conclusions and Future Work

This paper presented the hybrid switched capacitor converter for use in high-performance power electronic applications. Unlike other switched capacitor converters, this topology uses fewer controlled switches and relies on diode-capacitor stages to realize added gain. By using WBG switches and diodes, high-frequency, high-voltage, and high-efficiency operation is attainable. Three prototypes were presented with hardware results.

A unipolar HSCC was designed using a GaN MOSFET and SiC diodes to demonstrate the feasibility of a high-gain converter using a single active switch, diodes, and capacitors and to illustrate its operation. A bipolar HSCC configuration was then presented capable of 10 kV output. Improvements to the design and to the control and operation of the converter were then demonstrated in a third prototype referred to as a bipolar QSW HSCC converter. This converter achieved 97.9% efficiency at 10 kV and 4.96 kW output, with a modest peak power density of about 23 W/in^3.

The performances of the bipolar converters were compared, and key design aspects impacting efficiency and power handling ability were discussed.

With a better understanding of circuit operation, power density may be further improved by utilizing advanced packaging and cooling techniques. Future work will focus on making continued improvement in the power density and output voltage handling of this exciting converter topology.

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