Control Technique for Reliable Operation of the Synchronous Series Capacitor Tapped Inductor Converter

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***Abstract*—In the context of reducing total CO_2 emissions as well as reducing the total copper cable length and weight on cars, automotive manufacturers propose to derive all the supply voltages from a single $48\ \mathrm{V}$ bus through high step-down ratio dc-dc converters. The series capacitor tapped inductor (SCTI) converter is a promising topology for efficient single-stage step-down conversion from the $48\ \mathrm{V}$ bus. In the *synchronous* version of the SCTI, however, turn-off of the synchronous rectifier at positive drain-to-source current leads to a voltage spike and to a potential catastrophic failure of the converter. In this paper a simple control technique is proposed which prevents the foregoing condition to occur. The approach enables a reliable operation of the synchronous SCTI topology without disrupting its main features and advantages, and eliminating the need for additional snubbers, voltage clamps or auxiliary windings. The approach is validated via computer simulations and experimental tests on a $48\ \mathrm{V}$-to-$1.5\ \mathrm{V}$, $4\ \mathrm{A}$ SCTI converter prototype.**

I. Introduction

To address the need to limit CO_2 emissions and to decrease both weight and cost of on-board wiring cables, car manufacturers propose to introduce a $48\ \mathrm{V}$-based bus voltage standard [1], and to derive all the required supply voltages locally by means of small integrated dc-dc converters capable of efficiently handling a large step-down ratio. For example, specifications for a microcontroller power supply may impose an output voltage of $1.5\ \mathrm{V}$ at $5\ \mathrm{A}$, for a step-down ratio smaller than $\approx 3\ \%$ considering input voltage transients. While standard Buck topologies cannot efficiently handle such large step-down ratio requirement, there exist a number of high step-down conversion topologies which represent potential candidates for the automotive scenario [2]–[11].

The Tapped-Inductor Buck converter (TIB) and series-capacitor Buck converter (SCB), for instance, represent valid alternatives [2], [3], [6]. The main drawback of TIB converters is represented by the leakage inductance of the magnetic element, which causes large voltage spikes upon turn-off of the high-side MOSFET. Clamping circuits can be added at the cost of increasing the topology complexity and overall cost [3]. As for the SCB topology [5], [6], it does not have the above shortcomings but it is only capable of doubling the duty cycle with respect to the traditional Buck topology.

The series capacitor tapped inductor (SCTI) converter [7]–[9], illustrated in Fig. 1a represents a promising topology for the considered application which can bring a significant increase in the operating duty cycle. The SCTI topology achieves zero voltage switching (ZVS) turn-on for the three power devices, while it exhibits zero current switching (ZCS) turn-on for Q_3. The reduced switching losses and the increased duty cycle make the topology suitable for high-frequency operation, integration and large step-down applications. On the other hand, one major drawback of this converter is the large voltage spike appearing across Q_3 as a result of hard turn-off during *transient* events, which strongly compromises the reliability of the converter and limits its attractiveness.

In this paper a simple and effective control technique is proposed for the SCTI topology to prevent such phenomenon to occur. The proposed approach, sketched in Fig. 1b and described in detail in section IV, operates on a switching

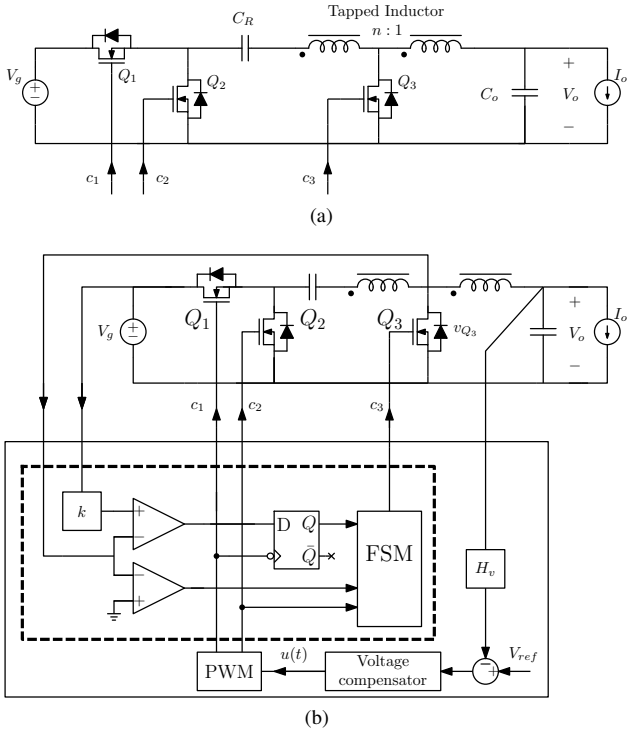

Fig. 1. (a) Synchronous series capacitor tapped inductor (SCTI) topology, and (b) converter with the proposed control technique.

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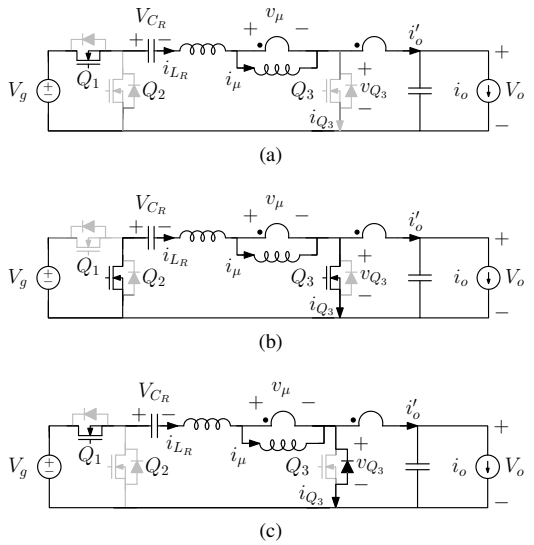


Fig. 2. SCTI during (a) ON-phase, (b) OFF-phase, and (c) free-wheeling phase.

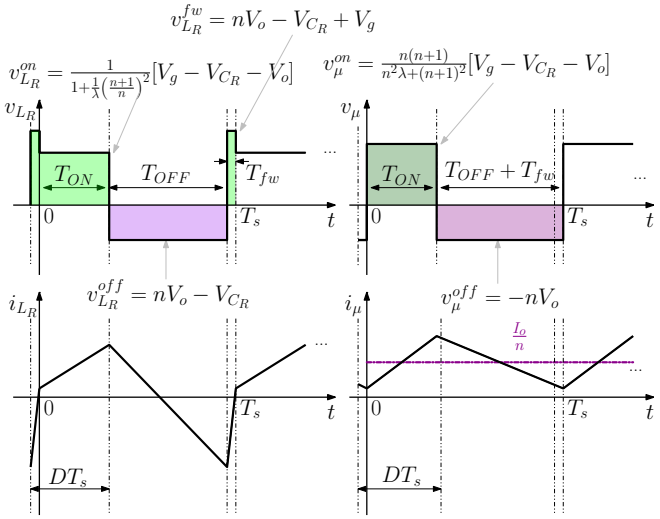


Fig. 3. Qualitative steady-state plots of voltages and currents associated with the magnetizing and leakage inductances.

cycle basis to prevent Q_3 to turn-off at positive drain-to-source current. The approach only involves sensing of the input voltage and of the drain voltage of Q_3, which are simply compared with two appropriate thresholds, with no need for dedicated analog conditioning of A/D conversion channels.

Section II first provides a general steady-state analysis of the SCTI topology, extending some of the results previously reported in the literature [7], [8]. Section III discusses the over-voltage issue concerning Q_3 as a result of hard turn-off during transient events. The proposed control technique is then disclosed in section IV, and validated experimentally in section V on a discrete 48 V-to-1.5 V, 4 A SCTI prototype.

II. Steady-State Analysis of the SCTI Converter

Steady-state analysis of the ideal (lossless) SCTI converter is here developed under the small-ripple approximation (SRA) for all capacitor voltages [12]. The switching rate is therefore assumed to be sufficiently higher respect to resonant frequencies. Notice that the analysis excludes those cases in which C_R acts as a resonant capacitor, and the SCTI operates in resonant mode.

The SCTI topological states are illustrated in Fig. 2, in which the tapped inductor is modeled by a magnetizing inductance and a leakage inductance. The converter is assumed to be operated via a constant frequency PWM with duty cycle D controlling the operation of switch Q_1. As for switches Q_2 and Q_3, they operate in a complementary fashion with respect of Q_1. The control signals of power devices are c_1, c_2, c_3 respectively. The SCTI operates in the following sub-topological states (refer to Fig. 3 for the main current waveforms):

- On-time (Q_1 ON, Q_2 and Q_3 OFF, Fig. 2a). The end of this time interval in the follow is indicated as T_{ON}. During this time interval the currents through magnetizing and leakage inductance increase. Therefore the energy stored in both inductance increases.
- Off-time (Q_1 OFF, Q_2 and Q_3 ON, Fig. 2b). In this time interval magnetizing and leakage currents decrease. The output and i_{Q_3} currents are a linear combination of magnetizing and leakage currents (e.g. $i_{Q_3} = (n+1)i_{L_R} - ni_\mu$).
- Freewheeling time (Q_1 ON, Q_2 OFF, Q_3 OFF but in body-diode conduction, Fig. 2c). This situation is sketched on Fig. 2c. During this interval the energy stored in magnetizing inductance continues to decrease, while the energy stored in leakage inductance quickly increases.

Notice that the average value of i_μ corresponds to the output current divided by turns ratio n, while the DC value of i_{L_R} is necessarily zero.

A. Voltage Conversion Ratio

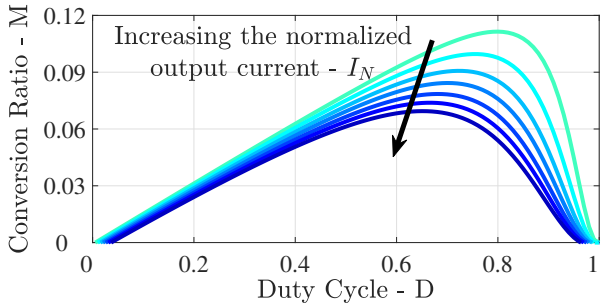
Under the hypotheses discussed so far, application of the volt-second balance and charge balance equations [12] leads to the converter voltage conversion ratio

$$M(D, I_N) = \frac{(1-D)\left[(1-D)\,D\,\dfrac{n+1}{\lambda} - I_N\right]}{\left[\lambda + \left(\dfrac{n+1}{n}\right)^2\right]\left[\dfrac{n^2}{\lambda}(1-D)^2 + \dfrac{n^2}{n+1} I_N\right]}, \quad (1)$$

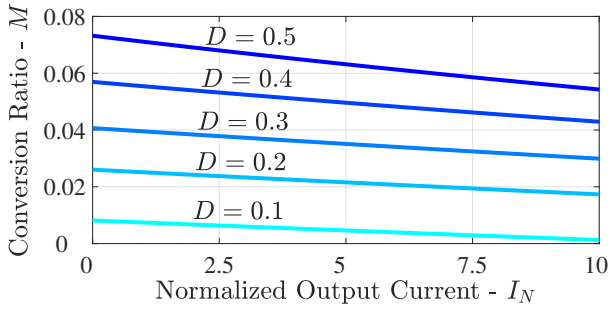
where

$$I_{oN} \triangleq \frac{V_g}{2 f_s L_\mu}; \quad I_N \triangleq \frac{I_o}{I_{oN}}; \quad \lambda \triangleq \frac{L_R}{L_\mu}. \quad (2)$$

This relation is general and includes the dependence of M on the load current, switching frequency and parameters of the tapped inductor. Eq. (1) is sketched in Fig. 4a for different values of normalized output current. The conversion ratio versus the normalized output current I_N is illustrated In Fig. 4b for different values of D. Notice that the dependence on the output current is almost linear.



(a)



(b)

Fig. 4. Voltage conversion ratio M as a function (a) of the duty cycle, and (b) of the normalized output current I_N.

The derived expression represents an extension of some of the results previously reported in the literature. For instance, in open circuit condition ($I_o = 0$), (1) reduces to [7], [8]:

$$M_0 \triangleq M(D,0) = \frac{D}{n+1}\,\frac{1}{1+\lambda\left(\frac{n}{n+1}\right)^2}, \qquad (3)$$

which exhibits a linear dependence on D. Furthermore, one has $M \leq M_0$ for all values of output current. Approximation $M \approx M_0$ is valid at low currents, when the freewheeling time is short enough to be negligible in the analysis. In this case the sub-topology corresponding to freewheeling time disappears and the SCTI operates across two topological states. During the on-time the source energy is stored in magnetizing inductance, and released to the output stage during off-time.

Notice that (3) well approximates into

$$M_0 \approx \frac{D}{n+1} \qquad (4)$$

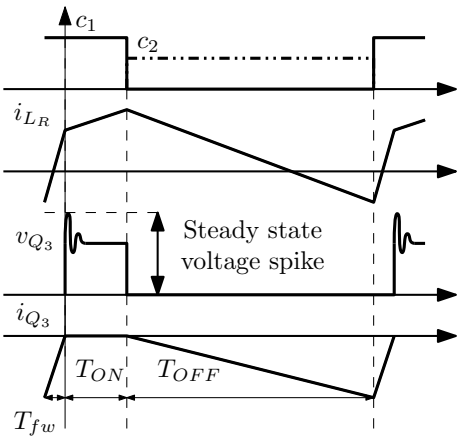
as long as

$$\lambda \ll \left(\frac{n+1}{n}\right)^2, \qquad (5)$$

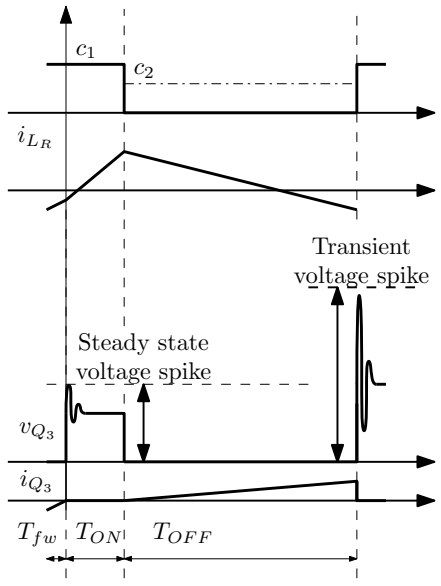
a condition which is easily met in practice.

B. Steady-state voltage ringing across Q_3

If the output current is not negligible, the freewheeling time sub-topology follows the off-time sub-topology, and a voltage ringing appears at drain node of Q_3. This phenomenon is similar to what occurs in a buck converter working in DCM [12]–[14]. The waveform corresponding to the steady-state operation are sketched in Fig. 5a.



(a)



(b)

Fig. 5. (a) Steady-state waveforms including the steady-state voltage ringing across Q_3, and (b) transient waveforms showing the large voltage spike caused by the hard turn-off of Q_3.

This type of *steady-state* ringing does not pose a reliability issue as long as the voltage rating of Q_3 is adequate. As discussed in section III, on the other hand, a much more severe voltage spike across Q_3 can occur during *transient* conditions in which Q_3 turns-off at positive drain-to-source currents.

C. Discussion

In the following, the main properties of SCTI working in steady-state are summarized.

First, as anticipated, the SCTI topology is capable of producing extremely small M's for a wide range of duty cycles,

which makes the converter extremely attractive for single-stage, high step-down scenarios.

Consider a practical case of a 40 V-to-100 V input, 1.5 V output dc-dc application for emerging automotive standards based on the 48 V dc bus. A classical CCM Buck converter would operate at $D = M \approx 1.5\% - 3.8\%$. On the other hand, a tapped inductor Buck converter (TIB) with turns ratio $n = 5$ has a voltage conversion ratio

$$M_{TIB} = \frac{D}{n-(n-1)D} \approx \frac{D}{n} \quad \text{(small } D\text{)}, \tag{6}$$

and would therefore operate at $D \approx 7\% - 16\%$. Using the SCTI for the same application, with the same turns ratio $n = 5$, the corresponding duty cycle would be $D \approx 10\% - 24\%$ according to (4).

Therefore, the TIB and SCTI operate across similar duty cycle ranges, with the SCTI providing a slightly better duty cycle expansion. On the other hand, while the TIB topology suffers from the well known issue of the leakage inductance, which causes large voltage spikes upon turn-off of the high-side MOSFET, the SCTI does not have this problem due to C_R forcing soft-switching of the input bridge.

More generally, notice that all three power devices of the SCTI operate at ZVS turn-ON, and Q_3 also exhibits ZVS at turn-off and ZCS at turn-on. Behaviour of $i_{L_R}(t)$ and $i_\mu(t)$, when output current is different than zero, are reported in Fig. 3.

In regard to the ZVS turn-off of Q_3, a few remarks are necessary. This condition can be proved by imposing $i_{Q_3} < 0$ at the device turn-off instant, which occurs if and only if the slope of i_{Q_3} is negative during the off-time. The steady-state condition for soft switching can therefore be written as

$$\left.\frac{\mathrm{d}i_{Q_3}}{\mathrm{d}t}\right|_{t=T_{ON}} = (n+1)\frac{V_{L_R}}{L_R} - n\frac{V_\mu}{L_\mu} \leq 0. \tag{7}$$

By solving (7) with respect to V_{C_R}, condition for ZVS turn-off of Q_3 becomes

$$v_{C_R} > n\left(1 + \frac{\lambda n}{n+1}\right) M V_g. \tag{8}$$

In order to prove (8), consider first that, in steady-state, the following equations hold,

$$\begin{aligned} V_{C_R} &= DV_g - V_o \\ M_0 &> M. \end{aligned} \tag{9}$$

Using the above results in (8), the following chain of inequalities can be written,

$$\begin{aligned} &DV_g - V_o\,(I_o > 0) > \\ &DV_g - V_o(I_o = 0) = n\left(1 + \lambda\frac{n}{n+1}\right) M_0 V_g > \\ &\qquad\qquad n\left(1 + \lambda\frac{n}{n+1}\right) M V_g, \end{aligned} \tag{10}$$

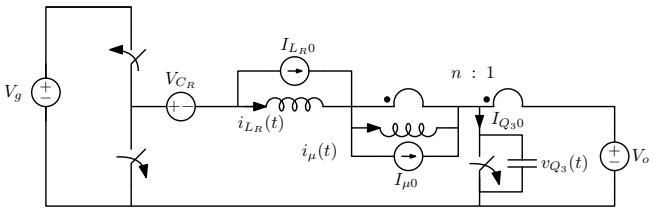


Fig. 6. Circuit model used for transient analysis of the over-voltage event across Q_3.

where the central equality is easily proved,

$$\begin{aligned} &DV_g - V_o\,(I_o = 0) = \\ &\left[(n+1)\left(1 + \lambda\left(\frac{n}{n+1}\right)^2\right) - 1\right] M_0 V_g \\ &= n\left(1 + \lambda\frac{n}{n+1}\right) M_0 V_g \end{aligned} \tag{11}$$

Therefore the ZVS turn-off condition for Q_3 expressed by (8) is always verified in steady-state.

III. SCTI Transient Over-Voltage Issue

As established in section II-C, Q_3 always undergoes ZVS turn-off *in steady-state*. On the other hand, during a transient induced, for instance, by a fast variation of the duty cycle, the drain-to-source current of Q_3 may be positive at device turn-off, as exemplified in Fig. 5b. This causes a hard turn-off of Q_3 which, in the SCTI topology, leads to a severe voltage spike at the drain of Q_3. The reason for such severe voltage spike is the resonance between the device output parasitic capacitance and inductances L_R and L_μ, excited by the sudden variation in the inductive currents i_{L_R} and i_{L_μ}. It is important to notice that the voltage spike is only limited by the characteristic impedance Z_o of the parasitic resonant circuit: with a hypothetical ideal device having zero output capacitance, turn-off of Q_3 at positive drain-to-source current would cause inductive currents i_{L_R} and i_{L_μ} to undergo an abrupt discontinuity, causing the resulting voltage spike to have infinite amplitude.

A. Analysis of the over-voltage event at Q_3 turn-off

Fig. 6 illustrates the circuit model used in the following to analyze the over-voltage event occurring when Q_3 turns-off at positive current during a transient condition. In the circuit model, capacitor C_R is approximated by a short-circuit during the spike event, and only its initial condition $V_{C_R} = DV_g - V_o$ is retained, corresponding to the dc value of v_{C_R}. This choice is consistent with the small-ripple approximation hypothesis made at the beginning of our analysis. The same considerations can be made for output capacitance. The ideal turn-on and turn-off of Q_1 and Q_2 respectively can be analytically modeled by a step function $1(t)V_g$, when $1(t)$ is the unit step function. For the sole purpose of obtaining a rough estimate of the voltage spike across Q_3, no lossy elements are included in the model.

TABLE I
PARAMETERS OF THE CASE STUDY SCTI CONVERTER.

Nominal input Voltage V_g	48 V
Input voltage range	40 V-90 V
Output voltage V_o	1.5 V
Output current I_o	4 A
Switching frequency f_s	195.3 kHz
Tapped inductor turns ratio n	5
Leakage Inductance	2.6 µH
Magnetizing Inductance	16 µH
Series capacitance C_R	3 x 33 µF
Output capacitance C_o	33 µF
V_g sensing attenuation factor α	0.047
v_{Q_3} sensing attenuation factor β	0.18

Current I_{Q_30} represents the current through Q_3 at the device turn-off instant, and is related to the initial conditions I_{L_R0} and $I_{\mu 0}$ on the leakage and magnetizing inductance by

$$I_{Q_30} = (1+n)I_{L_R0} - nI_{\mu 0}. \tag{12}$$

By solving the evolution of the circuit in Fig. 6, the voltage $v_{Q_3}(t)$ can be written as

$$v_{Q_3}(t) = \sqrt{V_p^2 + \left(I_{Q_30}\, Z_o\right)^2}\, \cos(\omega_o t - \theta) + V_p, \tag{13}$$

where

$$\begin{aligned}
\omega_o &\triangleq \frac{1}{\sqrt{C_{Q_3} L_R}}\,(n+1)\sqrt{1+\lambda\left(\frac{n}{n+1}\right)^2} \\
Z_o &\triangleq \frac{1}{\omega_o C_{Q_3}} = \sqrt{\frac{L_R}{C_{Q_3}}}\,(n+1)\sqrt{1+\lambda\left(\frac{n}{n+1}\right)^2} \\
V_p &\triangleq V_o + V_g\,\frac{1-D}{n+1}\left(1+\lambda\left(\frac{n}{n+1}\right)^2\right)^{-1} \\
\theta &\triangleq \arctan\left(\frac{I_{Q_30}\, Z_o}{V_p}\right)
\end{aligned} \tag{14}$$

The voltage peak at the drain of Q_3 can be expressed as

$$V_{Q_3MAX} = V_p\left(1+\sqrt{1+\left(\frac{I_{Q_30} Z_o}{V_p}\right)^2}\right) \tag{15}$$

This peak depends on the operating point (V_g, D, I_o), on the initial condition I_{Q_30}, on the capacitance C_{Q_3} and on tapped inductor parameters (λ, n, L_R). Notice that, as anticipated, the larger the characteristic impedance Z_o of the resonant circuit is, the larger the spike.

Voltage spike V_{Q_3MAX} is reported in Fig. 7 as a function of the drain-to-source current i_{Q_3} and for the reference values summarized in Tab. I. In the plot, a parasitic capacitance $C_{Q_3} \approx 0.1$ nF is assumed. As expected, the voltage spike is more and more severe as the leakage-to-magnetizing inductance ratio L_R/L_μ increases.

The transient over-voltage issue here briefly outline represents a strong reliability limitation of the synchronous SCTI converter. In the next section, a control provision is proposed which prevents such event to occur on a switching cycle basis.

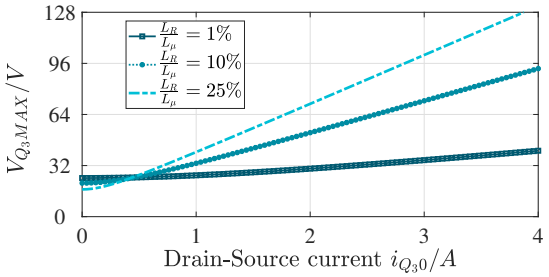


Fig. 7. Estimated voltage spike across Q_3 with respect to the drain-to-source current i_{Q_30} at the turn-off instant.

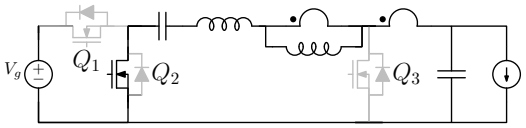


Fig. 8. Intermediate topological state IDLE introduced by the approach during critical switching cycles.

IV. PROPOSED CONTROL TECHNIQUE

The over-voltage event discussed in section III occurs when condition (7) for ZVS turn-off of Q_3 is not satisfied. Therefore the condition for ZVS turn-off Q_3 is also the condition for safe turn-off of Q_3. In fact, if $di_{Q_3}/dt > 0$ at $t = T_{ON}$, then it will be certainly positive at Q_3 turn-off. Viceversa, if $di_{Q_3}/dt < 0$ at $t = T_{ON}$, then it will be certainly negative when Q_3 is turned off. In summary, condition for safe switching of Q_3 can be tested *before* entering the OFF state directly from sign of $di_{Q_3}/dt|_{t=T_{ON}}$ or, equivalently by evaluating condition (8) at the same instant.

The proposed technique introduces an additional topological state in between states ON and OFF, called IDLE and illustrated in Fig. 8, and which only occurs in those switching cycles that would cause the overvoltage problem. To exemplify the approach, consider Fig. 9. For $t = T_{ON}$, if the condition on v_{C_R} is not satisfied the proposed technique turns on Q_2 but leaves Q_3 temporarily off, setting the topology in IDLE state. In this condition Q_3 and its body diode are both off and V_{Q_3} decreases. Consequently v_{C_R} increases, due to positive magnetizing current, until condition (8) becomes true. At this point Q_3 is turned on and the SCTI enters the OFF state. Notice that, in steady-state, the proposed approach is entirely inactive, and does not interfere with the normal converter operation. At the same time, the IDLE state can be introduced for several consecutive switching cycles during a transient, to prevent hard turn-off of Q_3.

Fig. 10 reports the simulation of a transient induced in the converter described by parameters of Tab. I by an abrupt duty cycle step from 20% to 30%. With the proposed approach

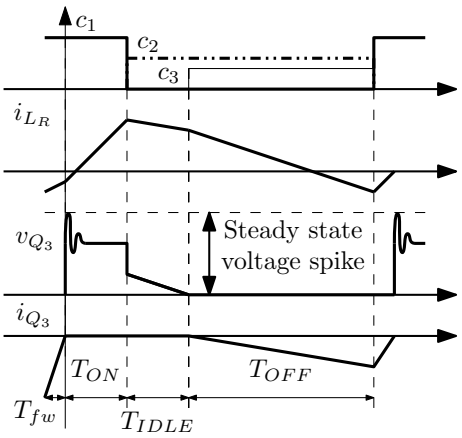
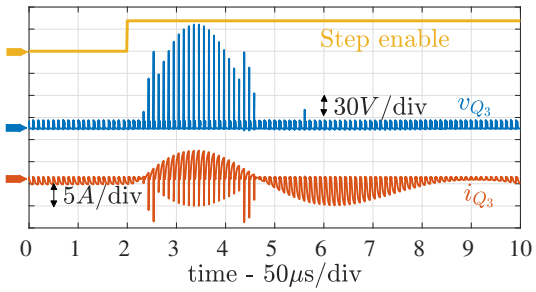
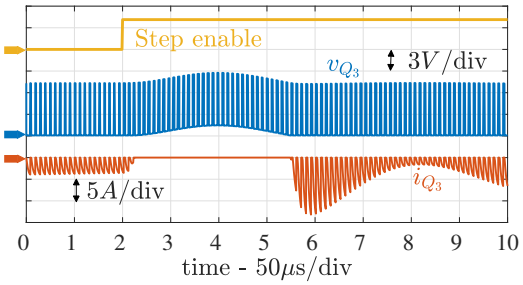


Fig. 9. Operation of the proposed approach during a critical switching cycle.



(a)



(b)

Fig. 10. Simulated transient due to a 20%-to-30% duty cycle variation (a) without and (b) with the proposed approach.

disabled (Fig. 10a), a voltage spike clearly appears across Q_3. When the proposed approach is enabled, the transient causes the proposed technique to intervene, preventing current i_{Q_3} from becoming positive and eliminating the voltage spike across Q_3.

A. Practical implementation of the approach

Directly monitoring condition (8) would present some technical challenges, as it would involve an accurate differential sensing of v_{C_R}. Presence of high-frequency common-mode voltage at the terminals of C_R would further complicate the

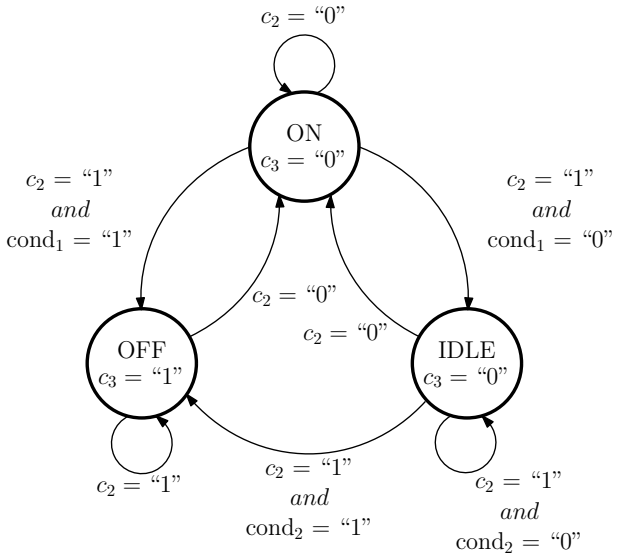


Fig. 11. FSM state transition diagram of the proposed technique.

sensing. However, (8) can be equivalently expressed by the following two conditions on v_{Q_3},

$$v_{Q_3} \leq \begin{cases} kV_g & \text{during } T_{ON} \quad (\text{cond}_1) \\ 0 & \text{during } T_{IDLE} \quad (\text{cond}_2), \end{cases} \tag{16}$$

where

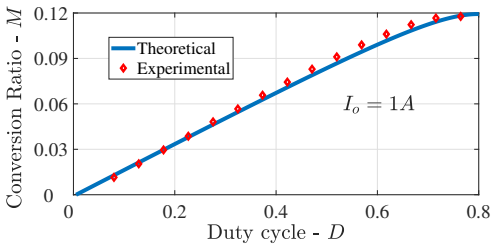
$$k \triangleq \frac{1}{n+1} \frac{1}{1+\lambda\left(\frac{n}{n+1}\right)^2} \approx \frac{1}{n+1}, \tag{17}$$

under the same approximation as (5). With this equivalent formulation, the system enters the IDLE state if $v_{Q_3} < kV_g$ at the end of the on-time. The IDLE state is then maintained either until $v_{Q_3} \leq 0$, or until the end of the switching period, whichever comes first. In the first case the system is brought into the OFF state, while in the second case a new switching period starts with the converter in the ON state.

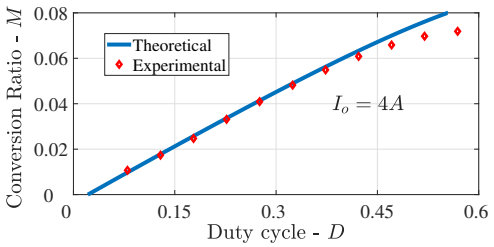
These steps are summarized by the FSM state transition diagram illustrated in Fig. 11. This diagram can be implemented with simple digital and analog components, as detailed in the next section.

V. Experimental Results

A 48 V-to-1.5 V, 4 A SCTI converter is prototyped using discrete components for the purpose of verification of the proposed technique. Parameters of the converter are reported in Tab. I. The converter is here tested open-loop, with the proposed technique implemented partially on-board (analog comparators), and partially on a FPGA commercial development board (modulation logic and FSM) for the purpose of rapid proof-of-concept verification. Notice, however, that the digital portion of the proposed technique is simple enough to be integrated in a custom-designed IC.



(a)



(b)

Fig. 12. Theoretical (solid line) vs. experimental (dots) voltage conversion ratio for (a) $I_o = 1$ A and (b) $I_o = 4$ A.

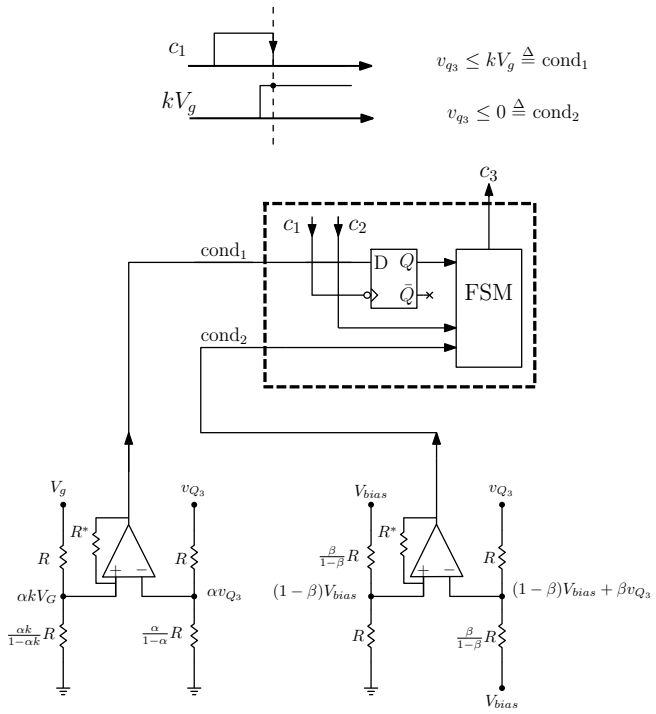


Fig. 13. Implementation of the proposed control technique. The inequalities of system 16 are implemented with two comparators.

A. Conversion Ratio

In order to verify the relation (1), steady-state measurements are carried out on the prototype. In Fig. 12 a comparison between the theoretical and measured voltage conversion ratio is reported for two distinct load current levels, namely $I_o = 1$ A in Fig. 12a and $I_o = 4$ A in Fig. 12b. The comparison fully confirms the accuracy of the analysis disclosed in section II-A, which in turn is an extension of previously reported results for the SCTI topology.

B. Proposed control technique

Conditions (16), which implement the proposed control technique for avoiding the over-voltage issue at the drain of Q_3, are realized with two separate comparators, while the subsequent logic which processes their outputs is here implemented in the commercial FPGA board. Since V_g can be as high as 90 V in the target application, the first condition of (16) is scaled by an attenuation factor α,

$$\alpha v_{Q_3} \leq \alpha k V_g. \tag{18}$$

As for the second inequality in (16), for the same reasons it is also scaled by an attenuation factor β, and level-shifted by a dc term $(1-\beta)V_{bias}$ in order to allow a single-supply implementation of the technique,

$$\beta v_{Q_3} + (1-\beta)V_{bias} \leq (1-\beta)V_{bias}. \tag{19}$$

The implementation scheme of the two modified inequalities of system (7) is shown on Fig. 13. In the implementation, a resistance R^* is also included in positive-feebdack configuration around the comparators, in order to provide a hysteresis window in the transitions and prevent chattering. Notice that, based on (19), only the lower threshold is of interest, hence a large hysteresis window can be employed if needed, without affect the accuracy of the approach.

In a first test, the proposed technique is first disabled, and a 20%-to-45% duty cycle step variation is applied to the converter in order to induce a large-signal transient severe enough to cause Q_3 to temporarily undergo hard turn-off. The transient event is reported in Fig. 14a, which clearly shows the large voltage spike at the drain of Q_3 when the device turns off at positive drain-to-source current. In the measurements, i_{Q_3} is calculated as $i_{Q_3} = i_{L_R} - i'_o$ by separately measuring i_{L_R} and i'_o with current probes.

Next, the proposed technique is enabled, and the same large-signal transient is induced in the converter. Corresponding results, illustrated in Fig. 14b, show how the turn-off of Q_3 at positive current is now completely prevented. As a result, no voltage spike is seen across Q_3. Furthermore, the converter falls back into normal steady-state operation after the transient.

A similar transient measurement is illustrated in Fig. 15a, while Fig. 15b reports the corresponding states of the FSM, acquired from the FPGA with a digital acquisition software. Both Fig. 15a and 15b are triggered and acquired on the same transient event. The figure proves that, in steady-state before and after the transient event, the converter normally rotates between the ON and OFF states, but during the transient the FSM temporarily forces the converter to operate in the IDLE subtopology, as intended.

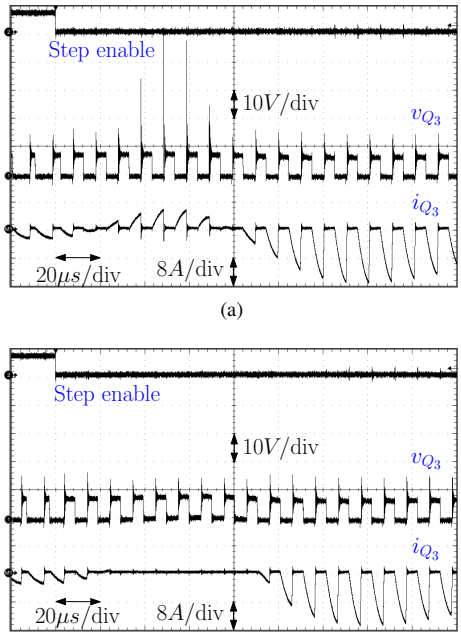


Fig. 14. Transient due to duty cycle step variation $D = 20\% \rightarrow 45\%$. Comparison between experimental waveforms (a) without and (b) with the proposed technique.

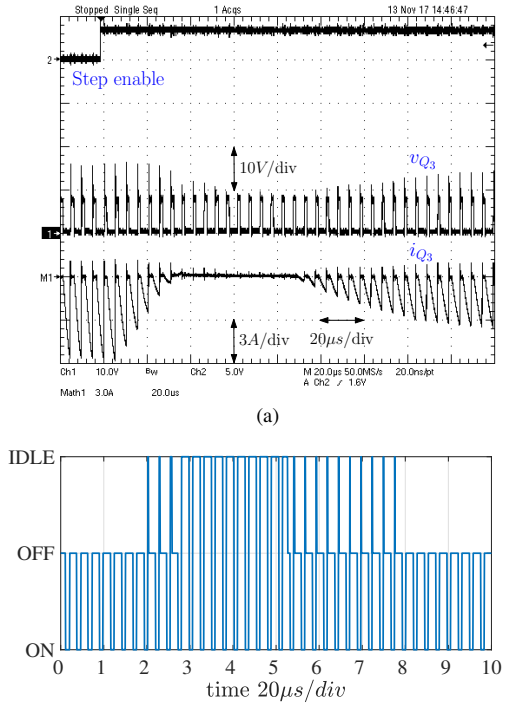


Fig. 15. Transient due to step of duty cycle $D = 20\% \rightarrow 30\%$ with the proposed approach. (a) SCTI waveforms and (b) corresponding states of the FSM.

VI. Conclusion

A control technique is proposed to enable reliable operation of the synchronous SCTI converter for high step-down applications in emerging automotive standards based on the 48 V bus. Voltage spikes occurring in the SCTI topology at the beginning of the off-time during transient events are prevented on a cycle-by-cycle basis via a simple control technique which does not require auxiliary snubbers, voltage clamps or auxiliary windings in the tapped-inductor. The approach is validated experimentally on a 48 V-to-1.5 V, 4 A SCTI converter prototype.

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