A Resonant Switched Capacitor Based 4-to-1 Bus Converter Achieving 2180 W/in^3 Power Density and 98.9% Peak Efficiency

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***Abstract*—Hybrid switched-capacitor (SC) converters are known to have the potential to achieve higher efficiency and higher power density than conventional SC and magnetic-based converters, thanks to the efficient utilization of both active and passive components. By comparing the total switch stress and the minimal passive component volume, the cascaded 2:1 resonant SC topology is found to be excellent for applications with large conversion ratio (e.g. data center power delivery). A 36-60 V input, 4:1 fixed ratio intermediate bus converter is built based on this topology. The prototype achieves 98.9% peak efficiency and up to 2180 W/in^3 power density, both of which are significantly higher than the state-of-the-art.**

I. Introduction

There is increasing demand for high performance power conversion in data centers and telecommunication systems. With the benefit of having high efficiency, good flexibility and reduced cost, the intermediate bus architecture (IBA) has been widely adopted [1]. In contrast to other architectures, the majority of the power conversion in IBA is performed on the motherboard, from 48 V backplane to 12 V bus using a bus converter, and then down to 1 V for CPUs using POL converters [1], [2]. However, the development of high performance IBA converters remains a bottleneck of the overall power delivery system. First, compared with the preceding conversion stages (e.g., 208 V_{ac} to 400 V_{dc} PFC, 400 V_{dc} to 48 V_{dc} LLC), the losses in IBA converters (48:12 V and 12:1 V) dominate the overall system losses [2]. Second, the bulky power converters on the motherboard reduce the usable area for data processing functions. Therefore, it is of great interest to simultaneously improve the efficiency and the power density of IBA converters for these performance-driven applications. As the isolation function can be alternatively provided by the front-end converters, the study of innovative non-isolated topologies for IBA converters shows promise for increased performance.

Recently, hybrid switched-capacitor (SC) converters [3]–[10], which use both capacitors and inductors in the voltage conversion and power transfer process, have received increased attention. In addition to the benefit of traditional SC converters (i.e., efficient utilization of switches, higher energy density of capacitor) [11], the additional inductor in hybrid SC converters can help eliminate the capacitor charge-sharing loss, through an operation called soft-charging [12]–[17]. As a result, without sacrificing the efficiency, the capacitor and inductor values can be selected to achieve a minimal passive component volume, which can be significantly smaller than that of a conventional SC or a magnetic-based converter [18]. With efficient utilization of both active and passive devices, these hybrid converters become good candidates for IBA power conversion where extreme efficiency and power density are critical. In this work, we strive to demonstrate the superiority of hybrid SC converters for IBA applications. After systematically comparing the performance of various hybrid SC converters, a 36-60 V input, 4:1 fixed ratio (unregulated), non-isolated bus converter is designed and implemented using two cascaded 2:1 hybrid SC converters. As shown in Fig. 1, each stage is a basic 2:1 SC converter with an inductor at the output (a structure similar to that of 3-level buck converter). The inductor is selected to resonate with the flying capacitor such that the converter is running in resonant mode (a special case of soft-charging) and zero current switching (ZCS) is achieved. The prototype has a total box volume of 0.275 in^3, and has been tested with up to 40 A output current (600 W at 15 V_{out}), leading to an ultra-high power density of 2180 W/in^3. Furthermore, the prototype's efficiency has a peak of 98.9% and maintains above 98% over a majority of the full load range, which is significantly higher than the state-of-the-art ($\sim$ 96% [2], [19]).

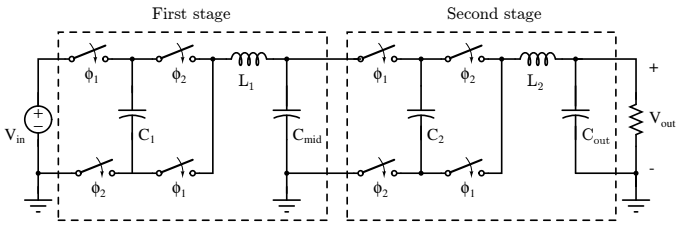

Fig. 1: Schematic drawing of a cascaded resonant converter.

This paper is organized as follows. Section II briefly revisits the analyzing method for comparing various hybrid (resonant) SC converters [20], and introduces the operation principle of the selected cascaded resonant converter. Section III discusses the considerations in hardware design and implementation. Section IV provides the experimental results. Finally, conclusions are made in Section V.

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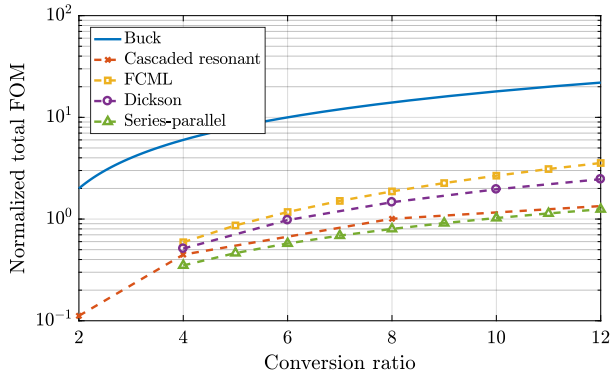


Fig. 2: Normalized FOM for various resonant SC converters. Lower is better.

II. Cascaded Resonant Converter

A. Resonant switched-capacitor topology comparison

In [14], it is shown that many hybrid SC topologies can be obtained by adding a single inductor at the output node of conventional SC converters. Moreover, it is often desirable to operate these hybrid converters at their resonant frequency, as it introduces soft switching and is the critical (minimum) frequency with low-conduction loss.

In order to select the most suitable hybrid resonant switched-capacitor topology for the IBA application, the analyzing method proposed in [20] is used to compare a number of hybrid topologies based on switch stress (reflecting power loss) and the optimized passive component volume (reflecting power density). Then, the overall performance figure of merit (FOM) is obtained by multiplying the normalized switch stress and the normalized passive component volume. It is based on the general trade-off that a converter with smaller switch stress can operate at a higher switching frequency for the same conduction and switching loss, which results in reduction in passive component volume. Therefore, combining both metrics can be indicative of the overall performance potential of the converter.

Here, we calculate the FOM of some commonly-used hybrid resonant topologies ("inductor-at-output" configuration), and the results are plotted in Fig. 2 in log-linear scale (FOM of the buck converter is included for reference). It shows that all of the hybrid converters out-perform the buck converter by a wide margin. In addition, it is interesting to learn that the cascaded resonant converter achieves the second lowest FOM, despite the common perception that cascading converters are not favored as they process the power twice. It should be noted that the weights of the switch stress and the passive component volume in the overall FOM can be adjusted to reflect the characteristics of available technologies, and the final performance for different topologies can be different than what is plotted here. After evaluation of the active and passive components available on the market, a bus converter based on the cascaded resonant topology is selected and constructed.

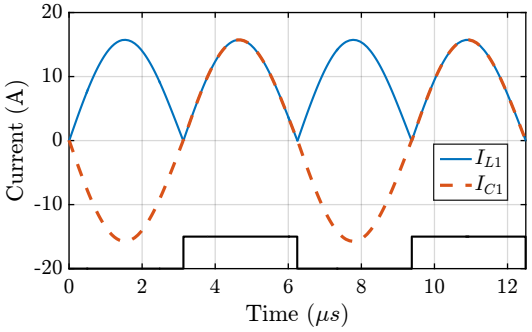


Fig. 3: Simulated inductor/capacitor current at first stage.

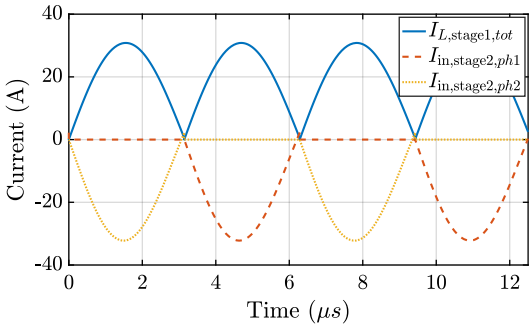


Fig. 4: Minimize C_{mid} with interleaved design.

B. Operation principle

The schematic of the cascaded resonant converter is shown in Fig. 1. It can also be seen as a cascade of two basic 2:1 SC structures followed by an inductor at each output. All switches have a fixed duty ratio of 50%, and every two adjacent switches have a phase shift of 180°. The switching frequency is the resonant frequency of the flying capacitor and the inductor ($f_{\text{sw}} = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{L_2 C_2}}$), as it is the minimum frequency with low conduction loss for soft-charging hybrid SC converters [14]. As shown in Fig. 3, the flying capacitors are resonantly charged in one state and discharged in the other state, resulting in no charge-redistribution loss. Additionally, since the inductor current takes the shape of a rectified sine wave, the current reaches zero at moments of phase transitions and zero current switching (ZCS) is achieved.

However, converters obtained in this way require that $C_{\text{mid}} \gg C_1$ & C_2, so that C_{mid} does not take part in the resonant operation. As a result, the volume of C_{mid} could dominate the size of the capacitors. One way to avoid the penalty is to interleave two phases of the cascaded converters and connect them at the input, middle and output point, and operate them 180° out of phase. As illustrated in Fig. 4, with this interleaving operation, the combined input current of the second stage also becomes a rectified sine wave, which closely matches the inductor current of the first stage. This way, the size of C_{mid} can be significant reduced.

In practical implementations, the flying capacitor value can deviate from the nominal value due to various reasons, and make it difficult to guarantee perfect resonant operation. To

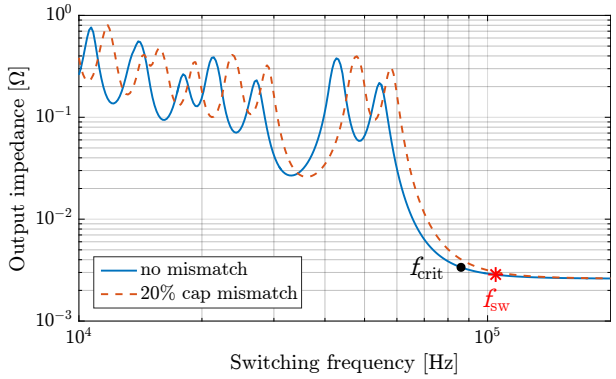


Fig. 5: Output impedance plot for cascaded resonant converter.

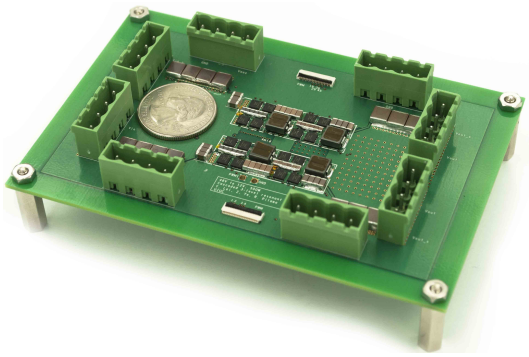


Fig. 6: Hardware prototype (two-phase interleaved). A US quarter is included for perspective.

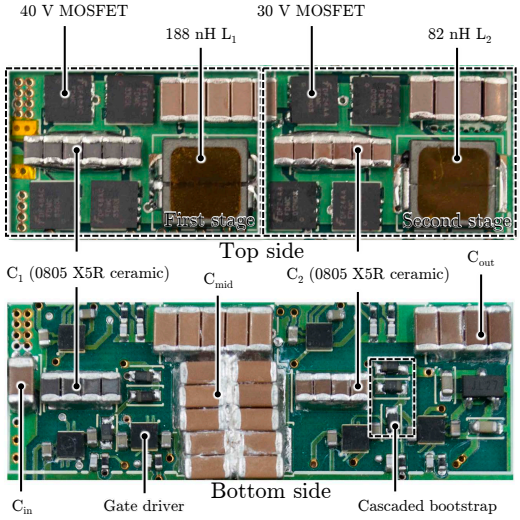


Fig. 7: Annotated photograph of the converter (one phase). Dimensions: 1.38×0.46×0.22 inch (3.5×1.17×0.55 cm).

study its effect on power loss, the output impedance with respect to the tolerance of the flying capacitor is simulated and plotted in Fig. 5. As expected, at the resonant frequency f_{crit}, the output impedance increases if the actual flying capacitors are smaller than their nominal value. On the other hand, when operating in the fast switching limit (FSL) region, the output impedance is flat and insensitive to the capacitor variance, which is a major advantage of the "inductor-at-output" configuration. In comparison, for those hybrid resonant SC converters with inductor in series with the flying capacitor [21], the output impedance increases sharply when the switching frequency is higher than f_{crit}. Therefore it is crucial to use high-precision LC components to ensure perfect resonant operation, otherwise conversion efficiency might be degraded heavily.

In addition to the benefit of good component tolerance, operating the cascaded resonant converter at a switching frequency slightly higher than f_{crit} can also lead to smaller output impedance. This is because the inductor current in FSL operation has smaller RMS value than the sinusoidal current in resonant operation. As will be shown in Section IV, for the high-current IBA application, this reduction of conduction loss might cancel out the increase of switching loss (due to higher switching frequency and imperfect ZCS operation), and lead to a higher overall efficiency.

III. Hardware Design and Implementation

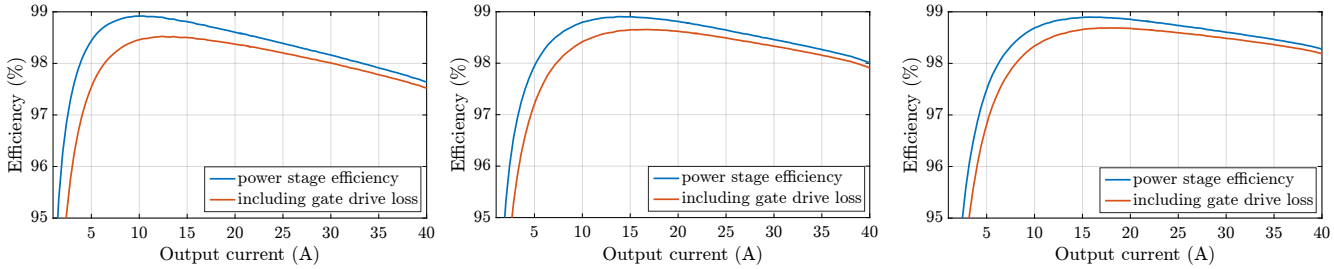
As has been mentioned, the added inductor offers an additional degree of freedom in the design space. The values of capacitors and inductors should be designed to reach a desired resonant frequency, while minimizing the total passive component volume. In general, given fixed output power and switching frequency, it is common to use higher capacitance (and lower inductance) for applications with low voltage and high current [20]. This is based on the fact that capacitor volume depends on the voltage, while inductor volume depends on the current. Besides optimizing the passive component volume, the associated power loss also needs to be considered. Since the resonant operation results in a high RMS current, the ESR of the capacitors and the DCR of the inductors are also important design metrics that can significantly affect the efficiency. Class II ceramic capacitors are found to be good candidates. They have a high energy density that is comparable to electrolytic ones, and have a typical dissipation factor less than 5%. The disadvantage is that their voltage de-rating and temperature characteristics make capacitor matching difficult. However, as discussed in Section II-B, this problem can be mitigated by operating the cascaded resonant converter slightly faster than the resonant frequency.

In terms of switch selection, thanks to the unique structure of the cascaded resonant topology, each switch only needs to block half of the input voltage (30 V for the 1$^{\text{st}}$ stage and 15 V for the 2$^{\text{nd}}$ stage), allowing the use of low voltage MOSFETs (40 V and 25 V). Notice that at this voltage rating, eGaN FETs generally do not outperform silicon MOSFET significantly (lower output capacitance and similar on-resistance) but has a much higher cost [22], [23]. Since the designed resonant frequency is relatively low ($\sim$ 100 kHz), the switching loss is not a dominating factor and MOSFET is a better choice from a cost perspective.

For SC converters, gate drive and level-shifter designs

TABLE I: Main Component Listing of the Cascaded Resonant Converter

Component	Part number	Parameters
1^{st} stage MOSFET	Fairchild FDMC8360L	40 V, 3.1 mΩ
1^{st} stage flying capacitor (C_1)	TDK C2012X5R1V226M125AC	35 V, 22 μF $\times$10
1^{st} stage inductor (L_1)	Coilcraft SLC7530D-500ML	188 nH
1^{st} stage output capacitor (C_{mid})	TDK C3216X5R1H106K160AB	50 V, 10 μF $\times$15
2^{nd} stage MOSFET	Fairchild FDMC012N03	30 V, 1.46 mΩ
2^{nd} stage flying capacitor (C_2)	TDK CGA4J1X5R1C106K125AC	16 V, 10 μF $\times$10
2^{nd} stage inductor (L_2)	Coilcraft SLC7530S-820ML	82 nH
Gate driver	Texas Instruments LM5113	100 V half-bridge
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V Schottky



(a) 36 V to 9 V (f_{sw} = 98 kHz). (b) 48 V to 12 V (f_{sw} = 105 kHz). (c) 60 V to 15 V (f_{sw} = 121 kHz).

Fig. 8: Measured efficiency at various input voltages.

have been a challenge. In this work, the cascaded bootstrap method presented in [24], [25] is used to power the floating gate drivers in an efficient and compact manner. The control signals (open loop, 50% fixed duty ratio square wave) are generated from a TI C2000 microcontroller. For large-scale manufacturing, these signals can be easily generated by a compact and low-cost digital circuit. Since this topology relies on its natural balancing property [26] to maintain the flying capacitor voltage at its desired value, the timing of the control signals (duty ratio, phase shift and gate drive propagation delay) should be carefully matched for all switches [27].

The photograph of the two-phase interleaved hardware prototype (with connectors and additional filter capacitors) is shown in Fig. 6. The PCB is a standard, low-cost 4-layer board. Figure 7 provides a closer look of the converter (one phase) with key components highlighted. The metrics of the LC tanks as well as the other main components can be found from Table I.

IV. Experimental Results

The prototype has been tested with up to 40 A output current with a Yokogawa WT3000 precision power meter. It can output 600 W power in 60-to-15 V conversion, with a very high power density of 2180 W/in^3 or 133 kW/L (as measured by the smallest rectangular box that can contain the converter). We note that the current design has not been optimized, as the commercial off-the-shelf inductors (maximum height of 0.118 inch) are much taller than the other components (maximum height of 0.071 inch). Further optimization of the component selection is therefore expected to increase the power density.

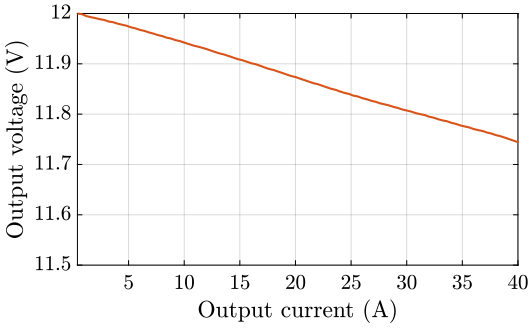


Fig. 9: Load regulation (V_{in} = 48 V, V_{out} = 12 V).

The efficiency performance at various input voltages are measured and plotted in Fig 8. By slightly tuning the switching frequency, the prototype can achieve 98.9% peak power stage efficiency across the entire input range. For the commonly used 48-to-12 V conversion, the overall efficiency (including gate drive loss) has a peak of 98.65%, and maintains 98% at full power. This excellent efficiency performance can also generate two other benefits. First, as shown in Fig. 9, the converter has very tight load regulation. Even though it is in fixed ratio mode (open loop), the output voltage only droops 250 mV (2% V_{in}) at full load. Second, the high efficiency significantly alleviates the cooling requirement, which can be

TABLE II: Comparison of this work and existing non-isolated, unregulated bus converters

Reference	Topology	Output Current (A)	Box Volume (inch^3)	Power Density (W/inch^3)	Efficiency	Notes
this work	cascaded resonant	40	0.275	1745	full load: 98.0%, peak: 98.9%	calculated based on 48:12 V conversion
Linear Technology LTC7820 [28] application design	cascaded pure 2:1 switched-capacitor	40	N/A	up to 1500	full load: $\leq$97.0%, peak: $\leq$98.6%	highly **integrated** 48:12 V design detailed data unavailable (use conservative estimate)
EPC9203 DrGAN demo board [2], [29]	buck	30	inductor volume only: 0.52	less than 692 (based on inductor volume)	full load: 97.3%, peak: 97.8%	48:12 V, **GaN** switches
Vicor [30] NBM3814x46C15A6yzz	sine amplitude	160	1.95	up to 1258	full load: 97.6%, peak: 97.9%	36-46 V input, **3:1** fixed ratio

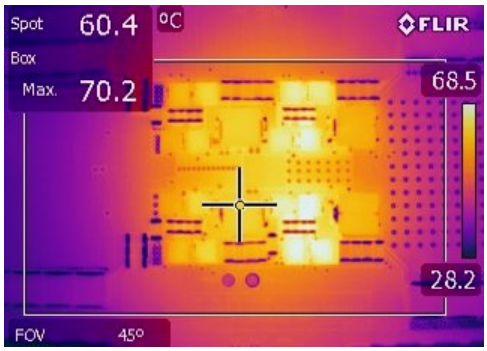


Fig. 10: Thermal performance with no cooling/heatsink (48:12 V, 400 W).

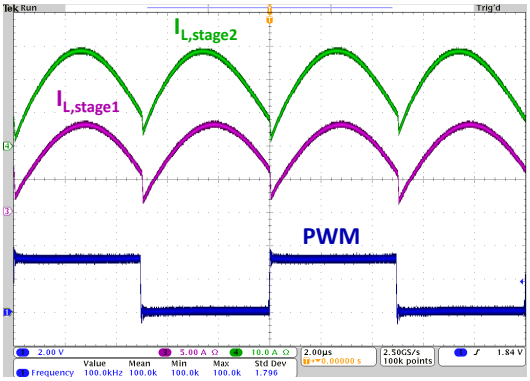


Fig. 12: The inductor currents of the two stages (one phase).

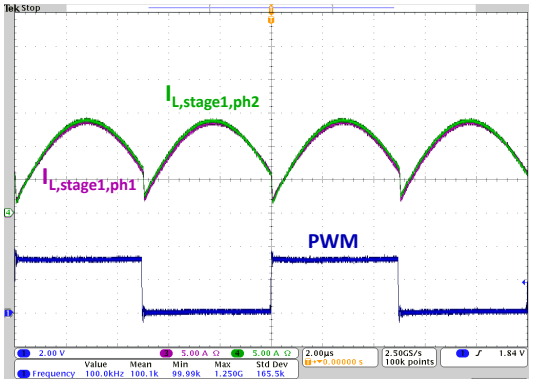


Fig. 11: The interleaved inductor currents at the first stage.

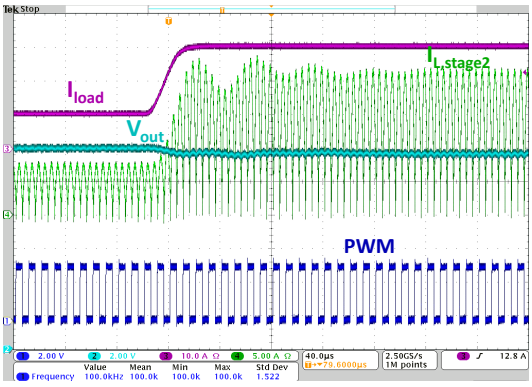


Fig. 13: Transient response of 10 A to 30 A load step.

seen from the temperature rises measured with only natural convection and no heatsink attached, as shown in Fig. 10.

In order to capture the current waveforms and observe the switching operation, wires need to be soldered onto the inductors. We use alternative inductors (with lower inductance) to compensate the extra inductance contributed by the wires, so that the captured waveforms can closely reflect the efficiency measurement scenario (inductors soldered on the board) we have previously. As shown in Fig. 11, the two-phase interleaved inductor currents have good current sharing, and the converter is operating slightly faster than the resonant frequency. The currents at the second stage take a shape similar to that in the first stage (shown in Fig. 12), which can significantly reduce the decoupling requirement of $C_{\mathbf{mid}}$. The prototype is also able to handle large load transients. In Fig. 13, a load step from 10 A to 30 A is introduced. The observed output voltage does not show significant undershoot, and stabilizes within several switching cycles.

Table II compares this work with some of the best existing works. Thanks to the high energy density of capacitors and the efficient utilization of the switches and the passive components, the cascaded resonant converter can have performance superior to that of conventional SC and magnetic-based converters. Compared with the premium, high power Vicor converter [30], this work has a lower power rating, with subsequent challenges associated with auxiliary components such as gate drives and level shifters, which represent a larger portion of the overall volume. Despite these challenges, we

demonstrate that, with a suitable topology and proper design, high efficiency and high power density can still be achieved simultaneously, in such a small form factor.

V. Conclusions

This work demonstrates that both in theory and with hardware prototypes, cascaded resonant converter has excellent performance for applications with large conversion ratio such as data center power delivery. A 36-60 V input, 4:1 fixed ratio bus converter is built, with 98.9% peak efficiency and up to 2180 W/in^3 power density. These results reflect a dramatic improvement over the state-of-the-art products on the market.

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