50-kW 1kV DC Bus Air-Cooled Inverter with 1.7 kV SiC MOSFETs and 3D-Printed Novel Power Module Packaging Structure for Grid Applications

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***Abstract*— The traditional heatsink design technologies for forced air-cooling and power semiconductors with low junction temperatures have constrained the converters to be designed with massive heatsinks. The low power losses of WBG device technology and higher junction temperature operation over a wide operating range of power have not been fully utilized with liquid-cooled systems. The other major limitation has also been the traditional power module packaging "stack" approach with baseplate. This paper presents a novel power stage design which involves 1.7 kV silicon carbide (SiC) MOSFETs, a heatsink design with Genetic Algorithm (GA) and built using 3D printing technology, and a novel integrated modular power module for high power density. The air-cooled module assembly has a SiC MOSFET phase leg module with split high-side and low-side switches and a gate driver with cross-talk and short circuit protection functions. The heatsink design was modeled using a co-simulation environment with finite element analysis software and GA in MATLAB and COMSOL. The proposed concepts were verified and validated through experiments at each stage of development. The power stage was evaluated at 800V, 900 V, and 1kV for 20 kHz switching frequency and 50-kW load. The experimental results show that the CEC efficiency is 98.4 %. In addition to the efficiency, a power density of 75 W/in^3 was also achieved.**

Keywords—Silicon carbide, 3D printing, air-cooling, Genetic Algorithms

I. INTRODUCTION

Air-cooled power converters have had the challenge of low power densities when compared to liquid-cooled power converters. There are several factors that have limited the power density of the converters with forced and convective air cooling. The traditional heatsink design technologies for forced air-cooling, power semiconductors with low junction temperatures, and conventional power module packaging have constrained the converters to be designed with massive heatsinks.

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The traditional method of heatsink design is to utilize finite element analysis (FEA) and iterate on flow patterns and heat dissipation pathways for a heat source. New optimization techniques are continuing to be developed to improve the heat transfer efficiencies [1]. Genetic Algorithms have also been used for optimizing the heatsink to improve the thermal resistance, especially for air cooling [2]. The design space and the selection criteria are finally limited by the manufacturing processes and techniques used to build the heatsink. However, 3D printing technology has brought a new dimension to the world of design and has been proven to be an effective tool to bring the imagination of the designer to reality. Although the 3D printing processes have breathed fresh air into the field of mechanical design, it is currently impaired for mass production by the materials, speed of manufacturing and post processing methods. While the manufacturing experts explore those challenges, the designers have not yet completely understood the benefits of 3D printing technology when compared to the traditional methods. There has been a lack of comprehensive methodology to optimize the heatsink designs with a multi-objective optimization approach.

The potential of silicon carbide (SiC) devices, such as high power density, high frequency, and high temperature operation, have not been fully utilized in liquid-cooled systems with higher thermal conductivity as compared to the air-cooled systems. Because of higher junction temperature operation capability and the reduced losses of SiC device technology over a wide operating power range, a small improvement in the thermal resistance, will have higher impact on power density and reliability of the air-cooled systems. The effect of SiC technology on air-cooled inverters has been demonstrated for solar applications [3]–[6]. However, all of these SiC power modules utilize the conventional power module packages available from vendors. The traditional power module packaging leads to a "stack" approach with substrate integrated to the baseplate and then attached to the heatsink through a thermal interface material. These layers increase the thermal resistance, leading to decrease in thermal efficiency and eventually to an increase in the size of cooling system.

The efficiency and power density targets for the Department of Energy (DOE) Sunshot program are 98% and > 100 W/in^3, respectively for residential and small commercial systems [7]. These targets are difficult to achieve with existing state-of-the art technologies and design approaches. One of the critical components of the inverter is a power stage that includes the DC bus capacitor, the power module and the gate driver technology for each module.

This paper presents a novel power stage design which includes the design and development of a 1.7 kV 100 A rated SiC MOSFET for > 20 kHz operation. A heatsink is designed using a new method of optimization in a co-simulation environment with FEA software and GA, and is manufactured using 3D printing technology. Based on the heatsink, a novel modular phase leg power module with split high-side and low-side switches and a gate driver with cross-talk and short circuit protection functions are developed for the inverter power stage. The design, development, and evaluation of each stage (from bare die to a three phase assembly) is presented in detail.

II. 1.7 KV SiC Device Characterization

In order to achieve the power density target, the DC bus voltage is chosen to be at least 1000 V. There are a few choices in WBG devices for this voltage and current rating that are suitable for a 480 V, 50 kW grid tied operation. The semiconductor devices used in the inverter design are 1700 V bare die samples of SiC MOSFETs and SiC Schottky diodes. The current ratings of single SiC MOSFET and SiC Schottky diode bare die are around 34 A and 50 A, respectively. These are experimental devices that were obtained from the manufacturer with limited device performance data. The static and dynamic characteristics of the bare dies were evaluated for a comprehensive power module and thermal design.

The temperature-dependent output characteristics of single SiC MOSFET bare die with a gate voltage of 20 V are shown in Fig. 1. With this gate voltage, the on-resistance $R_{ds,on}$ is mainly dominated by the drift region resistance, and thus a positive temperature coefficient of output characteristic is presented. The positive temperature coefficient of on-resistance is beneficial for current balancing of multi-chip modules. At a junction temperature of 125°C, the on-resistance value is 175 mΩ.

The anti-parallel SiC Schottky diodes are also characterized. The output characteristics of single diode bare die at different junction temperatures up to 175°C are shown in Fig. 2. As junction temperature increases, the threshold voltage decreases while the resistance increases. With a current level higher than 5 A, a positive temperature coefficient of resistance is observed, and the anti-parallel diodes are suitable for parallel operation.

The switching behavior of the SiC MOSFET bare die is also characterized using the double pulse test method. The temperature dependent turn-on and turn-off transient performance of the selected bare die are initially evaluated with a 600 V DC bus voltage, and then extrapolated to 1000V for switching loss estimation. Within the plotted current and temperature range, turn-on energy decreases with temperature while turn-off energy increases with temperature, resulting in an almost constant total switching energy loss. The total switching energy loss under different temperature and current levels is shown in Fig. 3. The temperature-insensitive feature would be beneficial for thermal stability under high power and high temperature operation.

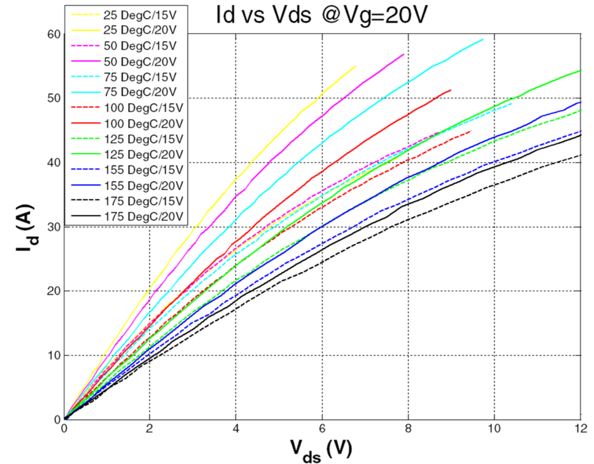

Fig. 1. 1700 V SiC MOSFET output characteristics.

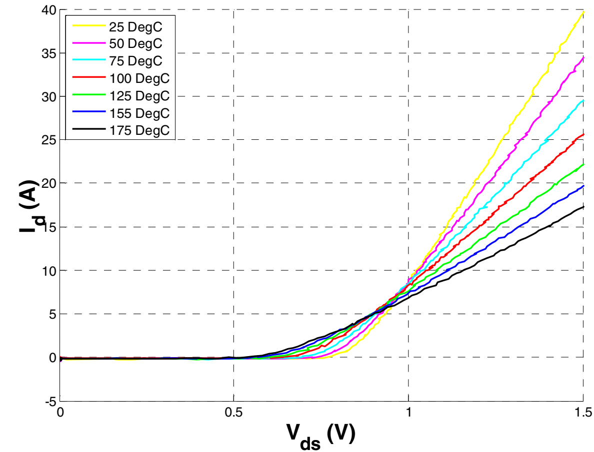

Fig. 2. 1700 V SiC diode forward characteristics.

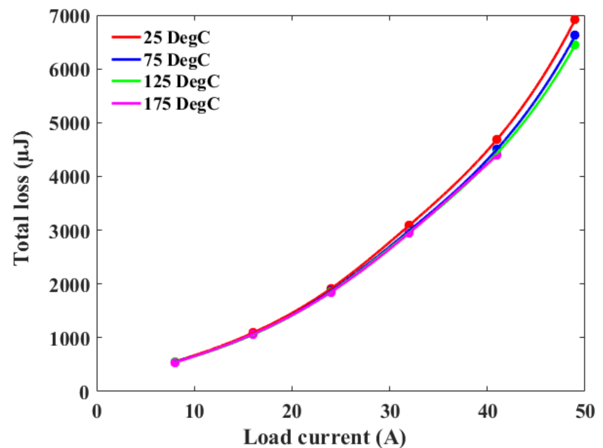

Fig. 3. Total switching energy of single SiC MOSFET bare die.

III. Power Loss Calculation and Thermal Design for the 1.7 kV Module

The power loss of the three phase inverter can be estimated based on the device characterization results and predefined rated operating condition which is summarized in Table 1.

Table 1. Design specification for the inverter.

Parameters	Value
Total power rating, P	50 kW
DC bus voltage, V_{DC}	1 kV
Power factor (grid side), $cos\theta$	1.0
Line-to-line voltage RMS, $V_{ll(rms)}$	480 V
Switching frequency, f_{sw}	20 kHz
Operating junction temperature, T_j	~125°C

The RMS and amplitude of the current for each phase can be calculated as:

$$I_{ll(rms)} = \frac{P}{\sqrt{3}\cdot V_{ll(rms)}\cdot \cos\theta} = 60.14\ A \quad (1)$$

$$I_{peak} = I_{ll(rms)} \cdot \sqrt{2} = 85.08\ A\ . \quad (2)$$

The switch current rating can be selected based on the phase current amplitude. In order to carry the desired current with a safety margin, five MOSFETs and three diodes are paralleled for one high-side/low-side switch position and placed in one Direct Bonded Copper (DBC) substrate, as shown in Fig. 4.

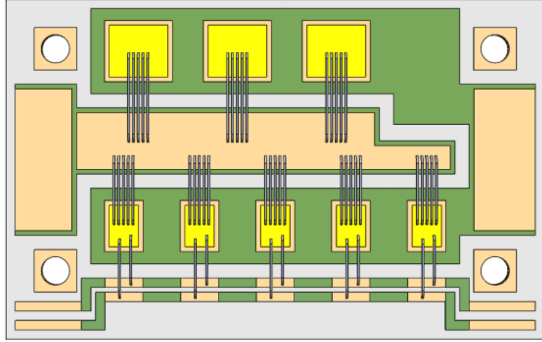

Fig. 4. Module substrate layout of one switch position.

A. Power Loss Calculation

Both the estimated switching loss and conduction loss of a switch position can be derived according to the measured device characterization results in the previous section.

For the SiC MOSFET-based three-phase inverter, the conduction loss calculation is similar to that of conventional IGBT-based inverter. However, unlike IGBTs without reverse current conduction capability, SiC MOSFETs are able to share reverse current with their anti-parallel SiC diodes, making the conduction loss calculation complicated. Given that the on-state voltage drop of five paralleled SiC MOSFET is generally much lower than the anti-parallel diode voltage drop, the reverse current is assumed to thoroughly flow through SiC MOSFETs. This assumption can provide more thermal margin to SiC MOSFET as more current stress is used for loss calculation.

The forward current I_{rms_P} and reverse current I_{rms_N} are given by

$$I_{rms_P} = \sqrt{2}\cdot I_{ll(rms)}\cdot\sqrt{\frac{1}{8}+\frac{m_a\cdot cos\theta}{3\pi}} = 40.42\ A \quad (3)$$

$$I_{rms_N} = \sqrt{2}\cdot I_{ll(rms)}\cdot\sqrt{\frac{1}{8}-\frac{m_a\cdot cos\theta}{3\pi}} = 13.23\ A\ . \quad (4)$$

According to the output characteristic, the on-state resistance of five parallel SiC MOSFETs at 125°C is ~35 mΩ, and thus the conduction loss of one switch position is

$$P_{cond} = I_{rms_P}^2\cdot R_{ds(on)} + I_{rms_N}^2\cdot R_{ds(on)} = 63.3\ W. \quad (5)$$

The switching loss can be calculated based on the dynamic double pulse test data. Since each switch only presents switching loss during forward half current fundamental cycle, the average value of the half fundamental current shall be used for switching loss calculation. The average current of each bare die SiC MOSFET for switching loss calculation is given as

$$I_{avg_die} = \frac{I_{peak}}{\pi} / 5 = 5.3\ A\ . \quad (6)$$

As the switching energy loss data is obtained at 600 V DC bus voltage, a linear scaling up to 1000 V should be conducted for loss evaluation. The switching energy loss of each bare die SiC MOSFET is estimated based on the loss value at the test condition of 600 V and 8 A, i.e.

$$E_{sw_die} = \frac{I_{avg_die}\cdot V_{dc}}{I_{test}\cdot V_{test}}\cdot E_{sw_die_test} = 596\ \mu J\ . \quad (7)$$

The switching loss of a switch position with 5 MOSFETs operating at 20kHz switching frequency is calculated as

$$P_{sw} = E_{sw_die}\cdot f_{sw}\cdot 5 = 59.6\ W\ . \quad (8)$$

By summing up the above conduction and switching loss, the total loss in one switch position is 123 W. This loss value was used as the heat source for thermal design.

B. Thermal Design

The heatsinks were optimized using GA, a machine learning algorithm that imitates the natural evolution process proposed in the Darwinian evolutionary theory. While using GA, coded in MATLAB, to generate design chromosomes of heatsink, FEA simulations are used to evaluate the fitness value of each. For automation purposes, FEA simulation commands executed in COMSOL are directly invoked from the algorithms implemented in MATLAB. As shown in Fig. 5, the automated interface between the optimization algorithm and the evaluation tool is created. All possible heatsink candidates are parameterized in MATLAB as a series of codes, like DNA of a living creature. To decode the design, genetic expression is performed by sending construction commands to COMSOL based on design instruction of chromosomes. In the meantime, predesigned components such as semiconductor devices are directly imported from SOLIDWORKS automatically. The fitness evaluation is then carried out in COMSOL with the simulation setting command delivered from MATLAB. Upon the completion of FEA, the target performance, for example, the junction temperature of the module is obtained and automatically sent back to GA in

MATLAB. Then, fitness value is assigned to the individual. After evaluating the whole population, individuals with higher fitness values will be provided better chances to pass their chromosomes to the offspring. The population of next iteration is then generated by crossover, mutating, and recombining selected chromosomes, and the GA repeats the similar process until optimized result is approached.

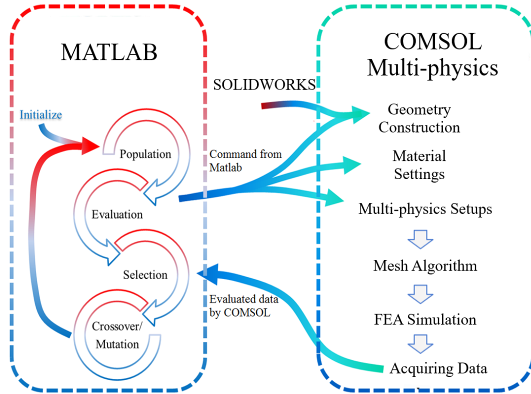

Fig. 5. Automated co-simulation environment concept.

Following this optimization method, a heatsink model generated for this inverter is shown in Fig. 6. The detailed design and analysis of the heatsink has been previously presented in [8]. Because of the complexity of the heatsink design generated, traditional manufacturing methods could not be used and 3D printing manufacturing technology was chosen for this design. This was a learning exercise for the optimization algorithm to further add the traditional manufacturing design constraints and generate designs that can be manufactured with traditional techniques as well.

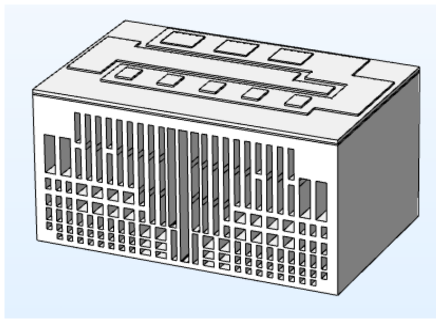

Fig. 6. Heatsink mode generated with GA optimization.

IV. 1.7 KV, 100 A Power Module Design and Evaluation

A. Power Module Package Design

The proposed air-cooled module with novel packaging structure is shown in Fig. 7, where P, N, and O denote the positive, negative, and output terminal of the phase leg module configuration respectively. The main objective of this novel structure is to increase the overall heat dissipation area by splitting the phase leg module into two submodules, i.e. a high-side switch module and a low-side switch module which are attached to two separate heatsinks. This module design is an improvement of the previous design of a 3D-printed air-cooled module described in [9]. Each submodule consists of a DBC substrate attached to the flow channel via thermal interface material. The aluminum flow channel is electrically insulated from the positive and negative DC bus by the aluminum nitride substrate. The high voltage DC bus interconnects the power module from the left side of air flow channel while the gate driver and control interfaces on the right side. In addition, a decoupling circuit board, adjacent to the DC buses, is designed to minimize the power loop parasitic inductances and improve switching performance.

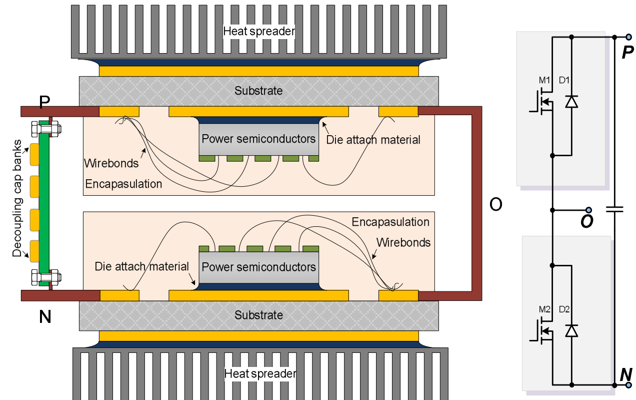

Fig. 7. Proposed packaging structure.

To relieve the mechanical stress that may damage the ceramic of the DBCs, the positions of the mounting holes are carefully designed. Moreover, the five MOSFETs are separated far enough to suppress the cross coupling of heat dissipation, thus reducing horizontal thermal resistance. By bending both gate and source strips closer to the MOSFETs, the distance is reduced to ease the bonding process. Sufficient isolation distance is planned to prevent potential high voltage breakdown issues.

B. Double Pulse Test

Before the fabricated module was assembled, each power module was evaluated at full 1000 V DC bus voltage and maximum current for full inverter operation. The double pulse test setup is shown in Fig. 8, and the experimental waveforms for turn-on and turn-off switching transient at 1000 V are shown in Fig. 9.

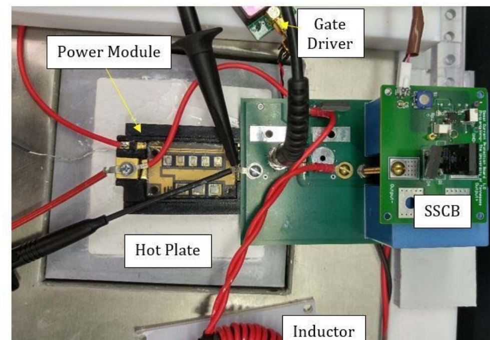

Fig. 8. Experimental setup for double pulse test of the developed module.

The total switching losses for the module were calculated from the test data, as shown in Fig. 10. The total energy loss is

~2900 μJ for 26.5 A switching which results in ~58 W switching loss at 20 kHz operation. The switching energy loss for the module is very close to the value estimated using the single die test data presented in section III. This clearly validated the voltage scaling of the single device data.

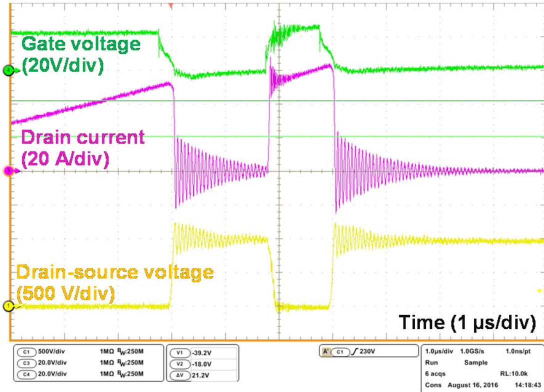

Fig. 9. Double pulse test waveform of the power module at 1 kV DC voltage.

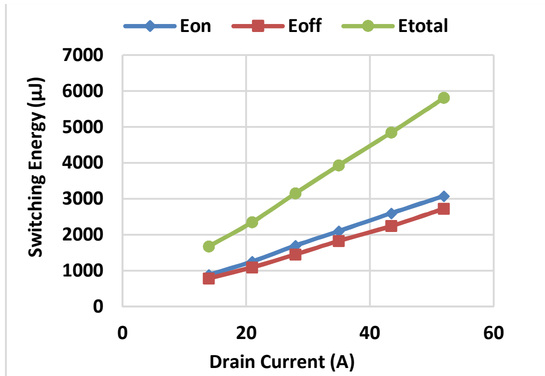

Fig. 10. Total switching energy of the power module at 1000V.

C. Buck Operation Evaluation

The fabricated power block assembly used for single phase continuous operation test is shown in Fig. 11, where only the low-side switch of the phase leg module is shown. The high-side switch has exactly the same structure, which is reversely stacked on top of low-side switch. The single phase assembly with the fan is shown in Fig. 12. The volume of this single phase power block is ~20 in^3 and the total combined volume of the power stage for the three phase inverter is ~60 in^3.

Fig. 11. Power module assembly.

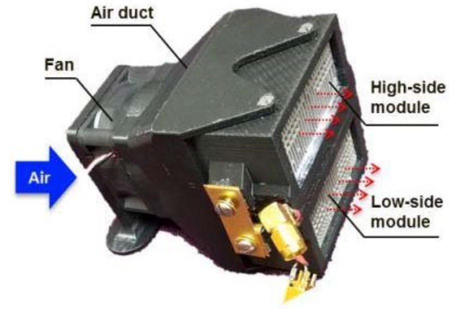

Fig. 12. Single phase block assembly of the power stage.

Before building the three phase power stage, a buck converter setup was built to evaluate the continuous power operation performance. The low-side SiC MOSFETs are reverse biased to serve as free-wheeling diodes, and the pure inductive load is replaced by a RLC load. The LC filter is composed of an inductor of 0.2 mH and a capacitor of 100 μF with an equivalent resistive load of around 10 Ω. The buck converter is operated at a 1 kV input DC bus voltage and 40% duty-cycle.

The phase leg power block is mounted within a 3D-printed plastic housing with two air ducts (one for high-side switch, one for low-side switch) for even air flow sharing and reduced air pressure loss. The gate driver boards are mounted on the front-side of the housing, with PWM signal (generated by a Digital Signal Processing board) input from the left side. The overcurrent protection component, i.e. solid state circuit breaker (SSCB), and DC link capacitors are mounted on back-side of the housing. A separate fan is also used to prevent the potential thermal runaway of the SSCB induced by its conduction power loss. In addition, two thermocouples are utilized to monitor the heatsink inlet and outlet temperature values. Fig. 13 illustrates the continuous operating waveforms and measurement results with 1 kV DC bus voltage and 20 kHz switching frequency. As can be observed, for 40% duty cycle, the inductor current is around 40A, and the ripple current is fairly high (~20 A) due to relatively low switching frequency and reduced filtering inductance at high DC current bias. According to the measurement results from the power analyzer, the input power is 15.59 kW, and the output power is 15.24 kW. The overall efficiency of the buck converter at 20 kHz is 97.76%. The continuous power test lasted for five to ten minutes to reach the thermal steady state, and then the inlet and outlet air temperatures were measured.

The thermal performance of the designed power module was evaluated through FEA-based thermal simulation, and then compared with the continuous experimental results. The following set of experimental data were utilized for loss calculation and thermal simulation purposes: 1000 V input voltage, 12.08 A input current, 11250 W input power, 371.6 V output voltage, 29.65 A output current, 10991 W output power, 97.71% efficiency, 40% duty cycle, 20 kHz switching frequency, 28.8°C inlet temperature with high-side MOSFETs outlet temperature of 74.8°C and low-side diodes outlet temperature of 40.2°C. It should be noted that the efficiency of the power block (without the filter stage) was measured to be ~98.8 % at 20 kHz switching frequency.

Based on the double pulse test results, both the static and dynamic characteristics for a single MOSFET and single diode have been obtained at 125°C case temperature. Specifically, the on-resistance and total switching loss of a single MOSFET are 174.36 mΩ and 540 µJ (at 600 V, 8 A), respectively. The forward voltage drop and equivalent on-resistance for a single diode are 0.7 V and 34 mΩ, respectively. According to the information above, the power loss for the buck converter can be roughly estimated. The detailed calculation procedure is omitted here due to space limit. The total switching and conduction losses of the high-side MOSFETs are 220 W and 12.8 W, respectively. The total losses of the low-side free-wheeling diodes are 22.8 W. The total calculated loss of the buck converter is 255.6 W, close to the power loss in the experiment (258 W).

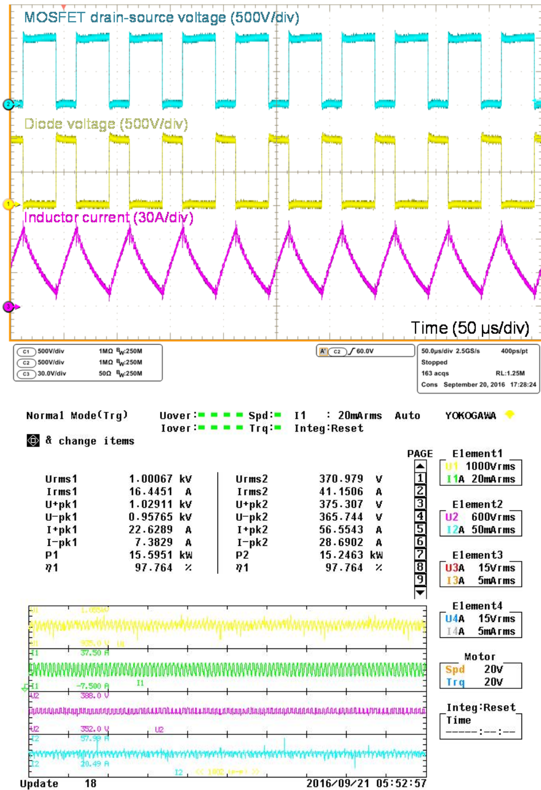

Fig. 13. 1 kV, 20 kHz Buck operation: experimental waveforms (top) and measured results from power analyzer (bottom).

With the above loss information and the manufacturer provided operating curve of the selected fan, the temperature distribution of the module was simulated in COMSOL. Fig. 14 shows the temperature of the outlet air and the heatsink outlet surface temperature. The temperatures of the testing points (the location of the thermocouple in the experiment) in the simulation are around 75°C on MOSFET and 38°C on diode, which match well with measured data of MOSFET 74.8°C and diode 40.2°C. Based on the validity of the thermal simulation, the real junction temperatures can be estimated from simulation results. In simulation, a 100 µm thermal grease with a thermal conductivity of 0.8 W / (m·K) is also assumed to emulate the real case more accurately. The temperature map of junction positions indicates that maximum MOSFET junction temperature is about 131.5 °C and maximum diode junction temperature is around 70.5 °C.

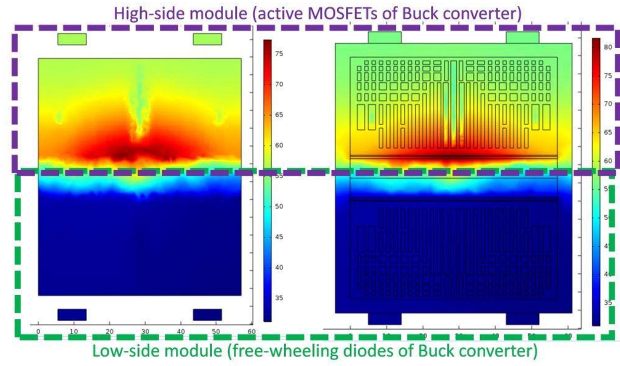

Fig. 14. Thermal simulation results: outlet air temperature (left) and surface temperature of heatsink outlet (right).

V. THREE PHASE INVERTER DESIGN AND EVALUATION

The power stage of the three phase inverter mainly includes the air-cooled power blocks, fans, DC-link capacitors, DC bus bars, and gate drivers. The 3D mechanical layout of the three phase inverter is shown in Fig. 15. The actual hardware prototype of the three phase inverter is shown in Fig. 16, with an overall volume of ~671 in^3. The power density for a 50-kW operation is 75 W/in^3. This is more than ~3.5 times improvement when compared to a commercial solar inverter power stage with a power density of 20 W/in^3. The commercial power stage density was calculated in the lab by opening up a commercial unit.

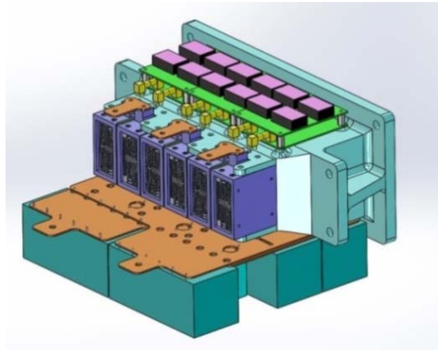

Fig. 15. 3D mechanical layout of the developed 50 kW three phase inverter.

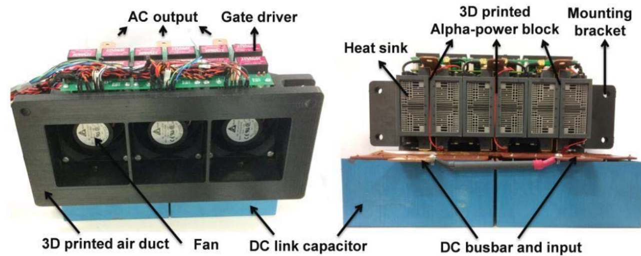

Fig. 16. Hardware prototype of power block based 50kW three phase inverter: front view (left) and back view (right).

The inverter is tested in an open-loop configuration, i.e. PWM signal is generated from a digital signal processor

(DSP) with a preset modulation index. The input power is provided by a DC power supply. The performance of the inverter is evaluated at three input voltage levels, i.e. 800V, 900V, and 1000V. In order to emulate a 480 V grid voltage, the inverter line-to-line output fundamental voltage is maintained at 480 V RMS by adjusting the modulation index at different DC bus voltage levels. The inverter was tested with an inductive load, consisting of an inductor of 0.9 mH and a step-change resistive load for different output active power up to 50 kW.

The overall test setup layout for the three phase inverter operation is shown in Fig. 17. Fig. 18 illustrates three-phase AC current when the three-phase inverter operates at 1 kV DC bus voltage and ~ 48 kW output power. The inverter AC output current is close to pure sinusoidal wave, with some switching ripples and minor distortion at zero-crossing point. The switching ripple can be better suppressed with higher filtering inductance and/or higher order harmonic filters in the future grid tied operation. Based on the power analyzer measurement results, the inverter output AC current (I_{rms2}) is around 60 A RMS with a total harmonic distortion of ~2.5%. The inverter line-to-line fundamental RMS voltage is around 460 V (U_{rms4}). However, the overall inverter line-to-line RMS voltage (U_{rms2}) is much higher than the fundamental value because of the high switching ripple and its side-band harmonics. That is why the inverter output apparent power (SΣA) is much larger than its active power (PΣA). The inverter input and output active power are 48.15 kW and 47. 28 kW respectively, resulting in an efficiency of ~98.2%.

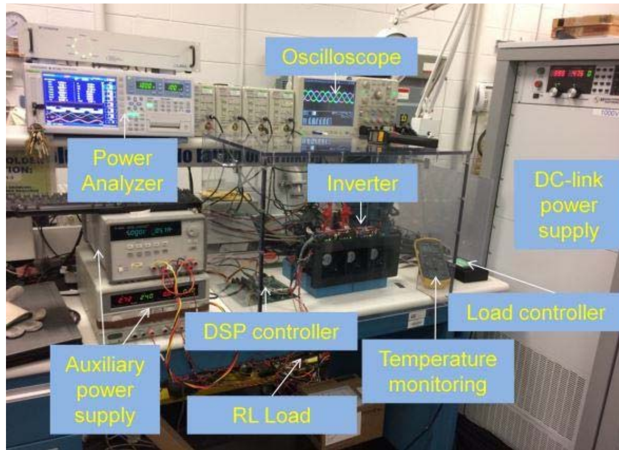

Fig. 17. Test setup for power block based three phase inverter operation.

The California Energy Commission (CEC) defined efficiency is also obtained for the purpose of rating and comparing efficiencies with other inverters [10]. According to the CEC inverter test protocol, in this test 18 inverter efficiency numbers are measured at six power levels (10%, 20%, 30%, 50%, 75%, and 100% of rated output AC power) and at three predefined DC voltage levels (V_{min} = 800 V, V_{nom} = 900 V, and V_{max} = 1000 V), as shown in Fig. 19. Then, the CEC efficiency is calculated as a weighted average efficiency of these 18 values, with the following DC voltage independent weighting factors for the six power levels: 10% ~ 0.04, 20% ~ 0.05, 30% ~ 0.12, 50% ~ 0.21, 75% ~ 0.53, 100% ~ 0.05. The calculated CEC efficiency is 98.42% for the developed inverter.

In addition to the power block and inverter test, the gate driver is also tested for overcurrent protection and noise immunity. Originally, the overcurrent protection threshold was set at around 70 A (peak), and it was successfully triggered at the preset threshold when the output AC current is increased to 40 A (RMS). The large current ripple due to small filtering inductance also contributed to reach the threshold. In order to further push the output AC current and power, the overcurrent protection threshold was increased to around 200 A (peak). The protection is not triggered when the output AC current is 60 A (RMS). During the whole debugging process, there is no electromagnetic noise induced false triggering either. The short circuit protection response time is around 2 µs.

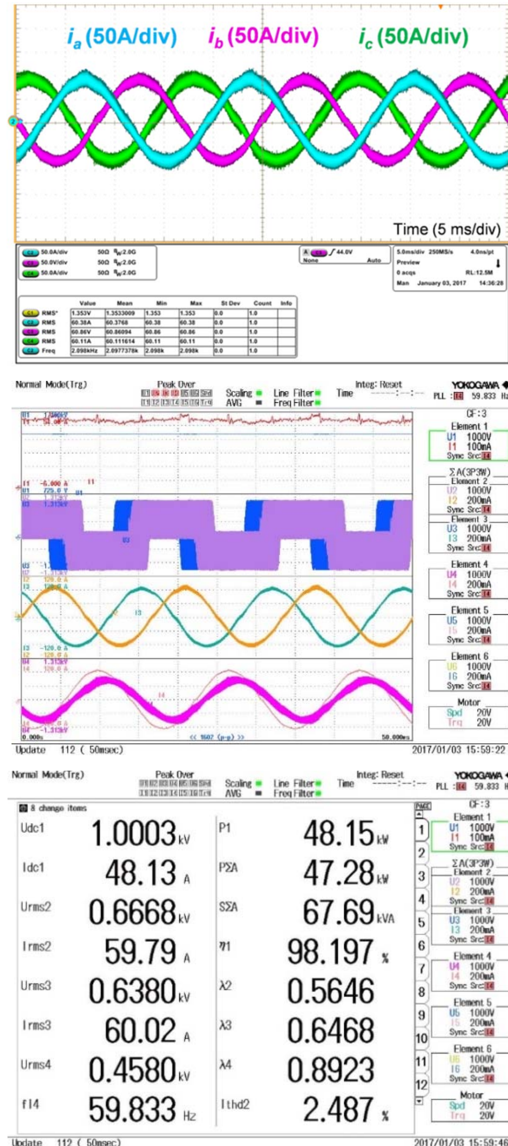

Fig. 18. Three-phase AC current (top), power analyzer waveforms (middle), and measurement data (bottom) of the three-phase inverter operating at 1 kV DC bus voltage and ~48 kW output power.

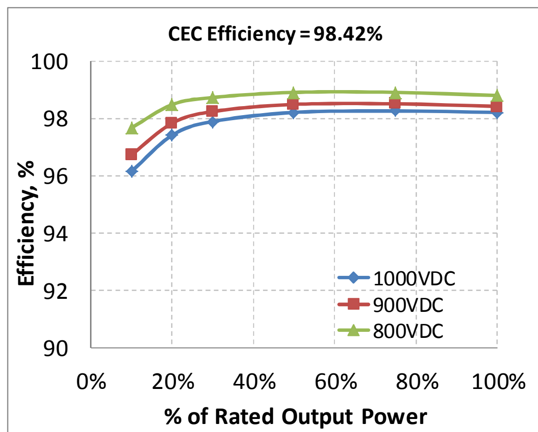

Fig. 19. CEC efficiency of the inverter.

An FEA simulation model is built in COMSOL to validate the thermal results obtained and to estimate the junction temperature of power semiconductors. The simulation is performed to obtain two different parameters: the average flow rate for each power module and the estimated junction temperature. Based on the experimental loss data, the simulated temperature profile of the power module under rated operation is shown in Fig. 20. The maximum junction temperature of the bare semiconductor die (MOSFET) is 103°C, and the temperature variation among the MOSFETs is within 10%. The temperature was measured from the simulation results in COMSOL. The MOSFET was used for validation as it has more losses than the diodes and much higher junction temperature.

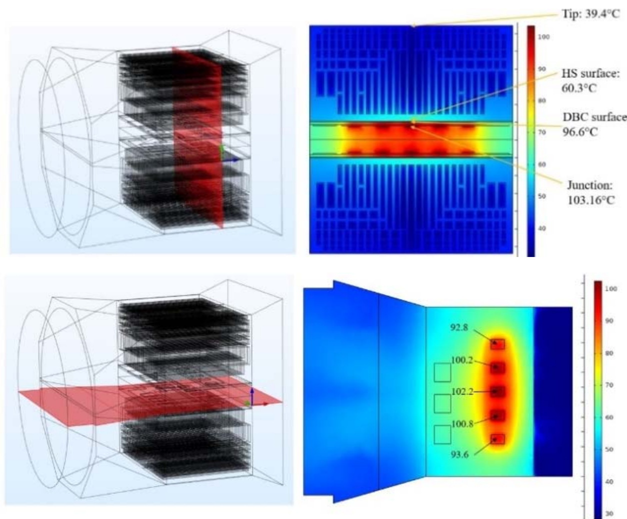

Fig. 20. Thermal profile plot of vertical (top) and horizontal cut plane (bottom).

VI. Conclusions

The work presented in this paper showed that the power density of the air-cooled power converters can be increased significantly when compared to the state-of-the-art systems. This was achieved by combining novel technologies like 3D printing and SiC devices and utlizing a new co-simulation environment using GA optimization and FEA software. A new packaging concept was used to develop a 1.7 kV SiC MOSFET module running 100 A at > 20 kHz operation. A systematic approach of designing an inverter power stage from a bare die to the three phase asemebly was also preseented in detail. A power stage design with an overall volume of ~671 in^3 and a CEC efficiency of 98.42 % at 1 kV and 50 kW operating conditions was demonstrated. Finally, the thermal performance of the inverter was also evaluated, and based on thermal simulation results the maximum junction temperature of the bare semiconductor dies is 103°C, and the temperature variation among the MOSFETs is within 10%.

Acknowledgment

This research was sponsored by the SunShot National Laboratory Multiyear Partnership (SuNLaMP) program, DOE Solar Energy Technologies Office (SETO), under a contract with UT Battelle, LLC.

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