A 10 kV DC Transformer (DCX) Based on Current Fed SRC and 15 kV SiC MOSFETs

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***Abstract*— In this paper, a two level 10 kV DC transformer (DCX) based on 15 kV SiC MOSFETs is presented for medium voltage application. Current fed series resonant converter is proposed as the main circuit for two purposes: 1) realize ZVS on MV MOSFETs and ZCS on LV MOSFETs across entire load range. 2) minimize total required system capacitance, allowing film capacitors to replace electrolytic capacitors for longer lifetime performance. 15 kV device is utilized to reach its full voltage, frequency and power potential of 10 kV, 100 kHz and 30 kW, respectively. Inherent cycle by cycle over load current limiting capability is achieved by paralleling diodes on LV resonant capacitors. The operation principle under normal load and short circuit conditions, as well as ZVS design are provided in this paper. An all film capacitor 20 kW DC-DC prototype that converts 10 kV to 340 V is built to verify the theoretical analysis, which achieves operation frequency of 37 kHz and peak efficiency over 98%. 10 kV constant operation is the highest reported voltage for a two-level structure based converter without devices in series. Short circuit is conducted at 3 kV with a peak current limited within 11 A, with expect peak current within in 35 A at 10 kV short circuit condition.**

Keywords—Two level; CFSRC; SiC MOSFET; ZVS; medium voltage; current limiting; DCX; capacitance reduction

I. INTRODUCTION

In recent years, the isolated medium voltage (MV, 1 kV – 35 kV) DC transformer (DCX) has drawn increasing interest in applications such as ship power, data center and solid state transformer (SST) [1]- [6]. MV DCX plays a crucial role to connect different load or energy system and offers galvanic isolation, voltage regulation and fault current limitation. There is a strong desire for a high efficiency, high reliability and high power density MV DC transformer (DCX). Current researches mainly focus on topology, semiconductor device and control design.

Zero voltage switching (ZVS) is the key to achieve high switching frequency. Hard switching in MV applications will significantly limit the switching frequency due to the energy loss from device's output charge [7].

Many researches have been done to introduce circuits with ZVS capability into MV DC applications. Dual active bridge (DAB) circuit is a popular solution with good ZVS capability and controllability [8]. However, this circuit has drawbacks of limited ZVS range and high turn off current, both of which limit its efficiency performance [8]. Additional auxiliary circuit or complex control scheme can be used to extend the ZVS range in DAB, but is not practical in MV applications [9],[10].

LLC type of series resonant converter (SRC) is attractive for its ZVS capability across the entire load range [11], [12]. Conventional SRC circuit shown in Fig. 1 is based on voltage fed structure, within which capacitors are placed on input and output sides to carry ripple currents. Large capacitance is normally required, especially in high power applications such as the low voltage (LV) side of MV DC systems. In MV applications, these capacitors' size and weight are dramatically increased due to the high voltage insulation requirement, which will affect the system power density. Electrolytic capacitors are normally adopted for power density consideration for its much higher energy density than film capacitors. However, electrolytic capacitors normally have limited lifetime (less than 10 years), which significantly limit the DCX's lifetime performance. On the other side, film capacitors offer much longer lifetime (over 20 years) and 2 times higher ripple current density.

Reducing the required system capacitance enables an all film capacitor MV DCX, which helps improve system lifetime performance and power density.

Many research groups have developed methods to reduce the required capacitance in DC systems. Paper [11] introduce a ripple eliminator circuit to replace bulky DC capacitors. Ripple current is transferred into auxiliary capacitor during operation. However, this method requires additional switches, passive components and control circuits, which is not practical in MV applications. Other works tried to combine SRC circuit with LC output filter to reduce capacitance, but all of them affect the ZVS performance of SRC [16], [17].

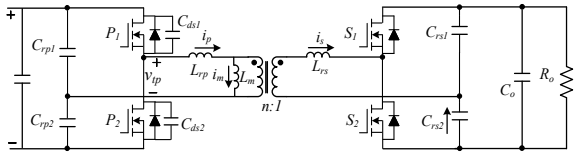


Fig. 1. Half bridge voltage-fed SRC topology

Based on the input current fed (ICF) cell concept proposed in paper [18], current fed SRC (CFSRC) shown in Fig. 2 is proposed in [19] for direct AC-AC applications. This topology can not only help to achieve ZVS across entire load range, but also helps minimize system total capacitance.

The 15 kV SiC MOSFETs developed by Wolfspeed are very promising device which have been increasingly

investigated in numerous MV applications [8], [11]. They can enable simple and robust two-level MV DCX where the peak voltage stress is less than 12 kV. High switching frequency is also achievable due to the fast switching capability of the device. With two level configuration, the system complexity and control scheme will be much simplified. Therefore, the system reliability will be improved, and higher efficiency can be achieved.

Some preliminary works including double pulse test, R_{on} and thermal tests were carried out to characterize the 15 kV SiC MOSFETs thoroughly [11], [13]. The voltage blocking capability of this device has been verified up to 12 kV. However, only few research groups have implemented this device into continuous operation. So far, highest achieved continuous operation voltage and frequency of this device in DC-DC converter is 6 kV, 40 kHz, respectively [11].

Current limiting capability is also a very desired functionality in MV applications. Several current limiting methods for SRCs have been previously proposed in the literatures [21], [22]. One approach is to increase frequency to increase the impedance of the circuit. Thus, limit the current during overload condition. However, this method is not applicable in MV applications since increasing frequency will contribute to risk of hard switching and higher conduction loss. Reference [22] discusses a very effective method by paralleling diodes on resonant capacitors to limit current during overload conditions. This method is attractive because cycle by cycle current limiting can be realized.

This paper proposes a 10 kV two level MV DCX based on 15 kV SiC MOSFETs. Half bridge CFSRC topology shown in Fig. 2 is adopted to achieve ZVS operation over entire load range, minimizing MV MF devices and required system capacitance. Therefore, the whole system can be very compact, cost effective and high efficiency.

Fig. 2 provides the detail system configuration. Resonant capacitors are split into two pairs of twin capacitors and distributed symmetrically on MV and LV sides, which helps minimize total MV MF MOSFETs number to two. Two diodes, D_1 and D_2, are paralleled on LV resonant capacitors for over current protection. Resonant capacitors, C_{rp1} and C_{rp2}, are designed intentionally larger than C_{rs1} and C_{rs2} for two purposes: (1) to achieve higher resonant tank impedance during overload condition to limit the circuit current and (2) decrease the ripple voltage on C_{rp1} and C_{rp2} to decrease the voltage stress on MV devices, P_1 and P_2.

This paper is devoted to the detailed design, analysis, and implementation of the proposed MV DCX under normal load and short circuit conditions at 10 kV voltage level.

II. Normal Load Operation Principle

Under normal operation, the ripple voltage on the secondary resonant capacitors will not exceed the output voltage, and the clamping diodes do not work. The detailed operation waveforms of the proposed circuit at resonant frequency are shown in Fig. 3.

There are two operation modes during half switching cycle.

Mode 1 [$t_0 \sim t_1$]: This mode begins when P_2 turns off at time t_0. The resonant current i_r is negative and starts to discharge the output charge Q_{oss} of P_1. This mode is a transient mode and will be neglected in analysis for simplification.

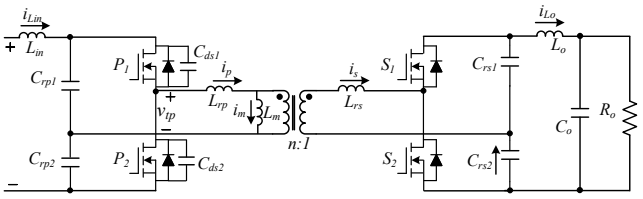


Fig. 2. Proposed half bridge current-fed SRC configuration

Mode 2 [$t_1 \sim t_2$]: At time t_1, the voltage on C_{ds1} is discharged to 0 and resonant current i_r flows through P_1's body diode. P_1 turns on after t_1 with ZVS, and i_r resonates at positive half cycle. The equivalent circuit for time interval [$t_1 \sim t_2$] is shown in Fig. 4. The input and output inductors are treated as two current sources, I_{in} and I_o. The current difference between I_{in} and i_r flows into C_{rp1}, while the difference between i_r and I_o goes into C_{rs1}. The other resonant capacitors, C_{rp2} and C_{rs2}, are clamped by I_{in} and I_o, respectively.

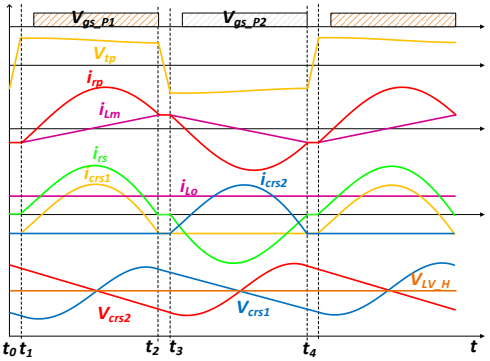


Fig. 3. Operation waveforms under normal load.

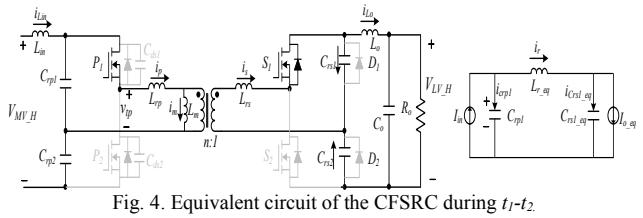


Fig. 4. Equivalent circuit of the CFSRC during t_1-t_2.

The detail analysis of CFSRC has been carried out in paper [19] under time domain and frequency domain.

Based on first harmonic approximation (FHA) method, the circuit can be simplified as shown in Fig. 5. In which a high frequency voltage source is driving a resonant network with all parameters reflected to the primary side. Equivalent ac load, resonant tank components values are expressed as

$$R_{ac} = \frac{2}{\pi^2} R_o \tag{1}$$

$$L_{eqp} = \frac{4}{\pi^2 \omega_s^2 C_{rp}}, L_{eqs} = \frac{4}{\pi^2 \omega_s^2 C_{rs}} \tag{2}$$

Fig. 5 indicates that the equivalent ac circuit of CFSRC is different from VFSRC, two additional inductors, L_{eqp} and L_{eqs}, are introduced into the circuit.

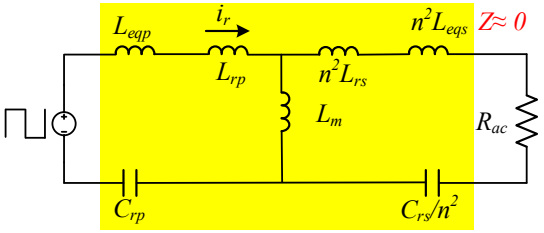


Fig. 5. Equivalent simplified circuit

The equivalent resonant frequency of CFSRC is derived as

$$f_{zc} = \frac{\sqrt{1-\frac{4}{\pi^2}}}{\sqrt{C_r L_r}} = \frac{0.771}{\sqrt{C_r L_r}} = 0.771 f_r \qquad (3)$$

Where $f_r = \frac{1}{\sqrt{L_r C_r}}$, $C_r = \frac{C_{rp}C_{rs}/n^2}{C_{rp}+C_{rs}/n^2}$, $L_r = L_{rp} + n^2 L_{rs}$

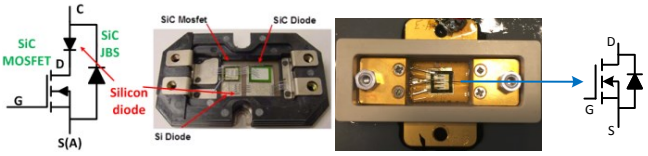
When switching frequency is selected at this frequency, the impedance of the resonant tank equals to zero and system gain is 1. In this paper, switching frequency is selected constantly at this point for high efficiency performance.

Under normal operation, ripple voltage on secondary resonant capacitors should not be large than output voltage to avoid conducting of their paralleled diodes. The constraint for the secondary resonant capacitor value offered in (4)

$$C_{rs} \geq \frac{I_o T_s}{2V_o} \qquad (4)$$

III. ZVS Design and Device Utilization

It is crucial to realize ZVS operation to utilize the 15 kV MOSFET's voltage and frequency potential. Otherwise energy stored in device output charge will result in huge switching loss, which will in turn limit the switching frequency [7].



(a) packaging with silicon and JBS diodes (b) single switch package

Fig. 6. 15 kV SiC MOSFET packaging types

A. Device Packaging Consideration

Body diode of the 15 kV SiC MOSFET has poor R_{ds_on} and reverse recovery performance. Additionally, some researchers have found that the forward conduction of the body diode may cause significantly device degradation [23], [24]. For above reasons, it is necessary to avoid current flowing through this diode during operation. Conventional applications solve this issue with advanced device packaging shown in Fig. 6 (a). A silicon diode is generally connected in series with the MOSFET to prevent the body diode from conducting, while a 15 kV SiC JBS diode is placed in paralleled to conduct the reverse current. However, this method has several drawbacks: 1) JBS diode may contributes significant higher output charge Q_{oss} of the device, which requires additional deadtime for ZVS operation. 2) The series Si diode experiences avalanche breakdown every switching cycle and may affect the reliability of device.

Single die package shown in Fig. 6 (b) shows a simpler structure.

The Q_{oss} of the MOSFET is nonlinear versus the applied voltage V_{ds}. Reference [14] proposed a very accurate method to measure the output charge of MOSFETs up to MV range. With this method, the Q_{oss} versus V_{ds} for two package types are depicted in Fig. 7 and the corresponding curve fitting equations are provided in (5) and (6), respectively.

$$Q_{oss\_combine}(V_{ds}) = 11.43\sqrt{V_{ds}} + 36 \cdot V_{ds} \qquad (5)$$

$$Q_{oss\_single}(V_{ds}) = 4.08\sqrt{V_{ds}} + 24.8 \cdot V_{ds} \qquad (6)$$

Equations (5) and (6) show that JBS diode doubles the total output charge of device, which means longer deadtime or higher turn off current are needed to realize ZVS, both of which will contributes to higher conduction loss.

This paper will show that, if the resonant tank and deadtime are designed properly, current won't flow through body diode and this property won't change as load changes. Thus, single die package shown in Fig. 6 (b) can be used.

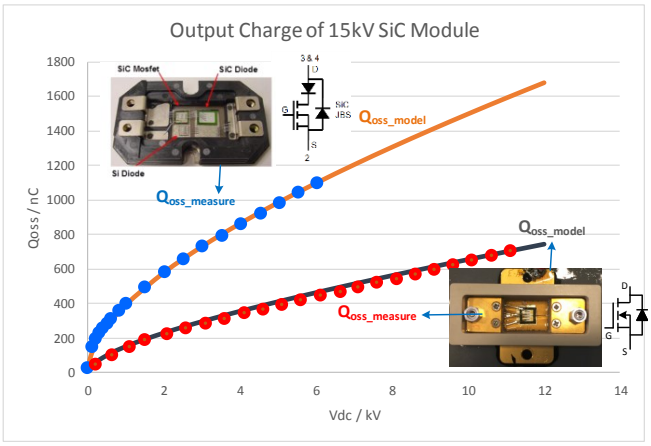


Fig. 7. Output charge of 15 kV SiC MOSFET modules

B. ZVS Design Based on 15kV SiC MOSFETs

With constant operation frequency, the ZVS condition is only associated with input voltage, magnetizing current, and deadtime. The turn off current of CFSRC is derived

$$I_{Lm}(V_{ds}) = \frac{V_{ds} T_s}{8 L_m} \qquad (7)$$

This current is independent of load condition and is used to discharge and charge the output charge, Q_{oss}, of the SiC MOSFETs switches, P_1 and P_2, during deadtime. ZVS constraint is obtained as

$$I_{Lm} t_{dead} \geq 2 Q_{oss} \qquad (8)$$

Increasing deadtime or decreasing magnetizing inductance helps to reduce the turn on loss. However, smaller magnetizing inductance leads to larger circulating and RMS current in the circuit. Longer deadtime also leads to higher RMS current.

Both methods will cause larger conduction loss in the circuit. The L_m and t_{dead} selection is actually a trade-off between switching loss and conduction loss.

RMS current on MV side can be calculated with equations (12) [25].

$$I_{RMS\_P} = \sqrt{\frac{\pi^2 I_o^2}{2n^2}\left(\frac{T_s}{T_s - 2t_{dead}}\right)^2 + \frac{\left(\frac{V_{in}T_0}{8L_m}\right)^2}{2}} \qquad (9)$$

In this paper, L_m and t_{dead} values are designed as 20 mH and 1.5 µs, respectively, at switching frequency of 40 kHz.

C. Device Switching Frequency and Thermal Utilization

With proper L_m and deadtime design, switching loss on MV device is almost zero. This indicates that potential higher switching frequency can be realized with this MOSFET. If deadtime keeps constant, increasing switching frequency will lead to higher RMS current and result in larger conduction loss. The SiC MOSFET on-resistance model can be found in [11]. In our case, the 15 kV SiC MOSFETs are mounted on a natural cooling heatsink with overall junction to air thermal resistance of 1.5 °C/W.

Paper [20] illustrates that MOSFET junction temperature T_j is related to gate driver topology. However, to simplify analysis, the on-state resistance R_{on}, and thermal model T_j of 15 kV SiC MOSFET in [11] is used for calculation.

To fully utilize the 15 kV SiC MOSFETs to its full voltage, frequency and power potential. Basing on the switching and conduction model, a series of optimized designs are provided in Fig. 8 with V_{MV} ranging from 6 to 12 kV and switching frequency, f_s, from 20 to 100 kHz. The figure shows that if ZVS is well secured, a potential switching frequency of 100 kHz and power over 30 kW can be achieved at 10 kV condition with only two 15 kV SiC MOSFETs.

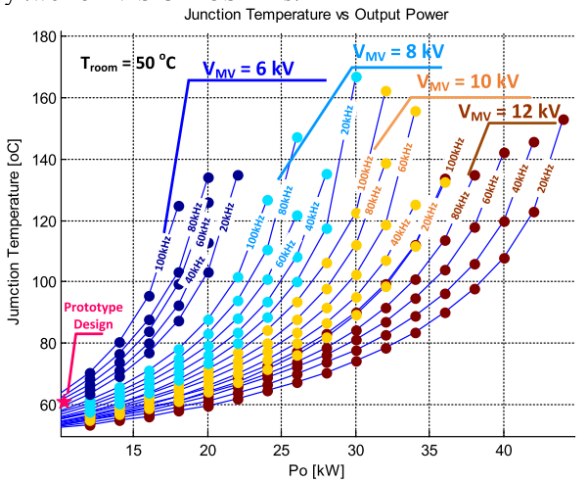


Fig. 8. Optimized (minimum)15 kV SiC MOSFET junction temperature versus processed power with different f_s and V_{MV} in DC-DC application. Cooling=Natural convection [11]

IV. Over Current Operation Principle

Current limiting capability is a very desirable property in MV applications. The short circuit current is a function of the voltage and the equivalent impedance of the resonant tank and load. As can be seen from Fig. 5, the equivalent impedance of resonant tank under normal operation is close to zero under normal load operation, which will result in huge current if short circuit happens.

Clamping resonant capacitors during over load condition is an effective way to limit current during over load condition in LLC type of circuits. However, resonant capacitors are distributed on both side of the converter in the proposed CFSRC circuit. In MV applications, it is not cost effective to parallel MV diodes on MV resonant capacitors merely for overload protection.

To simplify analysis, only worst case, short circuit condition, is analyzed in in this paper. Proposed circuit in this paper parallels only two diodes D_1 and D_2 on secondary side resonant capacitors. When short circuit happens, secondary side resonant capacitors are clamped by diodes.

The detailed operation waveforms under short circuit condition are found in Fig. 9.

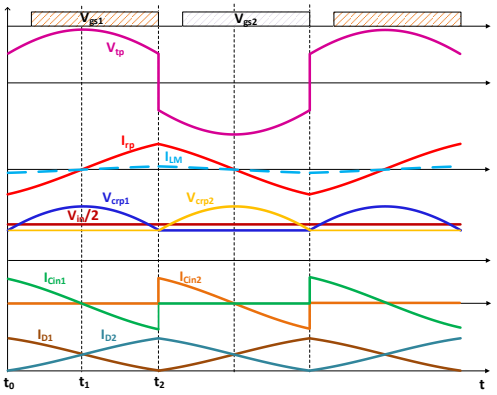


Fig. 9. Operation waveforms under short circuit condition.

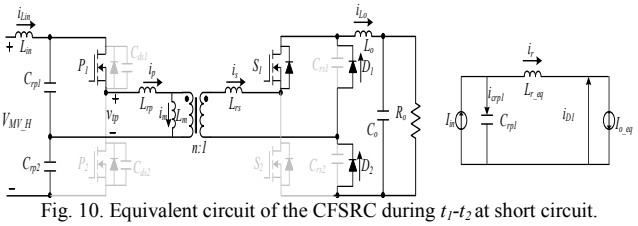


Fig. 10. Equivalent circuit of the CFSRC during t_1-t_2 at short circuit.

The equivalent circuit during time [$t_1 \sim t_2$] at short circuit condition is given in Fig. 10. The differential equation during this interval is derived in (13)

$$\frac{d^2 i_r(t)}{dt^2} + \frac{i_r(t)}{L_r C_{rp}} = \frac{I_{in}}{L_r C_{rp}} \qquad (10)$$

Where $\omega_{r1} = \frac{1}{\sqrt{L_r C_{rp}}}$.

Under short circuit condition, there is no real power transferred to the output, and secondary resonant capacitor is clamped out of the operation. Only reactive power is circulating inside the resonant tank and the input current can be regarded as zero. Therefore, (13) can be simplified into (14).

$$\frac{d^2 i_r(t)}{dt^2} + \frac{i_r(t)}{L_r C_{rp}} = 0 \qquad (11)$$

The common solution for (11) is derived in (12) and (13).

$$i_r(t) = -I_{r\_t0}\cos(\omega_{r1}(t-t_0)) + \frac{V_{crp\_t0}}{Z_{r1}}\sin(\omega_{r1}(t-t_0)) \quad (12)$$

$$v_{crp}(t) = I_{r\_t0}Z_{r1}\sin(\omega_{r1}(t-t_0)) + V_{crp\_t0}\cos(\omega_{r1}(t-t_0)) \quad (13)$$

Where $Z_{r1} = \sqrt{\frac{L_r}{C_{rp}}}$, $I_{r\_t0} = -I_r, V_{crp\_t0} = V_{crp0}$.

Current and voltage values at time $\frac{T_s}{2}$ are $i_r\left(\frac{T_s}{2}\right) = I_r$, $v_{crp}\left(\frac{T_s}{2}\right) = V_{crp0}$.

The charging balancing of the capacitors equation in (14) can be used to solve (12) and (13).

$$\int_{t_0}^{t_0+\frac{T_s}{2}} [I_r Z_{r1}\sin(\omega_{r1}(t-t_0)) + V_{crp\_t0}\cos(\omega_{r1}(t-t_0))]\,dt + \frac{T_s}{2}V_{crp\_t0} = \frac{V_{in}}{2}T_s \quad (14)$$

The distribution of the capacitor will affect the current limiting capability. Equivalent circuit capacitance C_r is decided by resonant frequency and L_r. If the relationship between C_{rp} and C_r is set as $C_{rp} = kC_r$, where k >1. (15) is derived

$$\varphi(k) = \omega_{r1}\left(\frac{T_s}{2}\right) = \frac{1.292\pi}{\sqrt{k}} \quad (15)$$

The peak current of primary side versus the input voltage and coefficient k can be derived based on (12), (13) and (14).

$$I_{peak}(k) = \frac{V_{in}\frac{\sin(\varphi(k))}{Z_{r1}}}{(1+\cos(\varphi(k))) + \frac{2\sin(\varphi(k))}{\varphi(k)}} \quad (16)$$

Equation (16) dictates the design criteria for short circuit current limiting capability, in particular the resonant tank components, L_r, C_{rp} and C_{rs}. The peak current under short circuit condition depends on L_r value and distribution of the resonant capacitors.

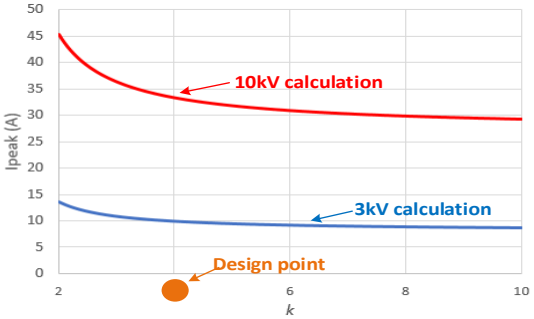


Fig. 11. Peak current versus k at different peak voltage conditions.

Fig. 11 shows the peak current curves versus the k value under different voltage conditions when L_r is designed at 1.3 mH. k represents the distribution of the resonant capacitance inside the system. Increasing k means C_{rp} is larger and C_{rs} is closer to C_r, which helps reduce the peak current at short circuit conditions. However, increasing k will result in larger capacitor values and leads to larger capacitor size and weight. While when k is large enough, increasing k doesn't significantly helps reduce peak current. k is selected as 4 in this design case, with which peak current is expected to be within 35 A at 10 kV short circuit condition.

V. Experimental Results

A compact 20 kW prototype is developed to verify the theoretical works presented in this paper. Fig. 12 shows the overall system hardware, in which only film capacitors are adopted. It is designed convert 10 kV to 340 V at switching frequency of 40 kHz. Table I summarizes the key system components and specifications. The whole control system is based on DSP TMS320F28377D.

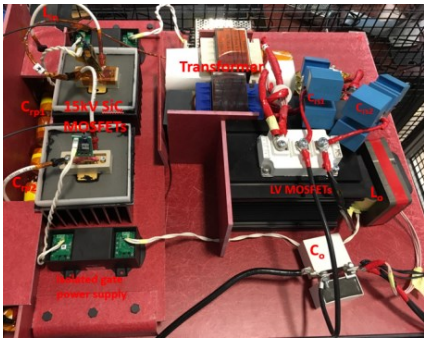


Fig. 12. Hardware structure of 10 kV/20 kW TLSS SST.

TABLE I
System Parameters for TLSS SST

Symbol	Quantity	Value
V_{MV}	MV input voltage	10kVac
V_{LV}	LV grid voltage	340Vac
f_s	Switching frequency	37kHz
P	System power	20kW
R_1-R_4	Input Diode Bridge	SKNa 47/50
L_{in}/L_o	MV/LV Side Inductor	10mH/400uH
L_m	Transformer Magnetizing inductance	18.5mH
L_r	Resonant inductance	1.32mH
C_{rp1}/C_{rp2}	Primary Resonant capacitance	37nF
C_{rs1}/C_{rs2}	Secondary Resonant capacitance	2.5uF
n	Transformer turns ratio	207:7
P_1/P_2	15kV SiC MOSFET	
S_1/S_2	Secondary MOSFET	CAS300M12BM2
C_o	LV Side Filter Capacitor	5uF
R_5-R_8	Unfolding Bridge Module	PM75RLB060
	Controller	TMS320F28377D

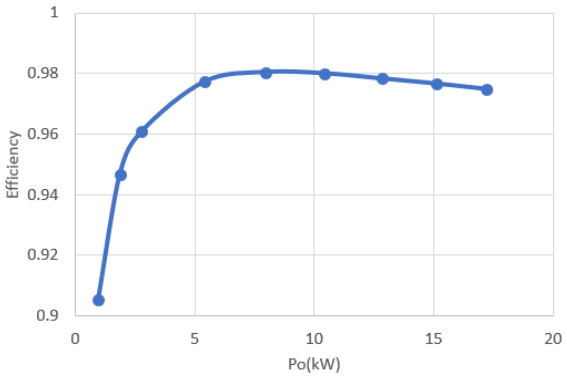


Fig. 13. Measured MV TLSS-SST efficiency, V_{MV}=10 kV, P_o from 900 W to 17 kW.

Fig. 14 (a) and (b) show the system operation waveforms at 10 kV, 17 kW condition. Fig. 14 (b) is the magnified view of the

switching cycle waveforms with a switching frequency of 37 kHz. The orange waveform is the V_{ds} voltage of the 15 kV MOSFET, which shows verifies that ZVS operation is achieved at 10 kV.

Fig. 14 (c) provides the detailed operation waveforms of this prototype under a very light load of 900 W. ZVS of the MV MOSFETs is still well realized under this load condition.

Efficiency of the prototype under 10 kV input voltage and wide load range are tested and the curve is provided in Fig. 13. The peak efficiency is over 98%. Efficiency under heavy load condtions are over 97%.

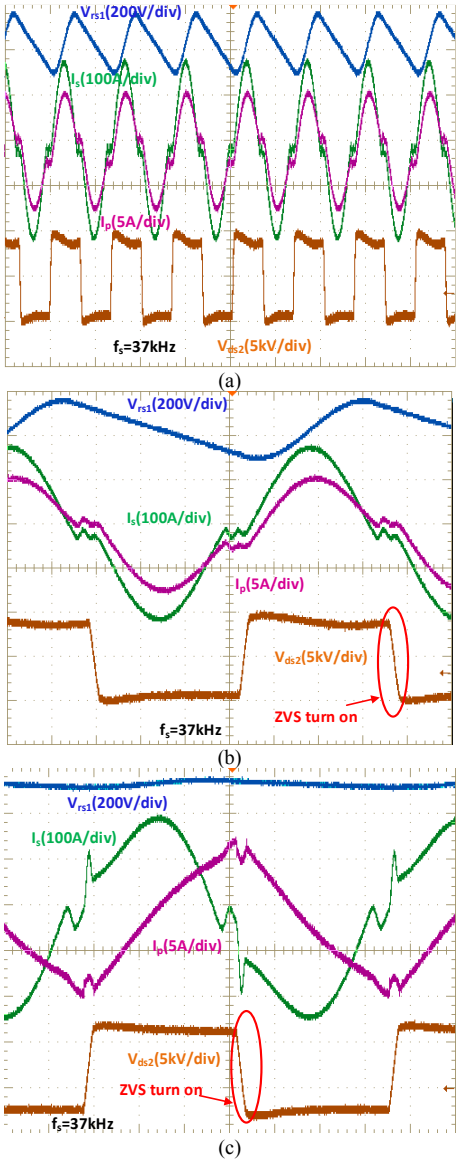


Fig. 14. Steady operation waveforms. (a) Line frequency viewpoint and (b) Switching frequency magnified at V_{MI}=10 kV, P_o=17 kW. (c) Magnified view with light load of P_o=900 W.

In order to verify the validity of the theoretic analysis on overload current limiting capability, short circuit tests are conducted under 2kV and 3 kV conditions. Experiments is not conducted under 10 kV because peak current will be around 35 A under that condition, which will exceed the device's current rating.

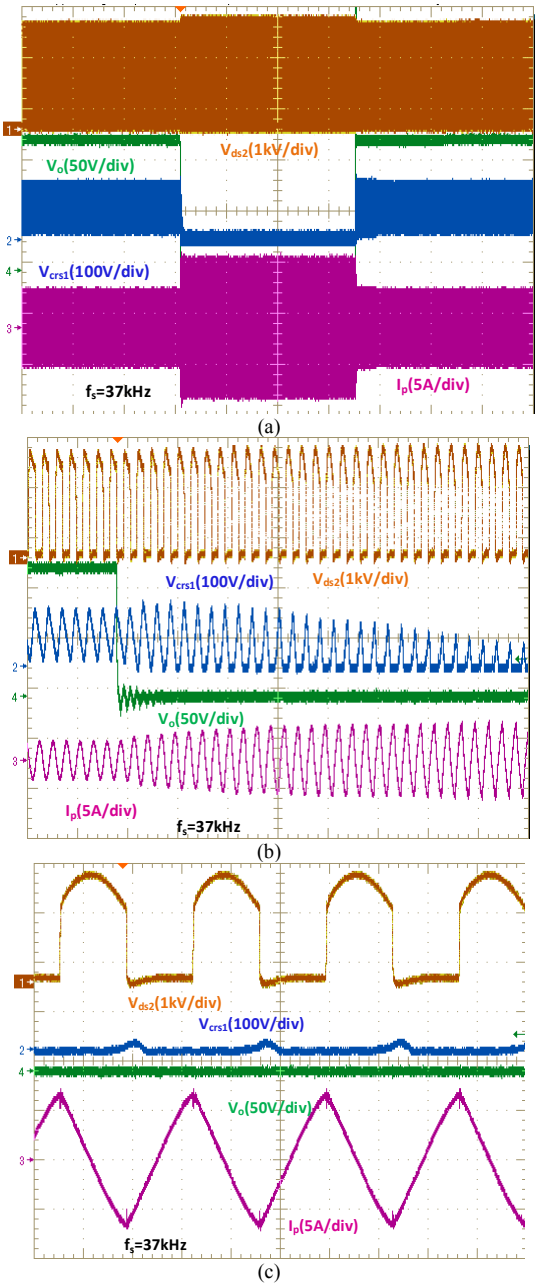


Fig. 15. Short circuit operation waveforms at 3 kV peak voltage. (a) and (b) short circuit dynamic. (c) short circuit steady state.

Fig. 15 (a) and (b) shows the transient moment when short circuit happens at 3 kV condition, at which moment the output voltage is pulled to zero within 1 μs. The blue curve is the voltage on secondary resonant capacitor, which start to be clamped by its paralleled diode from the moment. Cycle by cycle current limiting is achieved and the peak value of primary transformer current I_p. is limited within 11 A at this condition

as shown in Fig. 15 (c). Zero voltage turn on of the MV switches is still guaranteed under this condition. If system parameters and switching frequency keeps constant, this short circuit peak current is proportional to input voltage. Even at 10 kV voltage condition, the peak current is still limited within 35 A.

I. Conclusion

This paper proposes a high efficiency 10 kV DCX for MV applications based on a novel CFSRC topology and 15 kV MOSFETs. CFSRC enables ZVS operation across entire load range for high efficiency performance and all film capacitor system for high power density. Resonant tank and deadtime are designed properly for the use of single die packaged device. Paralleling diodes on LV resonant capacitors enables inherent cycle current limiting capability under over load condition. Theoretical analysis under normal load and over load conditions are provided. A compact 20 kW prototype is built to convert 10 kV to 340 kV with a switching frequency of 37 kHz, which achieves peak efficiency over 98%. ZVS is realized from light load to heavy load conditions. Short circuit is conducted under 3 kV, in which the peak current of the system is only 11 A. It is expected that when short circuit happens at 10 kV, the peak current inside the circuit can be limited within 35 A.

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