Single-Phase Transformerless Dual Buck-Based Grid-Connected Inverter

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***Abstract*—This work proposes a novel single-phase transformerless dual buck-based grid-connected inverter. The proposal features only two power semiconductors in the current path at all operating stages and, thus, enables low conduction losses. The topology guarantees increased robustness since the dc-bus cannot be short-circuited by a shoot-through event. Since the inverter uses two inductors the use of coupled inductors is proposed to reduce the overall passive components volume and better use of the magnetic cores. Experimental results of a 2 kW prototype (+380 V to 220 V /60 Hz) are presented, which show that the proposed inverter is able to achieve high efficiency ($> 98\%$) and low common-mode voltage when switching at 50 kHz.**

I. Introduction

A key enabler of the trend towards the universal deployment of distributed solar photovoltaic (PV) systems is the transformerless grid-connected PV inverter [1]–[3], i.e., dc-ac converters that ideally do not generate common-mode voltages at the switching frequency. Such feature prevents the generation of high ground leakage currents that would otherwise circulate through the typically high capacitance to ground found in PV modules arrangements. Therefore, transformerless inverters can be used without galvanic insulation and provide reduced dimensions, cost, weight, high frequency conducted emissions and increased efficiency.

The conventional H-bridge inverter can be used when bipolar modulation is employed. However, this leads to larger ac-side inductors when compared to the unipolar modulation. In addition, silicon MOSFETs cannot be used in hard switching conditions since their body diodes reverse recovery characteristics would lead to very high turn-on transition losses. Increasing the output current ripple can lead to soft switching operation, but lead to high rms current values and higher attenuation requirements for the ac-side EMC filter. Several transformerless inverter topologies and according modulation strategies have been proposed to improve the attainable performance with the conventional H-bridge. Transformerless hard-switching grid-connected inverter solutions include: (a) the HERIC inverter [4]; (b) the H5-inverter [5]; (c) the H-bridge inverter with dc bypass [6]; (d) the H6-inverter variations [7]–[9]; (e) the two paralleled buck converters inverter [10]; (f) two dual paralleled buck converters inverter [10]; (g) three-level inverters [11]; and, (h) the dual paralleled buck converters inverter with ac-side decoupling [12]. Most of the aforementioned topologies are protected under intellectual property rights.

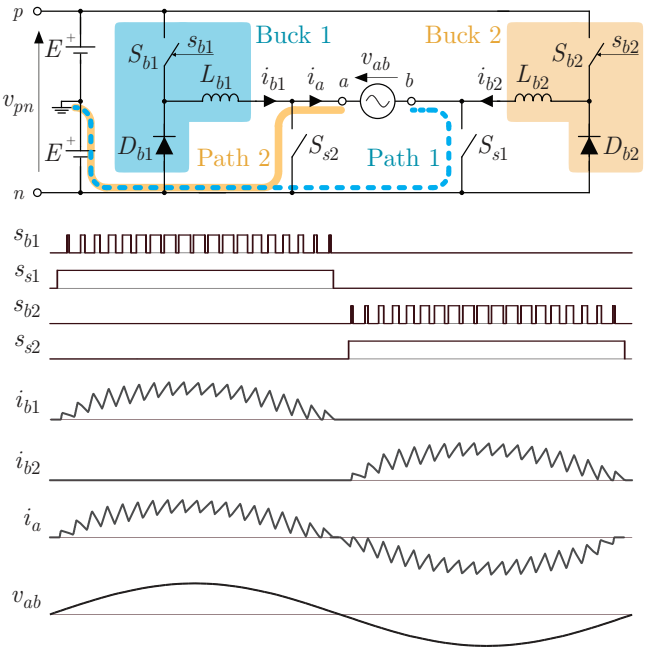

Fig. 1. Principle of a paralleled buck converter-based grid-connected inverter.

The three-level topologies require that the dc-bus average voltage level is, at least, twice the peak value of the ac-side voltage and, thus, demand higher voltage ratings for the power semiconductors. The H5-inverter, the H6-inverter and the H-bridge inverter with dc bypass present three power semiconductors conducting the inductor current in at least one operating stage, while the HERIC and the paralleled buck converters-based inverters (PBCIs) have only two semiconductors in the current path during all operating stages. This potentially leads to lower conduction losses, which is highly desirable for grid connected PV systems. In addition, the PBCIs are all shoot through free at least in their dc-side port due to diodes naturally offering a one way path to the currents. This enables higher robustness and the possibility to use silicon carbide (SiC) diodes to implement two of the high switching

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frequency devices. Thus, silicon (Si) MOSFET devices can be used for the other devices. SiC MOSFETs can also be advantageously employed. The converter presented in [12] also features no shoot through possibility at the ac-side since it has no pair of switches that could, by simultaneously conducting, create a short-circuit at the ac-side EMC filter capacitor. The other PBCIs present turn-off switches that directly connect one of the ac-side terminals to the dc-bus. This guarantees a hard physical connection and ideally null common-mode (CM) voltage across the converter at the switching frequency. The low common mode feature can be understood by examining Fig. 1, where the principle of a PCBI is illustrated. Two buck converters are present denoted by components with subindices 1 and 2. The first buck converter is composed of turn-off switch S_{b1}, diode D_{b1}, inductor L_{b1} and it operates whenever the selector switch S_{s1} is turned-on, i.e., during the mains half-cycle where current i_a is positive. Assuming that the local average value (defined with $\bar{x} = 1/T_{sw} \cdot \int_{t-T_{sw}}^{t} x(\tau)\, d\tau$) of the ac-side current a sinusoidal fundamental component for i_a defined with

$$\bar{i}_a = \hat{I} \sin(\omega t), \tag{1}$$

that is in phase with an ac-side voltage

$$\bar{v}_{ab} = \hat{V} \sin(\omega t). \tag{2}$$

The modulation index (M) assuming a constant dc-bus voltage $v_{pn} = V_{dc}$ can be defined as

$$M = \frac{\hat{V}}{V_{dc}} \tag{3}$$

The required duty-cycle for the buck 1 converter PWM switch is

$$\delta_{b1} = \bar{s}_{b1} = \begin{cases} M \sin(\omega t) & \text{if} \quad 0 \leq \omega t \leq \pi \\ 0 & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases}, \tag{4}$$

if the voltage drop across inductor L_{b1} at the fundamental frequency is negligible. Thus, the selector switch 1 is commanded with the duty-cycle

$$\delta_{s1} = \bar{s}_{s1} = \begin{cases} 1 & \text{if} \quad 0 \leq \omega t \leq \pi \\ 0 & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases}. \tag{5}$$

The second buck converter (composed of S_{b2}, D_{b2} and L_{b2}) operates during the other mains half-cycle, when selector switch S_{s2} is on. Thus, the duty-cycles for the second buck converter must be

$$\delta_{b2} = \bar{s}_{b2} = \begin{cases} 0 & \text{if} \quad 0 \leq \omega t \leq \pi \\ M \sin(\omega t) & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases} \tag{6}$$

and

$$\delta_{s2} = \bar{s}_{s2} = \begin{cases} 0 & \text{if} \quad 0 \leq \omega t \leq \pi \\ 1 & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases}. \tag{7}$$

The selector devices operate as a two pole single throw switch. It is then clear that either *Path 1* or *Path 2* do create a low impedance way between the dc-bus and the ac-port and, thus, no high frequency CM voltage is generated in this type of converter. The illustrated PCBI example also explains the fundamental limitation of this type of converter regarding the phase displacement from the mains voltage v_{ab} to the fundamental component of the injected current i_a, here named ϕ_a. The phase displacement must be null in order for this converter to inject a sinusoidal current into the grid. This is related to the use of diodes, e.g., in positions D_{b1} and D_{b2}, which prevent that the individual buck converter currents i_{b1} and i_{b2} become negative. Thus, the PCBIs that use diodes in the mentioned positions can only handle a displacement factor $\lambda = \cos(\phi_a) = 1$ and can be considered unidirectional inverters.

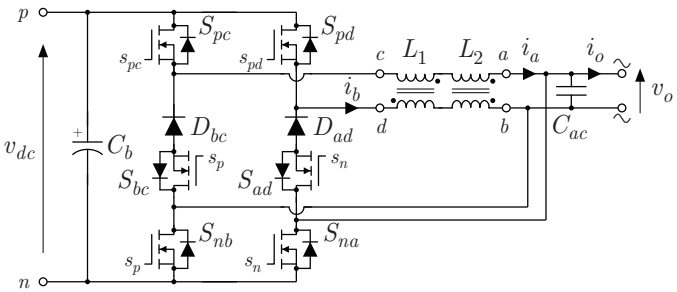

Fig. 2. Proposed transformerless dual buck-based grid-connected inverter.

This work proposes a new member to the PBCI-type inverters, which is presented in Fig. 2 and is here named dual buck-based inverter with coupled inductors. It features only two power semiconductors in the current path at all operating stages, i.e., low conduction losses are observed. It also presents the feature that the dc-bus cannot be short-circuited since diodes D_{bc} and D_{ad} prevent it in any case. Thus, robustness against shoot-through events is achieved. These diodes and the switches S_{pc} and S_{pd} switch at the PWM carrier frequency. Switches S_{bc}, S_{ad}, S_{nb} and S_{na} switch only at the ac-side fundamental frequency and, thus, can take advantage of low forward voltage drop power semiconductors. The proposed inverter principles of operation are presented in the Section II, the static analysis is shown in Section III, while experimental results are discussed in Section IV. Finally, conclusions are drawn.

II. Operation Principles

The proposed inverter is composed of two sub-converters that can be understood as two buck converters, each operating at one of the ac-side half-cycles. These sub-converters are shown in Fig. 3, where Fig. 3(a) highlights the components that carry current during the positive half-cycle of v_o and Fig. 3(b) during the negative one.

The employed modulation strategy is seen in Fig. 4(a) and Fig. 4(b). A modulating signal m is compared against a triangular carrier c and the resulting PWM signal s is then directed to the PWM switches s_{pc} and s_{pd} according to the ac-side polarity. The polarity of the ac-side voltage is used to define the switching signal

$$s_p = \frac{\text{sgn}(v_o) + 1}{2} \tag{8}$$

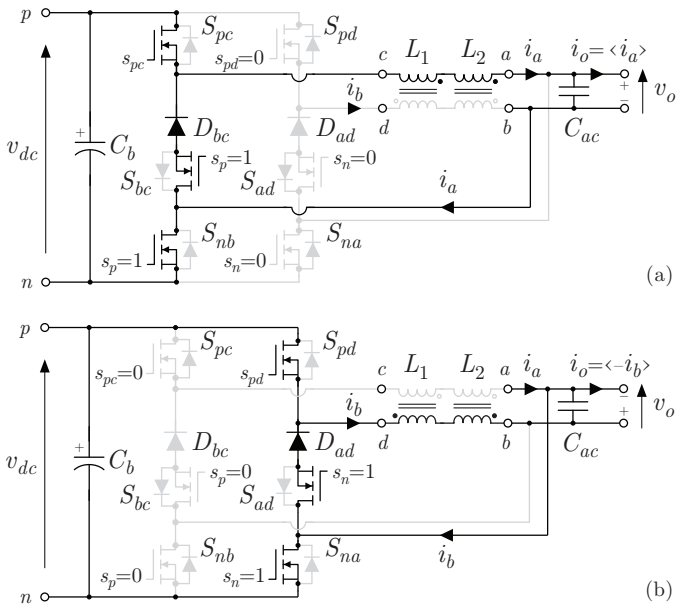

Fig. 3. Sub-converters: (a) ac-side positive half-cycle buck dc-dc converter; and, (b) negative half-cycle buck converter. The gray components ideally do not carry currents in the respective half-cycles of the fundamental period.

that commands the low frequency switches S_{bc} and S_{nb}, where

$$\text{sgn}(x) = \begin{cases} 1 & \text{if} \quad x > 0 \\ 0 & \text{if} \quad x = 0 \\ -1 & \text{if} \quad x < 0 \end{cases}, \tag{9}$$

while the switching signal

$$s_n = 1 - \text{sign}(v_o) \tag{10}$$

drives the switches S_{ad} and S_{na}. Thus,

$$s_{pc} = \begin{cases} s & \text{if} \quad 0 \leq \omega t \leq \pi \\ 0 & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases}, \tag{11}$$

$$s_{pd} = \begin{cases} 0 & \text{if} \quad 0 \leq \omega t \leq \pi \\ s & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases}, \tag{12}$$

and

$$s_{bc} = s_{nb} = 1 - s_{ad} = 1 - s_{na} = \begin{cases} 1 & \text{if} \quad 0 \leq \omega t \leq \pi \\ 0 & \text{if} \quad \pi \leq \omega t \leq 2\pi \end{cases}. \tag{13}$$

Diodes D_{bc} and D_{ad} operate complementarily to switches S_{pc} and S_{pd}, respectively.

The coupled inductors operate according to the same principles as presented in the power factor correction PWM rectifier proposed in [13].

An interlock delay time between the transitions of s_n and s_p, at the zero crossings of v_o is required in order to prevent a short-circuit of the capacitor C_{ac} during the polarity reversal events of the ac-side voltage v_o. This can be done by using an algorithm that has a phase locked looped (PLL) providing the ac-side voltage angle and a voltage sensor that measures the voltage. A logic can then be built in order to guarantee that there are no shoot throughs close to the polarity reversals.

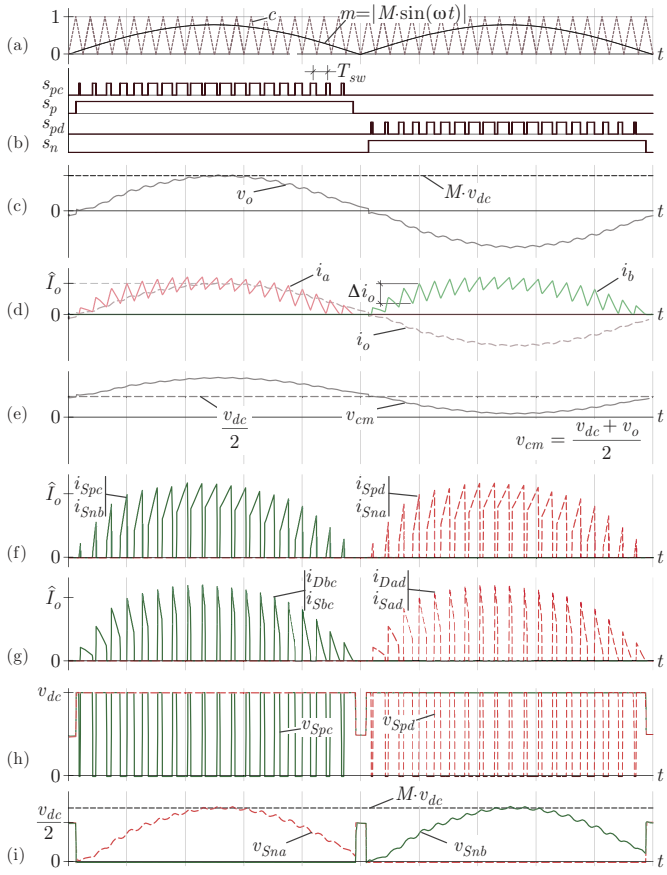

Fig. 4. Waveforms for ideal operation of the proposed inverter. Shown are: (a) carrier (c) and modulating (m) signals; (b) switching functions of the PWM switches (s_{pc} and s_{pd}) and of the fundamental frequency switches (s_p and s_n); (c) ac-side voltage (v_o); (d) ac-side current (i_o) and windings currents (i_a and i_b); (e) common-mode voltage (v_{cm}); (f) currents through the outer switches S_{pc}, S_{nb}, S_{pd} and S_{na}; (g) currents through the inner switches D_{bc}, S_{bc}, D_{ad} and S_{ad}; (h) voltages over the upper switches S_{pc} and S_{pd}; and, (i) voltages over the lower switches S_{nb} and S_{na}.

The ideal operation waveforms of the main components are presented in Fig. 4. Fig. 4(a) shows the modulation waveform m and carrier c. The resulting pulse pattern is seen in Fig. 4(b). The ac-side voltage considering a line filter is presented in Fig. 4(c). The currents flowing through the inductors and into the ac-side are depicted in Fig. 4(d). The inverter common mode voltage, defined by

$$v_{cm} = \frac{v_{dc} + v_o}{2} \tag{14}$$

is observed in Fig. 4(e), where no high switching frequency ideally exists. The instantaneous currents through the PWM switches are in Fig. 4(f) and Fig. 4(g). The voltages across the upper switches shown in Fig. 4(h), where it is seen that they do not switch close to the zero crossings due to the implemented interlock logic. This can also be seen in the voltages over S_{na} and S_{nb} in Fig. 4(i).

As the proposed inverter operates similarly to the one explained in Section I, it cannot handle non unity power factor

operating conditions without heavy distortions in the ac-side current waveform.

III. Static Analysis

This section presents the theoretical analysis of the current efforts in the main components of the proposed converter.

Assume that $i_o(t)$ is the inverter output current and it is given by

$$i_o = \hat{I}_o \sin(\omega t), \tag{15}$$

where $\hat{I}_o$ is the peak inverter output current and the $\omega = 2\pi f_o$ is the angular frequency of the inverter output current. The theoretical sinusoidal voltage reference is expressed by

$$m = |M \sin(\omega t)|, \tag{16}$$

where M is the inverter modulation index. The ac-side voltage local average value is then

$$\bar{v}_o = m \ (\text{sgn}\left[\sin(\omega t)\right]) \ v_{dc} = M \sin(\omega t). \tag{17}$$

The duty ratios for S_x devices, with $x = \{pc, pd\}$ at their respective working half-cycles are

$$\delta_{S_x} = m, \tag{18}$$

and the duty ratios for S_y devices, with $y = \{bc, ad\}$, at their respective working half-cycles are

$$\delta_{S_y} = 1 - m. \tag{19}$$

The local average and rms values of a given device S_z can be ideally expressed by

$$\bar{i}_{S_z} = \bar{i}_o \cdot \delta_{S_z} \tag{20}$$

and

$$i_{S_z}^{\text{rms}} = i_o^{\text{rms}} \cdot \sqrt{\delta_{S_z}}, \tag{21}$$

respectively, where $\bar{i}_o$ and i_o^{rms} are respectively the output current average and rms local values. This assumes that the ac-side current i_o presents low ripple and slow time variation.

Finally, the global average and rms values of the S_x and S_y devices can be found with

$$\bar{X} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} x \ d\omega t} \tag{22}$$

and

$$X^{\text{rms}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} x^2 \ d\omega t}, \tag{23}$$

respectively.

The overall average and rms values for the power semiconductors currents assuming a piecewise linear evolution of the inductors currents (i.e., the high frequency ripple at each switching period is accounted for) are given by

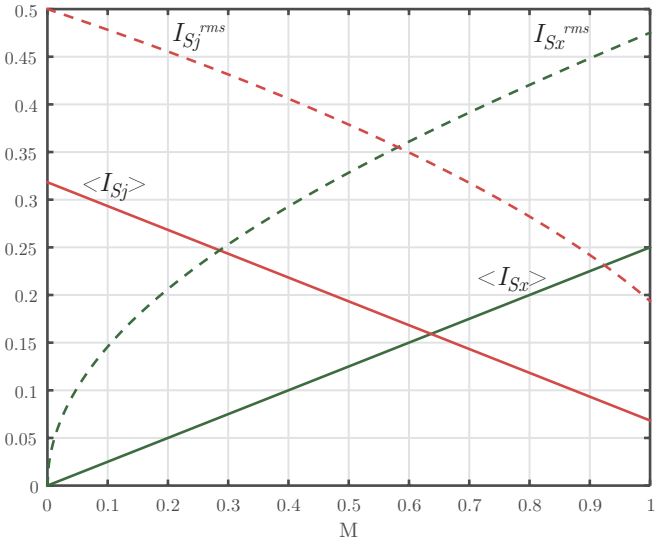

Fig. 5. Normalized average and RMS currents values to the peak value as a function of M.

$$\bar{I}_{S_x} = \frac{M\,\hat{I}_o}{4} \tag{24}$$

$$I_{S_x}^{\text{rms}} = \frac{1}{15}\sqrt{\frac{10\left(M^3\hat{V}_o^2 + 15\,M\hat{I}_o^2L^2f_s^2\right)}{\pi L^2 f_s^2}} \tag{25}$$

$$\bar{I}_{S_y} = \hat{I}_o\left(\frac{M}{4} - \frac{1}{\pi}\right) \tag{26}$$

$$I_{S_y}^{rms} = \frac{1}{120}\sqrt{\frac{5}{\pi L^2 f_s^2}\begin{bmatrix} -\,128\,M^3\hat{V}_o^2 & \ldots \\ +\,45\pi\,M^2\hat{V}_o^2 & \ldots \\ -\,1920\,M\,\hat{I}_o^2L^2f_s^2 & \ldots \\ +\,720\pi\,\hat{I}_o^2L^2f_s^2 & \end{bmatrix}}. \tag{27}$$

Expressions (24) to (27) are used to plot average and rms currents values normalized by $\hat{I}_o$ and as functions of M. This is seen in Fig. 5. Table I presents values that are calculated according using (24) to (27) and results obtained from simulation of the proposed converter operating with $M = 0.819$ and $M = 0.4$. The comparison of these values show very good agreement.

IV. Experimental Results

A prototype with the specifications given in Table II has been built (see Fig. 6) and used to measure the main waveforms of the proposed inverter feeding a resistive load. The high frequency MOSFETs are C2M0080120D from Wolfspeed. The diodes are IDH10G65C5 from Infineon. The low frequency ones are super junction MOSFETS IPW65R037C6 from Infineon. The first version of this inverter uses electrolytic capacitors at the dc-bus. An EMC filter is included. The control is performed by a TMS320F28377S from Texas Instruments. The measured efficiency at rated power was 98.01%.

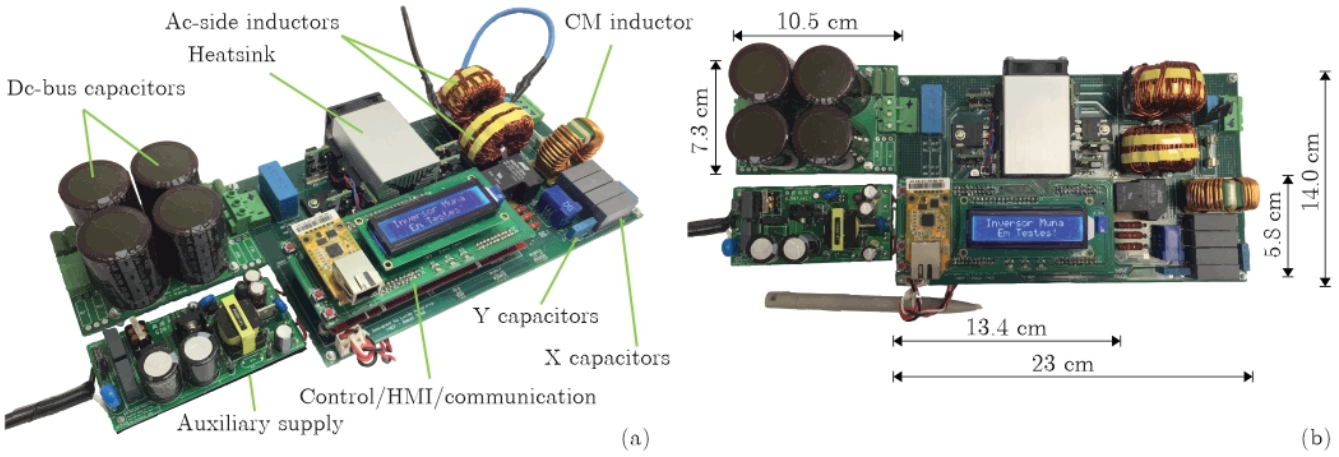

Fig. 6. Photographs of the built 2-kW/220-V inverter prototype.

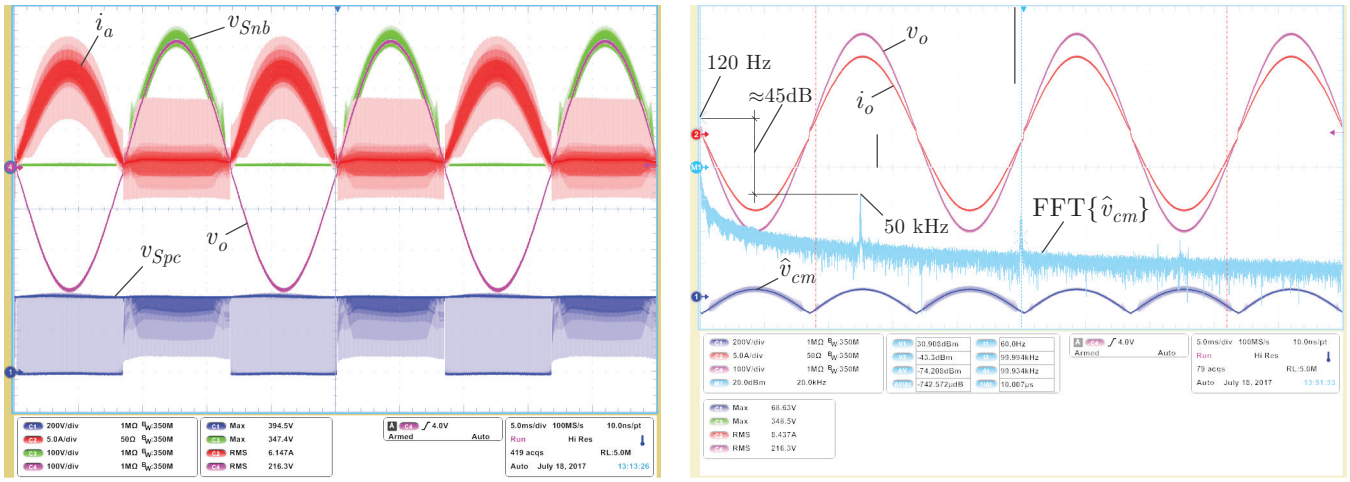

Fig. 7. Experimental waveforms measured in the built inverter prototype: (a) current through one of the inductors (i_a — 5 A/div), voltage across the upper switch S_{pc} (v_{Spc} — 200 V/div), voltage across the lower switch S_{nb} (v_{Snb} — 100 V/div) and ac-side voltage (v_o — 100 V/div); (b) ac-side current (i_o — 5 A/div), ac-side voltage (v_o — 100 V/div), common-mode voltage (v_{cm} — 200 V/div) and its computed FFT (FFT$\{v_{cm}\}$ — 200 dB/div).

TABLE I
COMPARISON BETWEEN CALCULATED AND SIMULATED CURRENT VALUES.

	M = 0.819		M = 0.400	
Variable	Calculated	Simulated	Calculated	Simulated
$\bar{I}_{S_x}$	2.632 A	2.630 A	1.285	1.285
$I_{S_x}^{\text{rms}}$	5.474 A	5.373 A	3.765	3.752
$\bar{I}_{S_j}$	1.460 A	1.462 A	2.806	2.807
$I_{S_j}^{\text{rms}}$	3.536 A	3.571 A	5.219	5.234

Fig. 7(a) shows the current i_a in one of the windings of the coupled inductors, the voltage across the low-side MOSFET S_{nb}, the ac-side voltage v_o across an EMC filter capacitor and the voltage through the upper switch S_{pc}. (refer to Fig. 2). The local average value of the current i_a follows a rectified half sine wave during the positive half-cycle and zero at the negative as expected. Very high frequency current components that appear from the excitation of parasitic components resonances are observed during the whole period. The main components involved in this phenomena are the power semiconductors and PCB capacitances and the loop leakage inductances. These resonances might excite oscillatory voltage waveforms that generate overvoltages across switches S_{bc} and S_{ad}. Two clamping diodes were connected from the negative terminal of the dc-bus to the sources of these MOSFETs due to this reason. The voltages observed across the switches are then well controlled.

The ac-port current i_o and voltage v_o are seen in Fig. 7(b) along with an indirect measurement of the common-mode voltage $\hat{v}_{cm}$ (measured from the negative terminal of the dc-bus to the common point of the EMC filter Y-capacitors).

TABLE II
DUAL-BUCK INVERTER PROTOTYPE SPECIFICATIONS.

Power	Ac voltage	Dc voltage	Switching frequency	Inductors	Dc-bus capacitors
2 kW	220 V / 60 Hz	380 V	50 kHz	490 μH total	1880 μF total

In addition the Fast Fourier Transform of the CM voltage, FFT($\hat{v}_{cm}$), computed by the oscilloscope is shown. A comparison between the 120 Hz component and the switching frequency ($f_{sw} = 50$ kHz) one is seen, where a difference of over 40 dB was measured. Thus, the CM free operation can be confirmed. The output voltage v_o presents low harmonic distortion.

V. CONCLUSIONS

A single-phase transformerless dual buck-based inverter that can be used in grid-connected applications was proposed. It features only two power semiconductors in the current path at any operating stage. This leads to low conduction losses. A dc-bus shoot-through is prevented by the use of two diodes leading to a robust topology, where such diodes can be advantageously implemented with wide bandgap devices and, thus, present very low switching losses. Only two of the four turn-off switches operate at the PWM frequency. The other two devices can be implemented with power semiconductors that can be designed for optimized forward conduction voltage drop. Coupled inductors are used to reduce the inverter passive elements volume and use the magnetic cores during the whole period unlike other known PBCI topologies. Two low frequency switches are used to directly connect the negative terminal of the dc-bus to the ac-side terminals. This guarantees ideally null CM voltage at the switching frequency. Experimental results of a 2-kW prototype were presented, which show that the proposed inverter generate a very low common-mode voltage at the switching frequency. In addition, the paralleled buck-based inverter achieved an efficiency higher than 98% at rated power when switching at 50 kHz and employing SiC devices for the PWM switching devices and Si super junction MOSFETs for the low frequency turn-off switches.

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