Common-Ground Transformerless Inverter for Solar Photovoltaic Module

Saad Ul Hasan[*], Benjamin Shaffer[†], Hassan. A Hassan[†], Mark. J Scott[†], Yam Siwakoti*[†], Graham. E. Town[*]
[*]School of Engineering, Macquarie University, NSW-2109, Australia
[†]Department of Electrical and Computer Engineering, Miami University Oxford, OH 45056, USA
*[†]Faculty of Engineering and IT, University of Technology Sydney, Ultimo NSW 2007, Australia

***Abstract*—This paper presents a new single-phase transformerless inverter providing common ground for grid-connected photovoltaic (PV) systems. It consists of 5 switches, one diode, one capacitor, one small inductor and a small filter at the output stage. A simple Unipolar Sinusoidal Pulse-Width Modulation (SPWM) technique is used to operate the proposed inverter to minimize losses, output current ripple, filter requirements and improve its electromagnetic compatibility (EMC). The proposed topology shares a common ground with the grid and a capacitor is utilized as a virtual DC bus to provide the negative power cycle of the inverter. The capacitor is charged regardless of any switching cycle using a dedicated switch which can in turn reduce the size of capacitor in relation to the switching frequency. The peak ac output voltage is equal to the input DC voltage which reduces the requirement of the high input DC voltages. Simulation and experimental results for a 1 kW prototype are presented to demonstrate the usefulness of the proposed topology.**

Keywords*—Common mode (CM) current; photovoltaic (PV) system; transformerless inverter; unipolar sinusoidal pulse width modulation (SPWM); virtual DC bus.

I. INTRODUCTION

Grid connected photovoltaic (PV) systems are becoming common worldwide due to advancement of power electronics and semiconductor technology along with the falling PV prices due to government subsidies [1]. In the recent years, a strong trend in using various transformerless inverter topologies has been seen to achieve higher efficiencies, improved electromagnetic compatibility (EMC), low ground leakage current in addition to reduction in cost and weight [2]. Various transformerless topologies have been proposed to eliminate the leakage current problems by clamping Common Mode Voltage (CMV) [2-3] or using common ground configurations [4-9]. The CMV clamping requires additional switches, which increases costs and the switch parasitics may still not allow to eliminate the leakage current completely [10], therefore common ground based topologies are gaining more attention. The transformerless inverter topologies with common ground configurations that utilize the concept of virtual DC bus are well suited to reduce the leakage current in a PV system. A common ground transformerless topology has been reported in [4], but the capacitor is only charged in positive cycle which restricts its versatility. An improved capacitor charging process has been reported in [11] in which the capacitor is charged in both cycles. This reduces the size of capacitors, but the topology has additional passive components with a large filter inductor of 5 mH. Recently, several common ground transformerless topologies are reported in [5] and the selection for an optimal topology depends upon various factors such as: 1) minimal number of active and passive components, 2) small filter, 3) simple modulation, 4) capacitor being used as an intermediate energy storage and charged regardless of switching cycles, 5) no leakage current, 6) low switch stress, 7) peak output voltage equal to the DC input and 8) the topology being able to send reactive power to the grid.

The topologies reported in [5] are proposed based on the above-mentioned attributes but the inrush current phenomenon is inevitable as the capacitor is being charged directly via a switch [12]. The novel topology presented in this paper uses a dedicated switch to charge the capacitor regardless of any switching cycles via an inverted buck-boost topology incorporated in the circuit and effectively reduces the inrush current problems along with accomplishing various aforementioned attributes. Section II presents the novel topology along with operation principle, various switching states and comparison table. The usefulness of the proposed topology is validated in section III via simulation and experimental results. Finally, the conclusion is presented in section IV.

II. PROPOSED TOPOLOGY AND PRINCIPLE OF OPERATION

A. Principle of operation

The proposed common-ground transformerless inverter topology utilizes a capacitor as a virtual DC bus [4]. Fig. 1 demonstrates the charging principle of the capacitor C_O which has been essentially utilized as a virtual DC bus.

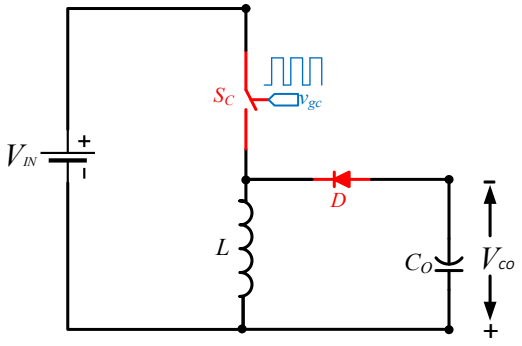

Fig. 1. Principle of operation of virtual DC bus capacitor.

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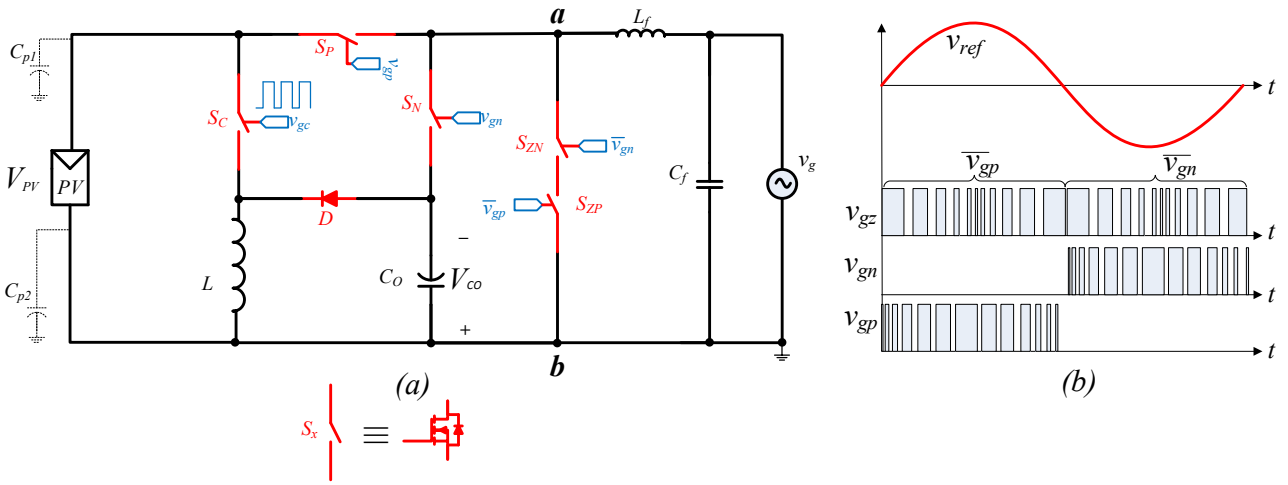

Fig. 2. (a) Proposed transformerless common ground topology and corresponding (b) Unipolar SPWM.

The capacitor is charged through an inductor by a double charging process as used in a classical buck-boost DC-DC converter. First the energy is stored in the inductor and then transferred to the capacitor in next switching cycle. This process repeats itself at a high switching frequency to maintain a constant voltage across the load, while also considering the power drain from the capacitor during the negative cycle. Additionally, the switching frequency can customize the dimensions of C_O as well as the output filter requirements.

The voltage across C_O (V_{CO}) can be expressed as follows using the volt-second balance:

$$V_{CO} = V_{IN} * \left(\frac{D}{1-D} \right) \tag{1}$$

B. Proposed topology

The proposed topology is shown in Fig. 2(a). It utilizes an inverted buck-boost topology to flexibly charge the virtual DC bus capacitor to get the required negative voltage level on the output side. A small inductor L helps to minimize the in-rush current while the charge across the capacitor C_O is governed by the duty cycle of the switch S_C. A simple PI controller can be used to maintain the voltage across the capacitor same as the input voltage so that the magnitude of voltage in the positive and negative power cycles generated by the proposed topology are equal in magnitude. The switch S_C is switched at high frequency regardless of the other switching states, hence the capacitor size can be dimensioned appropriately as desired. The capacitor C_O acts as a virtual DC bus to create the negative power cycle through switch S_N and the positive power cycle through switch S_P.

The switching pattern for the proposed inverter is based on the simple concept of the standard unipolar sinusoidal pulse-width modulation (SPWM) as shown in Fig. 2(b). This reduces the overall loss, electromagnetic interference (EMI) and output filter requirements. Additionally, the flexibility in controlling the charge across the capacitor C_O, low inrush current, common ground with the grid and reduced number of active and passive components makes this topology very attractive and versatile for grid-connected photovoltaic systems.

C. Operating States of the Proposed topology

There are four distinct operating states for the proposed topology, which repeat in each fundamental switching cycle. Each switching state is explained as follows:

(1) Positive Cycle (active): In this state, the switch S_P switches in an SPWM manner to provide the positive power cycle of the inverter output while S_C switches at a higher frequency to charge the capacitor C_O. The switching conditions of diode D depend on the switching state of S_C:

$$D = \begin{cases} 0 & for\ S_C = 1 \\ 1 & for\ S_C = 0 \end{cases} \tag{2}$$

The correct switching logic for S_C is generated by comparing the positive half of the modulation signal with the triangular carrier waveform.

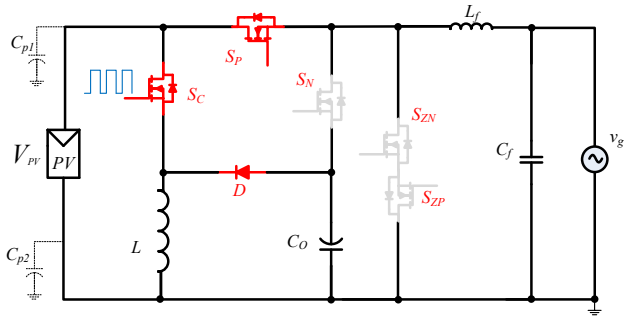

Fig. 3(a). Positive cycle (active).

Switches S_{ZP} and S_{ZN} remain off during this state along with S_N. S_{ZP} and S_{ZN} are only used to provide the zero states during the positive and negative half cycles. It can be noted that only

one switch is used in this state which leads to lower conduction losses.

(2) Positive Cycle (zero): The switches S_P and S_N are off during this state. S_{ZP} switches complimentary to S_P to provide a zero state. During this state, the body diode of S_{ZN} conducts along with the switch S_{ZP} to create a zero voltage before the filter providing free-wheeling current flow path.

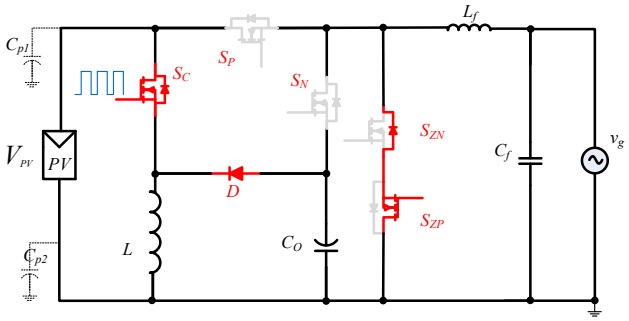

Fig. 3(b). Positive cycle (zero).

A unipolar positive voltage is created before the filter in the positive power cycle which filters out as a clean sinusoidal voltage and current. Moreover, the capacitor gets precharged during the positive power cycle, ready to be utilized in the negative power cycle.

(3) Negative Cycle (active): In this state, the switch S_N switches in an SPWM manner to provide the negative half cycle of the inverter. The correct switching sequence is generated by comparing the negative half of the modulation signal with the uni-negative triangular carrier waveform. The pre-charged capacitor C_O is utilized to create a negative polarity across the filter. This operation of C_O is also known as capacitor utilization as a virtual DC bus [4]. The conduction losses are minimal as only one switch S_N is utilized to generate the negative polarity across the filter.

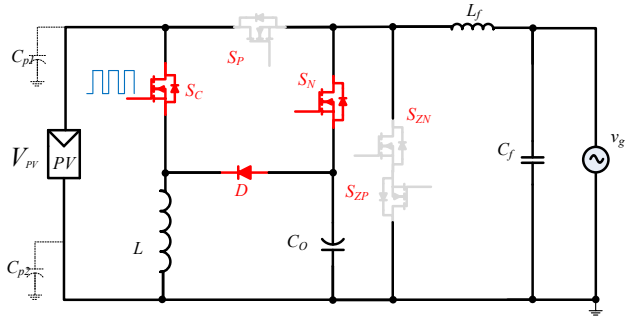

Fig. 3(c). Negative cycle (active).

(4) Negative Cycle (zero): In this state, S_{ZN} switches in a complimentary manner to S_N to provide a zero state during the negative half cycle. The body diode of S_{ZP} conducts along with S_{ZN} to provide the zero state before the filter and allow freewheeling current path. The switch S_P is off during this state and switch S_C keeps switching to maintain the voltage across C_O same as the input voltage.

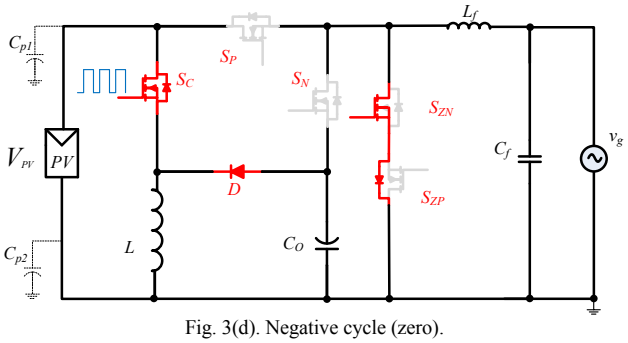

Fig. 3(d). Negative cycle (zero).

The aforementioned switching states repeat in each power cycle to produce a unipolar positive and negative voltage before the *LC* filter to produce a pure sinusoidal voltage and current to the load. The switching states can be summarized as follows in table I.

TABLE I. OPERATING MODES AND SWITCHING STATES OF THE PROPOSED TOPOLOGY

States	S_P	S_N	S_{ZP}/D	S_{ZN}/D
Positive (active)	1	0	0	0
Positive (zero)	0	0	1/0	0/1
Negative (active)	0	1	0	0
Negative (zero)	0	0	0/1	1/0

D. Comparison of proposed topology with various conventional topologies

TABLE II. COMPARISON OF PROPOSED TOPOLOGY WITH VARIOUS TRANSFORMERLESS TOPOLOGIES

Transformer-less topologies	Number of components				S in load path		V_{in} (V)	V_S (Number)	η (%)
	S	D	C*	L	+	-			
Proposed topology	5	1	2	1	1	1	400	V_{in} (2), $2V_{in}$ (3)	91.6
H5 [13]	5	0	1	0	3	3	400	$2V_{in}$ (5)	98.5
HERIC [14]	6	2	1	0	2	2	400	V_{in} (6)	97
H6 [15]	6	2	2	0	3	2	400	V_{in} (2) $2V_{in}$ (4)	97.4
Virtual DC bus [4]	5	0	2	0	2	2	400	Vin (5)	95.2
NPC three level [16]	4	2	2	0	2	2	800	V_{in} (4)	98.16
Flying capacitor [7]	4	1	2	0	2	2	400	V_{in} (4)	99.2
Siwakoti-H [8]	4	0	2	0	1	1	400	V_{in} (2) $2V_{in}$ (2)	98%

Where,

S= Number of switches,
C*= Number of Capacitors including the input capacitor
V_{in}= Input voltage for a 230 Vrms output
η= Reported efficiency
+ = Positive cycle,
- = Negative cycle.

Table II presents a detailed comparison based on several key factors associated with transformerless inverter topologies. These parameters include number of active and passive

constituent elements, switches being utilized during the provision of positive and negative power cycle, the input voltage (V_{in}) requirement for a 230 Vrms output, voltage stress (V_S) across active switches, and the reported maximum efficiency.

It can be noted that the proposed topology has the least number of switches during the provision of positive and negative power cycles, low inrush current due to the double charging process, low switching losses, low output current ripple and small filter requirements due to unipolar SPWM. Additionally, the possibility to implement the proposed topology with two industry standard half-bridge modules for better integration, cost reduction and increased power density makes this topology more versatile.

III. Simulation and Experimental Results

The simulations of the proposed topology were carried out in MATLAB-Simulink using PLECS toolbox for performance validation. The key parameters used for simulation and experimental purpose have been listed in Table III.

TABLE III. Parameters and Components for Simulation and Experimental Purposes

Parameter/Description	Value
Rated Power, P	1 kW
Input voltage, v_{in}	340 ~ 380 V
Output voltage, v_{ac}	220 ~ 240 V
Switching frequency for SPWM, f_S	20 kHz
Switching frequency for S_C	100 kHz
Line frequency	50 Hz
Load (Resistive)	48 Ω
Inductor L	0.37 mH
LC filter	0.37 mH, 2.4 µF
Virtual DC bus capacitor C_O	100 µF
Power switches	SiC MOSFET C3M0280090D

The key simulated waveforms are shown in Fig. 4 where v_{ab} denotes the chopped DC voltage before the LC filter to be filtered out as a pure sinusoidal output voltage which is indicated as v_{ac}. The output current is denoted by i_{ac} which is in phase with the output voltage. The rms value of v_{ac} is 240 V with a dc-link voltage of 380 V. The modulation index m is 0.9 and the i_{ac} is 4.4 A for a resistive load of 48 Ω. The three level voltage v_{ab} across LC filter is also shown along with the switch stress across the four switches which are modulated in an SPWM manner. It can be noted that the voltage stress across S_P and S_N is double the dc-link voltage, whereas the voltage across S_{ZP} and S_{ZN} is same as the dc-link voltage. Furthermore, the voltage across S_C, and D is also twice the dc-link voltage.

The 1 kW prototype shown in Fig. 5 was built to validate the performance of the proposed topology. The switching signals were realized via a TI C2000 peripheral Explorer Kit and the driving logic was implemented in PSIM software utilizing the SimCoder block for implementation of SPWM and generating the switching signal for S_C. The auto-code ability of PSIM was utilized to generate the switching signals. Additionally, the diode D was replaced by a SiC MOSFET to be used as a synchronous rectifier to achieve a better switching performance and an enhanced efficiency.

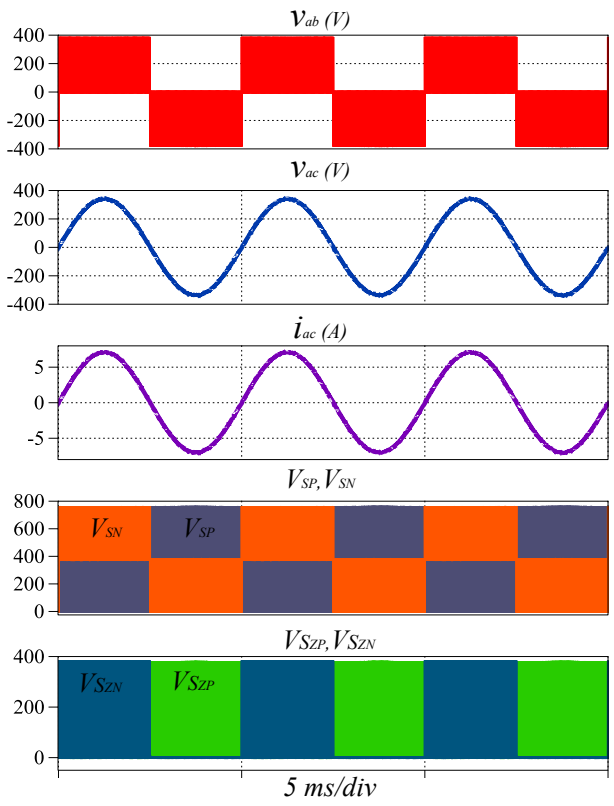

Fig. 4. Key simulated waveforms for output voltage/current, unipolar voltage across filter and switch stresses.

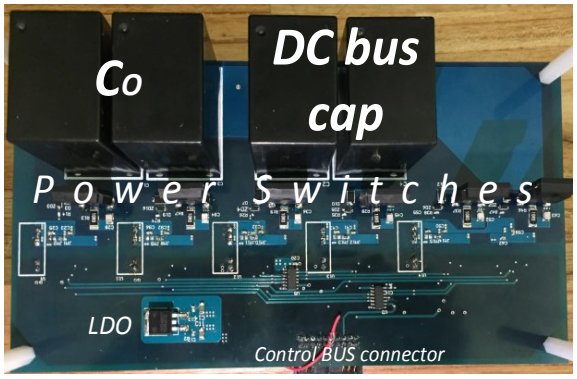

Fig. 5. 1 kW prototype of the proposed topology.

The key experimental waveforms are shown in Fig. 6 and a good match between the experimental and simulation results validates the idea of the proposed inverter topology. The switch

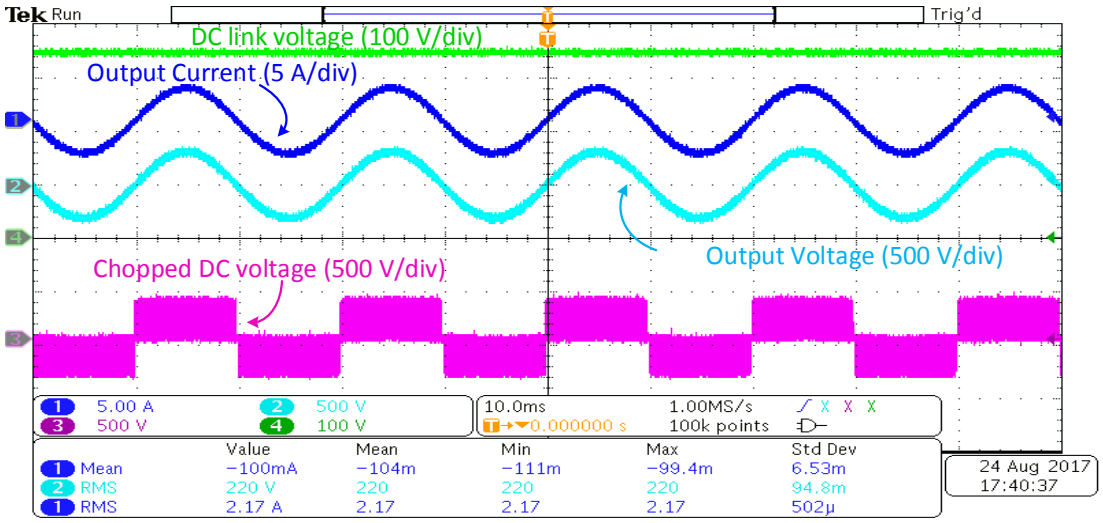

Fig. 6. Key experimental waveforms for the proposed topology.

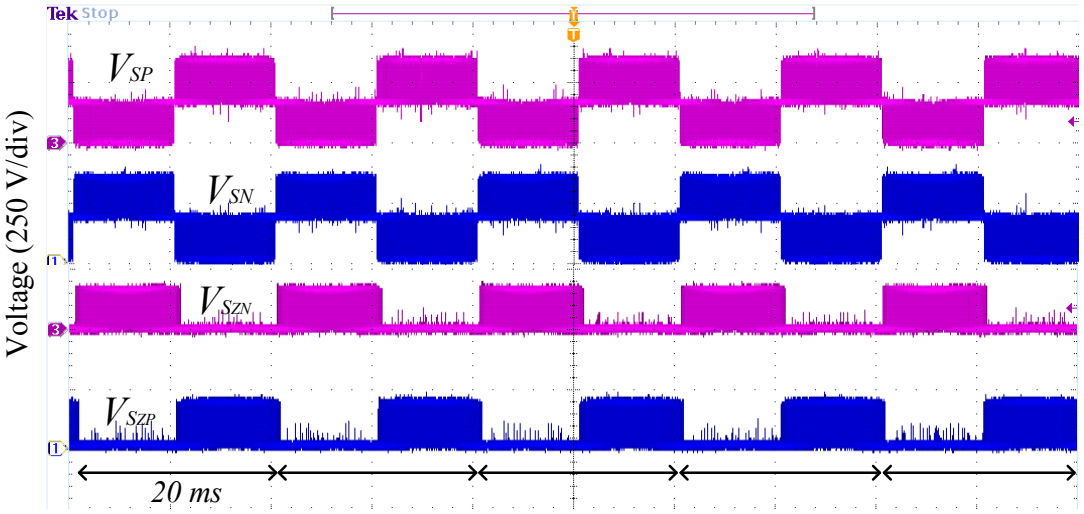

Fig. 7. Voltage stress across the power switches modulated in SPWM manner (for 110 Vrms output voltage).

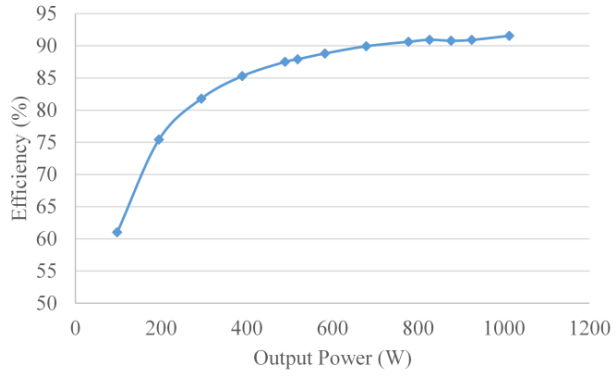

Fig. 8. Measured efficiency of the inverter at various power levels.

stress patterns are shown in Fig. 7 which are same as the simulation results. It can be noted that the output voltage is 220 V rms with a dc-link voltage of 340 V. The efficiency of the inverter was measured with a high precision power analyzer Hioki PW3390 and maximum efficiency measured was 91.6% at a load of 1012 watts. Moreover, the total harmonic distortion (THD) was measured to be < 2%. The measured efficiency of the inverter as a function of load is shown in Fig. 8 revealing increased efficiency with higher loads.

IV. CONCLUSION

This manuscript presents a novel common-ground transformerless PV inverter topology, which is based on the concept of virtual DC bus capacitor. It is charged by a double-charging process through an inductor to minimize inrush current issues in switched capacitor based power converters. The proposed topology offers minimal leakage current and a simple operation based on unipolar SPWM leads to small filter requirements, low switching losses, low EMI and low ripple in the output current. Additionally, only 1 switch is operated in the active states which helps to reduce the associated conduction

losses. The expected performance was demonstrated by a 1 kW laboratory prototype that validates the idea as being useful in grid-connected PV systems. In addition to the simple operation of the proposed converter, the design can be implemented with two industry standard half-bridge modules. This can reduce the size of the inverter, which makes it a favorable choice to be implemented as a microinverter installed on the back of a PV module.

REFERENCES

[1] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology," *IEEE Ind. Electron. Magazine*, vol. 9, no. 1, pp. 47–61, Mar. 2015.

[2] I. Patrao, E. Figueres, F. G. Espin, and G. Garcera,"Transformerless Topologies for Grid Connected Single Phase Photovoltaic Inverters," *Elsavier Renewable and Sustainable Energy Reviews*, vol. 15, pp. 3423-3431, 2011.

[3] Y. R. Kafle, G. E. Town, X. Guochun and S. Gautam, "Performance comparison of single-phase transformerless PV inverter systems," in *Proc. Appl. Power Electron. Conf. & Expo. (APEC)*, pp. 3589-3593, Mar. 2017.

[4] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li and X. He, "Transformerless inverter with virtual DC bus concept for cost-effictive grid-connected PV power systems," *IEEE Trans. Power Electron*., vol. 28, no. 2, pp. 793-805, Feb. 2013.

[5] Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," *IEEE Trans. Ind. Electron*., vol. PP, no. 99, pp. 1-1.

[6] J. F. Ardashir, Y. P. Siwakoti, M. Sabahi, Seyed Hossein Hosseini and F. Blaabjerg, "S4 grid-connected single-phase transformerless inverter for PV application," in *Proc. IEEE IECON 2016*, Florence, 2016, pp. 2384-2389.

[7] Y. P. Siwakoti and F. Blaabjerg, "A Novel Flying Capacitor Transformerless Inverter for Single-Phase Grid Connected Solar Photovoltaic System," in *Proc. 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG 2016)*, 27th – 30th of June, 2016, Vancouver, Canada.

[8] Y. P. Siwakoti and F. Blaabjerg, "H-Bridge transformerless inverter with common ground for single-phase solar-photovoltaic system," in *Proc. Appl. Power Electron. Conf. & Expo.(APEC)*, pp. 2610-2614, March, 2017.

[9] Q.-C. Zhong and W.-L. Ming, "A θ-converter that reduces common mode currents, output voltage ripples and total capacitance required," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8435–8447, Dec. 2016.

[10] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved Transformerless Inverter with Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System," *IEEE Trans. Power Electron*., vol. 27, no. 2, pp. 752–762, Feb. 2012.

[11] M. Gommeringer, F. Kammerer, A. Schmitt, M. Braun,"A Transformerless Single-Phase PV Inverter Circuit for Thin-Film or Back-Side Contacted Solar Modules," in *Proc. IECON 2014*, pp. 1148-1153, Nov. 2014.

[12] A. Kaknevicius and A. Hoover, "Application report: Managing Inrush Current" TI SLVA670A–August 2014–Revised May 2015 [Online]. Avaliable: http://www.ti.com/lit/an/slva670a/slva670a.pdf

[13] M. Victor, F. Greizer, S. Bremicker, and U. Hubler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage," U.S. Patent 7 411 802, Aug. 12, 2008.

[14] J. Ketterer, H. Schmidt, C. Siedle, "Inverter for transforming a DC voltage into an AC current or an AC voltage," Europe Patent 1 369 985 (A2), May 13, 2003.

[15] L. Zhang, K. Sun, Y. Xing, and M. Xing, "H6 transformerless full-bridge PV grid-tied inverters," *IEEE Trans. Power Electron*., vol. 29, no. 3, pp. 1229–1238, Mar. 2014.

[16] R. González, E. Gubía, J. López, and L. Marroyo, "Transformerless single-phase multilevel-based photovoltaic inverter," *IEEE Trans. Ind. Electron*., vol. 55, no. 7, pp. 2694-2702, Jul. 2008.