Auxiliary Power Supply for Medium-voltage Power Electronics Systems

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***Abstract*— This paper presents an auxiliary power supply for medium-voltage (MV) power electronics systems, based on modular multilevel series-parallel converter (MMSPC). The converter connects to 2.4 kV RMS at the input, and produces 24 V dc at the output, providing 100 W of power with 10 kV isolation. Unlike the traditional solutions which use a grid-frequency bulky and heavy potential transformers, the proposed converter can operate at higher switching frequencies, thus reducing the weight and providing higher power density, compared to the traditional approach. Additionally, the proposed converter features an internal capacitor voltage balancing and achieves power factor correction (PFC) by using predictive control. The proposed converter is simulated and its operation is experimentally validated on the developed prototype at low input voltage.**

Keywords—auxiliary power supply, medium voltage, multilevel converter, rectifier, SiC MOSFET

I. INTRODUCTION

The most challenging requirement for an auxiliary power supply in a medium-voltage (MV) power converter system, such as [1] is to provide a high step-down ratio and high isolation in a reasonably simple and cost effective way. Typically, two different approaches are used to meet those requirements [2]. The first approach relies on using a low-frequency (50/60 Hz) potential transformer which is connected directly to the MV grid. Although reliable and simple, the main disadvantage of this system is its size and weight (the 2,400/120 V transformer weighs almost 30 lb.), and a more compact solution would be preferred if the overall system power density is paramount. The other approach makes use of a dc voltage already present in the system, such as dc bus voltage or the voltage across one of the system capacitors. This approach brings the advantages of reduced weight and size. Most papers discuss an application of standalone high-step-down dc/dc converters as power supplies for MV systems [3]-[7]. In [3], a flyback converter with a high-voltage (4,000 V) Si MOSFET (IXTF1N400) and a commercial controller was supplied from a 1600 V dc source, and provided 72 W at 24 V output, with 78.3% efficiency. However, the single-flyback approach cannot be used at higher voltage levels due to the high voltage requirements for the used transistor. To overcome this issue at high input dc voltage, the multilevel approach based on flyback converter is used in [4]-[6], and a tapped-inductor buck converter is presented in [7]. A modular multilevel series-parallel converter (MMSPC) topology is investigated in [8] and [9]. The MMSPC topology, which is a generalization of the traditional MMC topology, allows not only series but also parallel connections among modules. The main advantages of MMSPC are that the balancing of the modules' voltage can be achieved without having to sense those voltages, and that each MMSPC switch can have half of the current rating of a MMC switch. The modular approach of MMSPC and advantages of intrinsic balancing of its modules' voltage is utilized to develop an auxiliary power supply presented in this paper. The basic idea, from which the proposed converter is derived, is shown in Fig. 1.

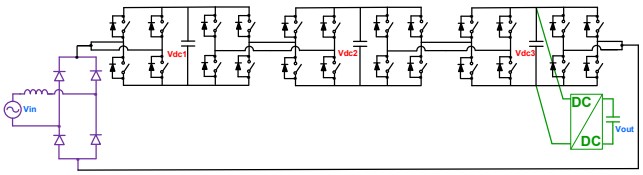

Fig. 1. Basic idea of using a MMSPC as an auxiliary power supply in a medium voltage system.

Additionally, the proposed converter features an internal capacitor voltage balancing and requires only one dc-link voltage sensor to perform the required control. However, even though in this application (a 100 W auxiliary power supply) the input current is relatively small, the concept of the power factor correction (PFC) should be introduced in order to get unity power factor (PF) and a low total harmonic distortion (THD) of the input current. For this reason, a predictive PFC control algorithm is introduced for this topology and described in detail. The proposed converter is simulated and validated by experiments on the developed prototype with off-the-shelf 1.7 kV Silicon Carbide (SiC) devices.

II. TOPOLOGY CONSIDERATIONS AND CONTROL STRATEGY

A. Topology consideration: AC/DC stage

Although conventional MMSPC is capable of bidirectional operation [8], [9], its application as a power supply requires only unidirectional power flow: from the HV ac input to the dc output. As shown in Fig. 2 (a) and (b), this means that only bypass connection, parallel connections and series connection with negative polarity can be used in this application. This allows us to substitute some of the MOSFETs by diodes, as shown in Fig. 2 (b). Further, it can be noticed that some of the

devices would always stay in the ON state, while some would always remain in the OFF state. Those that would stay in the ON state (marked yellow in Fig. 2 (b)) can be replaced by a short circuit, whereas those that would always remain OFF (marked green in Fig. 2 (b)) can be completely removed from the circuit. Additionally, some MOSFETs (marked red in Fig. 2 (b)) can be replaced by diodes, since they need to conduct only when their body diodes would naturally conduct (i.e. in the absence of the gate signal). This would further simplify the circuit (as shown in Fig. 2 (c)), which could then be rearranged as shown in Fig. 2 (d).

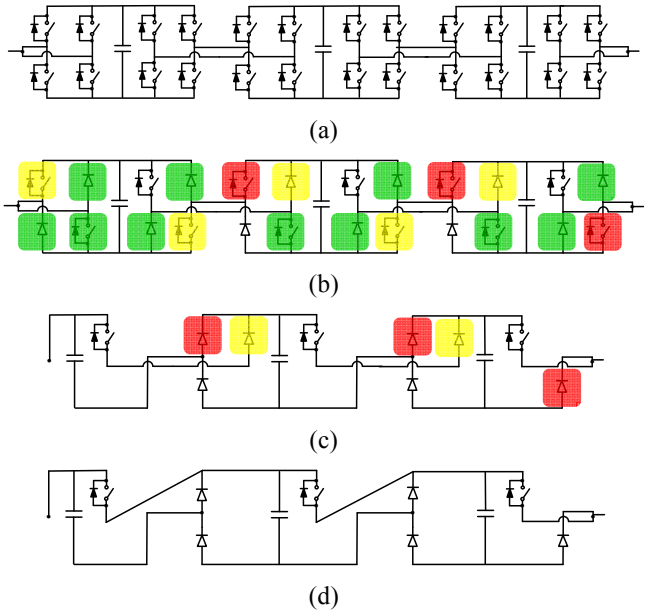

Fig. 2. (a) Conventional MMSPC topology with 3 modules, (b) MOSFETs substituted by diodes due to the unidirectional operation, (c) Circuit further simplified by shorting the devices in the permanent ON state and removing the devices in the permanent OFF state, and (d) Rearranged circuit from (c)

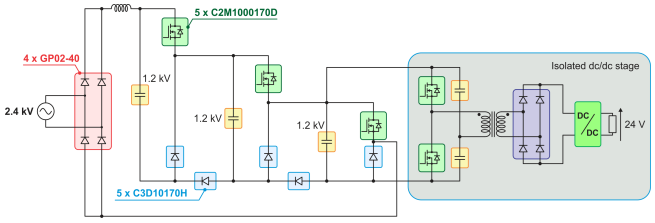

Fig. 3. Proposed auxiliary power supply topology based on MMSPC converter.

The ac/dc part of the proposed converter in Fig. 3 has similar topology as switched capacitor (SC) converter from [10]-[12], but differs in the way the series/parallel connections are achieved, as well as in the modulation strategy. The proposed topology is fully scalable and can adapt to higher MV input voltage by simply increasing the number of series-connected modules. As shown in Fig. 3, an additional isolated dc/dc stage is necessary in order to produce the required constant dc output voltage.

B. Operating principle

Depending on the states of the S1, S2 and S3, the proposed converter can produce 0V, 1xVbus, 2xVbus, or 3xVbus at the left hand side of the input inductor by connecting the dc bus capacitors in series or in parallel, as shown in Fig. 4. The Table I lists four different operating modes that can be achieved by the proposed converter. The parallel connection of modules (dc bus capacitors) can be used to improve the dc-link voltages balancing and only one dc-link voltage sensor is required (at the C3 in Fig. 4(a)). No other balancing control is necessary.

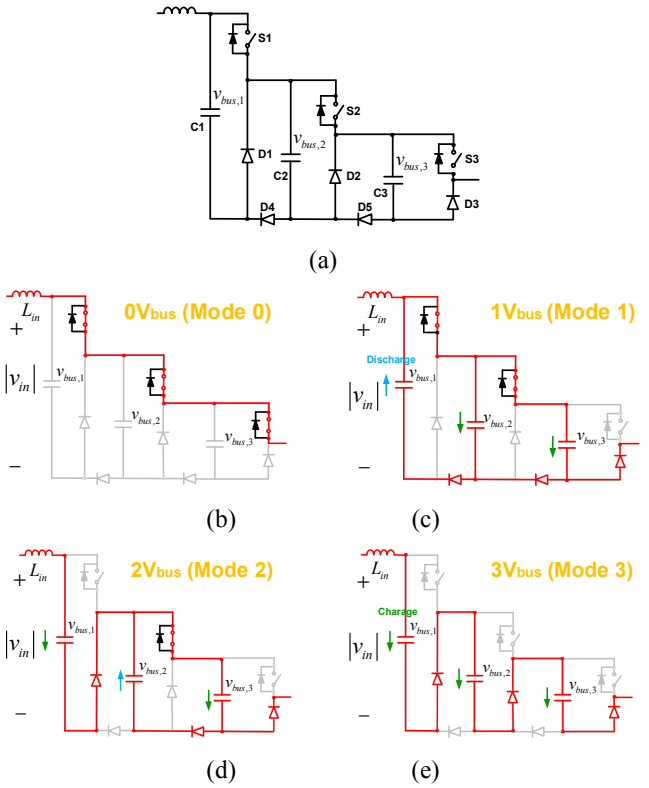

Fig. 4. Operating modes of the modified MMSPC converter: (a) converter topology, (b) 0Vdc (Mode 0 – bypass connection); (c) 1Vdc (Mode 1 – parallel connection on all modules; (d) 2Vdc (Mode 2 – series connection followed by parallel connection); (e) 3Vdc (Mode 3 – series connection of all modules).

TABLE I. BALANCING EFFECT ACCORDING TO SWITCHING STATE

Mode	Switching state	Balancing effect	Composed voltage
0	(1, 1, 1)	-	$0V_{bus}$
1	(1, 1, 0)	$V_{bus,1}$, $V_{bus,2}$, $V_{bus,3}$	$1V_{bus}$
	(1, 0, 1)	$V_{bus,1}$, $V_{bus,2}$	
	(0, 1, 1)	$V_{bus,2}$, $V_{bus,3}$	
2	(1, 0, 0)	$V_{bus,1}$, $V_{bus,2}$	$2V_{bus}$
	(0, 1, 0)	$V_{bus,2}$, $V_{bus,3}$	
	(0, 0, 1)	-	
3	(0, 0, 0)	-	$3V_{bus}$

TABLE II. OPERATING REGIONS AND CORRESPONDING MODES OF THE PROPOSED CONVERTER TOPOLOGY

Range	Duty	Mode	Current Ripple slope	
Region 1 $\lvert v_{in}\rvert < V_{bus}$	$\frac{2}{3} \le d < 1$	Mode 0,1	$up: \frac{\lvert v_{in}\rvert}{L}$	$down: \frac{\lvert v_{in}\rvert - v_{bus}}{L}$
Region 2 $V_{bus} < \lvert v_{in}\rvert < 2V_{bus}$	$\frac{1}{3} \le d < \frac{2}{3}$	Mode 1,2	$up: \frac{\lvert v_{in}\rvert - v_{bus}}{L}$	$down: \frac{\lvert v_{in}\rvert - 2v_{bus}}{L}$
Region 3 $2V_{bus} < \lvert v_{in}\rvert < 3V_{bus}$	$0 \le d < \frac{1}{3}$	Mode 2,3	$up: \frac{\lvert v_{in}\rvert - 2v_{bus}}{L}$	$down: \frac{\lvert v_{in}\rvert - 3v_{bus}}{L}$

The equations that describe the input inductor's current slope in each of the 4 modes illustrated in Fig. 4 are presented in Table II. Due to the interleaved PWM scheme applied in this case, there are three distinct regions of the input voltage and three intervals of duty cycle d in which only certain operating modes can be applied, as shown in Table II.

Region 1: In this region, the equivalent circuit is changing between Mode 0 and Mode 1 (see Fig. 4(b) and (c)). This means that the converter have all bypass connections or all parallel connections. In Mode 0, due to the all bypass connections, the inductor sees a positive voltage $\lvert v_{in}\rvert$, resulting in increasing inductor current. On the other hand, in mode 1, the inductor sees the negative voltage of $\lvert v_{in}\rvert - v_{bus}$ (because $\lvert v_{in}\rvert$ is lower than v_{bus}). In this mode, the inductor current decreases. Even though Mode 1 can have switching states other than (1,1,0) shown in Fig. 4(c), all these states would produce the same inductor current ripple and can be described by the following two equations:

$$\Delta i_{L\_up} = \frac{\lvert v_{in}\rvert}{Lf_s}\left(d - \frac{2}{3}\right) \tag{1}$$

$$\Delta i_{L\_down} = \frac{v_{bus} - \lvert v_{in}\rvert}{Lf_s}(1-d) \tag{2}$$

where d is the duty cycle and f_s is the switching frequency.

Region 2: In this region, the modules' connections are changing between Mode 1 and Mode 2 (see Fig. 4(c) and (d)). In Mode 2, the inductor sees a negative voltage of $\lvert v_{in}\rvert - 2v_{bus}$, resulting in decreasing of the inductor current. In this region, the inductor current ripple can be described by the following two equations:

$$\Delta i_{L\_up} = \frac{\lvert v_{in}\rvert - v_{bus}}{Lf_s}\left(d - \frac{1}{3}\right) \tag{3}$$

$$\Delta i_{L\_down} = \frac{2v_{bus} - \lvert v_{in}\rvert}{Lf_s}\left(\frac{2}{3} - d\right) \tag{4}$$

Region 3: In this region, the modules' connections are changing between Mode 2 and Mode 3 (see Fig. 4(d) and (e)). The analysis of Mode 2 is same as Region 2. In Mode 3, the inductor sees a negative voltage of $\lvert v_{in}\rvert - 3v_{bus}$. In this region, the inductor current ripple can be described by the following two equations:

$$\Delta i_{L\_up} = \frac{\lvert v_{in}\rvert - 2v_{bus}}{Lf_s} d \tag{5}$$

$$\Delta i_{L\_down} = \frac{3v_{bus} - \lvert v_{in}\rvert}{Lf_s}\left(\frac{1}{3} - d\right) \tag{6}$$

C. Control strategy: Predictive control

In this section, the predictive control approaches proposed in [14] and [15] are evaluated as potential candidates for the converter's PFC control. The control objective was to make the system stable and its operation unaffected by the mode change and the accompanying problems at mode change transitions due to the noise and input current sensor resolution. The prediction paths for the two considered approaches are illustrated in Fig. 5.

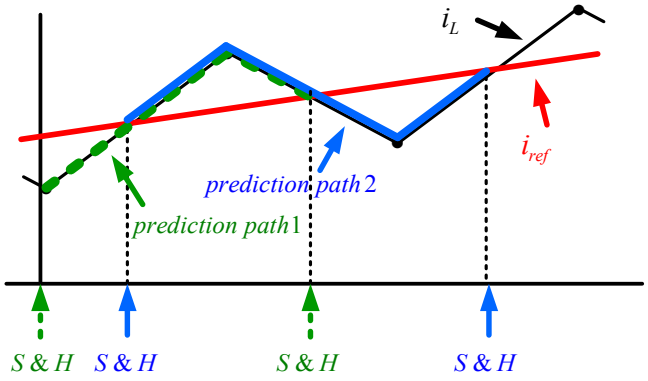

Fig. 5. The considered prediction paths: a prediction path 1 [14], and a prediction path 2 [15].

Prediction path 1 [14] (green dotted line in Fig. 5) can be expressed with the following equation:

$$i_L(n) + \Delta i_{L\_up} - \frac{1}{2}\Delta i_{L\_down} = i_{ref}(n+1) \tag{7}$$

Considering the region 1 and substituting (1) and (2) into (7), we could derive duty cycle $d_1(n)$ in Region 1 as a function of input voltage, bus voltage, inductor current, inductance, sampling time, and current reference:

$$d_1(n) = \frac{2L}{T_s}\frac{i_{ref}(n+1) - i_L(n)}{\lvert v_{in}\rvert + v_{bus}} + \frac{3v_{bus} + \lvert v_{in}\rvert}{3\left(\lvert v_{in}\rvert + v_{bus}\right)} \tag{8}$$

Similarly, $d_2(n)$ and $d_3(n)$ could be obtained as follows:

$$d_2(n) = \frac{2L}{T_s}\frac{i_{ref}(n+1) - i_L(n)}{\lvert v_{in}\rvert} + \frac{2v_{bus}}{3\lvert v_{in}\rvert} \tag{9}$$

$$d_3(n) = \frac{2L}{T_s}\frac{i_{ref}(n+1) - i_L(n)}{\lvert v_{in}\rvert - v_{bus}} + \frac{3v_{bus} - \lvert v_{in}\rvert}{3\left(\lvert v_{in}\rvert - v_{bus}\right)} \tag{10}$$

As can be seen from Fig. 6 and equations (8-10), the trajectories of the duty cycle are different in different regions and the region detection is needed in this approach. Moreover, the applied duty cycle envelope shows distortion compared to the ideal sinusoidal reference.

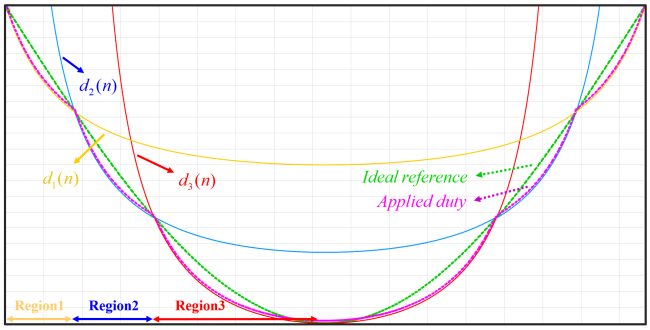

Fig. 6. Prediction path 1 requires region detection: duty cycles in different operating regions and the ideal duty cycle.

Prediction path 2 [15] (blue solid line in Fig. 5) can be expressed with the following equation:

$$i_L(n)+\Delta i_{L\_up}+\Delta i_{L\_down}=i_{ref}(n+1) \tag{11}$$

Considering the region 1 and substituting (1) and (2) into (11), a duty cycle $d_1(n)$ in Region 1 can be derived as a function of input voltage, bus voltage, inductor current, inductance, sampling time, and current reference:

$$i_L(n)+\frac{|v_{in}|}{Lf_s}\left(d_1-\frac{2}{3}\right)-\frac{v_{bus}-|v_{in}|}{Lf_s}(1-d_1)=i_{ref}(n+1) \tag{12}$$

$$d_1\left(\frac{|v_{in}|}{Lf_s}+\frac{v_{bus}-|v_{in}|}{Lf_s}\right)=i_{ref}(n+1)-i_L(n)+\frac{2|v_{in}|}{3Lf_s}+\frac{v_{bus}-|v_{in}|}{Lf_s} \tag{13}$$

$$d_1\left(\frac{v_{bus}}{Lf_s}\right)=i_{ref}(n+1)-i_L(n)+\frac{2|v_{in}|+3v_{bus}-3|v_{in}|}{3Lf_s} \tag{14}$$

$$d_1=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L}{T_s}+\frac{3v_{bus}-|v_{in}|}{3v_{bus}} \tag{15}$$

In region 2, the duty cycle can be obtained by substituting (3) and (4) into (11):

$$i_L(n)+\frac{|v_{in}|-v_{bus}}{Lf_s}\left(d_2-\frac{1}{3}\right)-\frac{2v_{bus}-|v_{in}|}{Lf_s}\left(\frac{2}{3}-d_2\right)=i_{ref}(n+1) \tag{16}$$

$$\begin{aligned} &d_2\left(\frac{|v_{in}|-v_{bus}}{Lf_s}+\frac{2v_{bus}-|v_{in}|}{Lf_s}\right)= \\ &=i_{ref}(n+1)-i_L(n)+\frac{|v_{in}|-v_{bus}}{3Lf_s}+\frac{2}{3}\left(\frac{2v_{bus}-|v_{in}|}{Lf_s}\right) \end{aligned} \tag{17}$$

$$d_2\left(\frac{v_{bus}}{Lf_s}\right)=i_{ref}(n+1)-i_L(n)+\frac{|v_{in}|-v_{bus}+4v_{bus}-2|v_{in}|}{3Lf_s} \tag{18}$$

$$d_2=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L}{T_s}+\frac{3v_{bus}-|v_{in}|}{3v_{bus}} \tag{19}$$

Finally, in Region 3, the duty cycle can be obtained by substituting (5) and (6) into (11):

$$i_L(n)+\frac{|v_{in}|-2v_{bus}}{Lf_s}d_3-\frac{3v_{bus}-|v_{in}|}{Lf_s}\left(\frac{1}{3}-d_3\right)=i_{ref}(n+1) \tag{20}$$

$$\begin{aligned} &d_3\left(\frac{|v_{in}|-2v_{bus}}{Lf_s}+\frac{3v_{bus}-|v_{in}|}{Lf_s}\right)= \\ &=i_{ref}(n+1)-i_L(n)+\frac{3v_{bus}-|v_{in}|}{3Lf_s} \end{aligned} \tag{21}$$

$$d_3=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L}{T_s}+\frac{3v_{bus}-|v_{in}|}{3v_{bus}} \tag{22}$$

Finally, it is evident that equations (15), (19) and (22) are identical, i.e. one equation can be used in all operating regions and no region detection is necessary:

$$\therefore d=d_1=d_2=d_3=\frac{i_{ref}(n+1)-i_L(n)}{v_{bus}}\frac{L}{T_s}+\frac{3v_{bus}-|v_{in}|}{3v_{bus}} \tag{23}$$

The first term in (23) is a dynamic component which regulates the current at switching frequency. The second term is a static component which is related to the operating point of the converter where variables vary at line frequency. Based on the equation (23), a predictive control is implemented with conventional PI voltage controller and Second Order Generalized Integrator (SOGI) PLL algorithm [16], as shown in Fig. 7. As can be seen from Fig. 7, only one capacitor voltage (V_{bus3}) needs to be sensed, since the topology can utilize the modes with capacitors in parallel to keep the capacitors' voltages well balanced. The sampling is done at the effective switching frequency $f_{S/H}=f_{sw,effiecive}=N\times f_{sw}$, where N is the number of modules. The applied phase shift is:

$$phase\,shift=\frac{2\pi}{N} \tag{24}$$

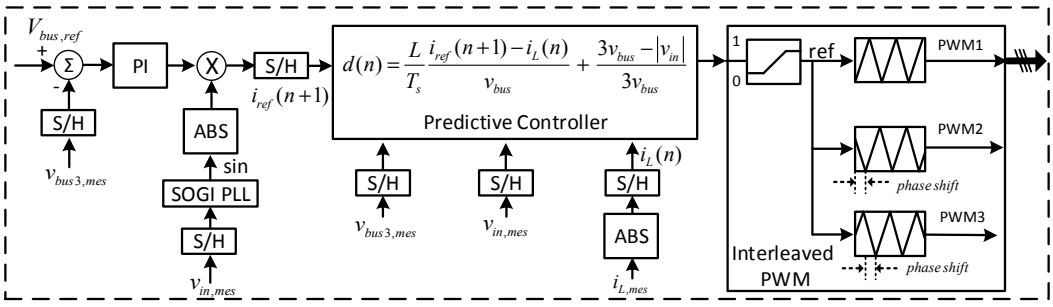

Fig. 7. Predictive control block diagram

D. DC/DC stage and startup principle

A 1200/24V isolated dc/dc converter is built based on a standard isolated half-bridge (HB) converter topology, as shown in Fig. 8. The transformer is made using nanocrystalline vitroperm 500F core, with 190:13:6 turns in primary, secondary and tertiary windings respectively. The transformer was tested for isolation at 10 kV dc, which is applied for 10 minutes between each combination of the windings. The UCC21520DW gate driver was used to drive 1700V, 5A, SiC MOSFETs, C2M1000170D.

Primary side was operating in open loop and a switching regulator is used at the secondary side. The tertiary winding was used for supplying power to the local control circuit and the gate driver after the startup transient is finished. Since during the startup the tertiary winding is not energized yet, a startup circuit needs to act as a temporary power supply until the tertiary circuit is energized. Once the voltage of C4 reaches a certain value, the startup circuit begins to discharge C4 and deliver suitable voltage level to tertiary circuit. When a stable 5V is sensed at the output of the dc/dc converter in tertiary circuit (Fig.8), a normally-closed solid-state relay disconnects startup circuit from C4.

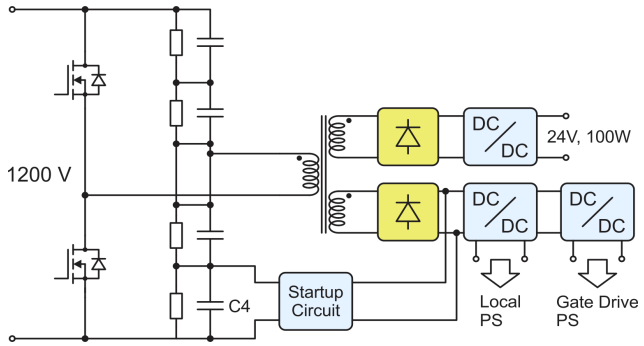

Fig. 8. Detailed configuration of the dc/dc stage

III. Simulation and Experimental Results

In order to validate the control approach, the simulations of the input stage are done in PLECS and the results are shown in Fig. 9. The converter efficiency is simulated in PLECS using the developed component thermal models, and the system loss breakdown is shown in Fig. 10. Figure 11 illustrates the advantages of the proposed system in terms of size and weight reduction, compared to the traditionally used potential transformer.

The experiments were carried out on the realized prototype converter, shown in Fig. 12. The converter operating values and used active and passive components are listed in Table III. The experiments are performed separately for the ac/dc and dc/dc stages. Due to the limitations in the input voltage measurement circuit of the ac/dc stage, the experimental results for the input stage are obtained only at very low input voltage, as shown in Figs. 13 and 14. The output stage was tested at full voltage and power and the waveforms are shown in Fig. 15.

As can be seen in Fig. 13, the PFC control performs well, with the achieved input current THD of 8.13%. Also, the capacitor voltages are well balanced, as shown in Fig. 14.

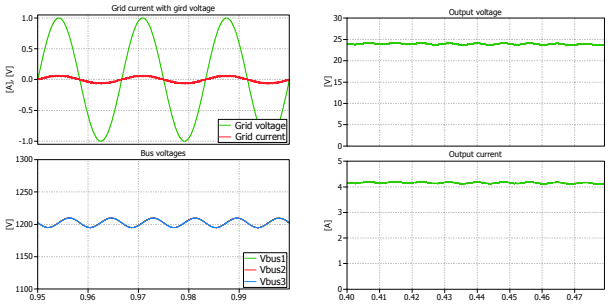

Fig. 9 Steady state response of the system, with 2400 V ac at the input and 24 V dc at the output, supplying 100 W to the resistive load.

Vin=2400 Vac, Vout=24 Vdc, Pout=100 W, Lin=1.5 mH, Ta=25 °C

Losses [W]

Input Rect.	Inductor	AC/DC Semiconductors (50kHz)	Transformer	DC/DC HB (100kHz)	Output Rect.
0.29	0.0077	2.56	0.42	0.98	7.86

Total losses [W]	12.12
Output power [W]	97.92
Efficiency [%]	90.7

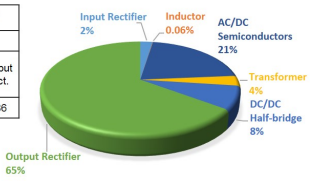

Fig. 10. Simulated system efficiency and power loss breakdown.

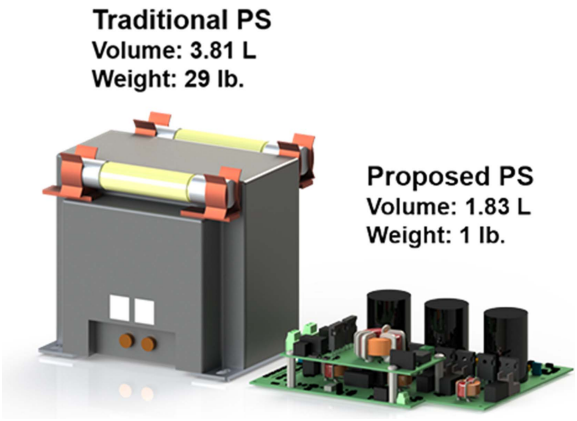

Fig. 11. 3D rendering of the proposed system compared to the traditional solution with potential transformer.

TABLE III. Parameters and Components

Parameter	Value	Component	Part number
v_{in} (Input voltage)	2400 V	$C_1 = C_2 = C_3$ (dc link cap)	UNL15W4P7K
v_o (Output volage)	24 V	SiC MOSFETs	C2M1000170D
P_o (Ouput power)	100 W	SiC Diodes	C3D10170H
L_{in} (Input inductor)	1.5 mH	Input Rectifer Diodes	GP02-40
f_{sw} (Switching frequecny, ac/dc)	50 kHz	Ouput Rectifer Diodes	CDBC5100-G
f_{sw} (Switching frequecny, dc/dc)	100 kHz	Input Current Sensor	LA 55

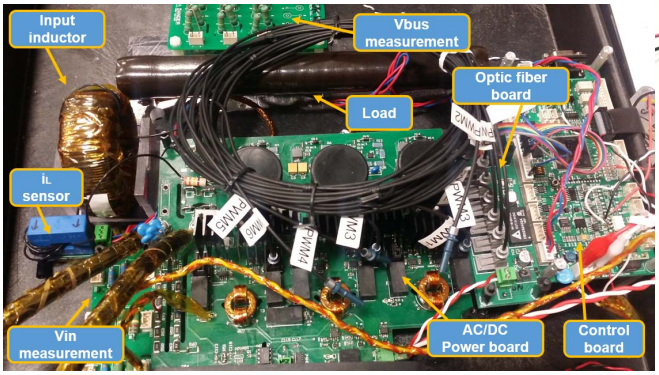

Fig. 12. The experimental setup: (left) ac/dc part of the system, (right) dc/dc part of the system.

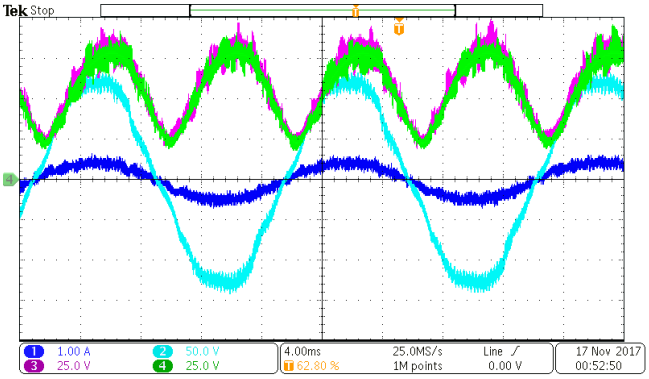

Fig. 13. Converter input voltage and current with predictive control applied. CH1: input current; CH2: input voltage; CH3: first bus capacitor voltage; CH4: third bus capacitor voltage.

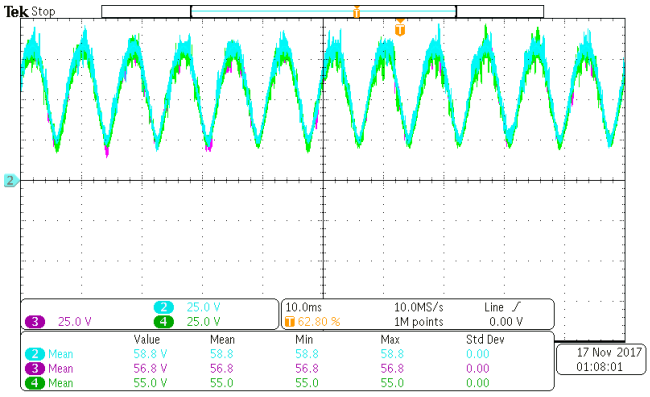

Fig. 104. DC-link voltages with predictive control applied. CH2: first bus capacitor voltage; CH3: second bus capacitor voltage; CH4: third bus capacitor voltage.

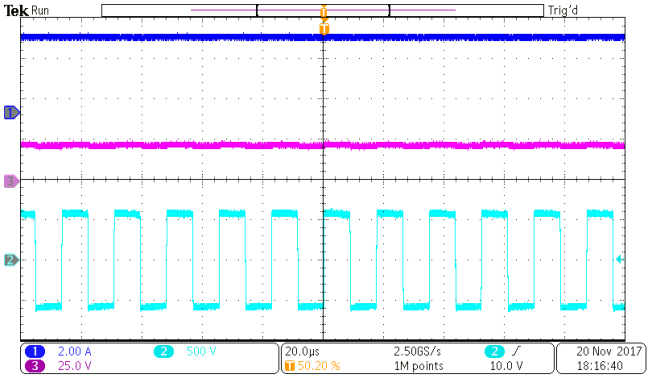

Fig. 15. The experimental results for the dc/dc stage, with 1.2 kV at the input and 24 V at the output, supplying 100 W to the resistive load. CH1: output current; CH2: output voltage; CH3: transformer primary voltage.

IV. Conclusion

This paper has presented an auxiliary power supply for medium-voltage power electronics systems, based on modular multilevel series-parallel converter. The proposed converter does not require the operating region detection to perform the required predictive control, and no additional balancing algorithm is necessary due to the internal balancing effect. The topology can be scaled-up to support commonly used MV distribution voltages. The effectiveness and performance of the proposed topology have been verified by simulations, and by experiments at reduced input voltage.

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