Controller and EMI filter design for Modular Front-End Solid-State Transformer

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***Abstract*—This paper discusses the details of the control scheme and EMI filter design for a modular front-end solid-state transformer (SST). The multi-cell configuration is achieved by connecting the active-front-end (AFE) cells in series, with the voltage from the MV evenly distributed among the cells. The isolated outputs of the dc-dc converters are tied in parallel. The EMI filter is designed to reduce line impedance and switching noise. Simulations showed the EMI filter reduced noise below FCC Class A standards. The SST controller consists of a voltage controller, current controller, and a phase lock loop (PLL) with an ideal duty feedforward. The implementation of these subsystems is explained and its integration in the system is shown. The results show that at low voltage level, the input current waveform is nearly sinusoidal.**

Keywords—SST, EMI filter, medium voltage

I. INTRODUCTION

Solid-state transformers (SSTs) are one of the leading edge subjects in today's power electronics development. SSTs are connected to medium voltage (MV) lines and are galvanically isolated with transformers that operate at high-frequency, whereas traditional power transformers operate at low-frequency. As a result, SSTs have operational flexibility via the controller, whereas conventional transformers simply provide isolation and voltage level conversions. The intelligent universal transformer (IUT) incorporates smart functions into a SST for utility applications, with features that have been proven with hardware implementation [1-4]. For our SST, commercially available 1.2-kV LV SiC devices are connected in series to achieve high voltage blocking capabilities. Although HV SiC devices demonstrated better performance when compared to HV Si devices in terms of increased voltage rating and switching speed [5, 6], none of these SiC devices are offered commercially at the moment. Besides, noise induced by the high voltage slew rate (dv/dt) from common mode coupling can impact the circuit's intended function and possibly require substantial switching speed reduction to allow for reliable operation. The purpose of this paper is to explain the control scheme and to show the performance of the SST. Power factor correction circuits (PFCs) have a similar control scheme [7-9], but are neither MV level capable nor modular in design. Typically, PFCs use an analog controller in smaller applications, or a digital processor with a fast sampling frequency, so the impacts of delays are not as severe compared to an SST. In this paper, the input voltage harmonic measurement has been showed under full voltage condition, and EMI filter was designed. The proposed controller is design to reduce the input distortion under delayed system. The implementation of these subsystems is explained and its integration in the system is shown.

II. SYSTEM CONFIGURATION

A. Circuit topologies

The complete MV front-end converter consists of three stages: (1) diode rectification, (2) power factor correction (PFC) boost converter, and (3) isolated dc-dc converter. The top portion of Fig. 1 is the block diagram of a 7.2-kV front-end converter, which consists of 20 modules with the individual module circuit diagram shown in the bottom portion of Fig. 1. The input side of each module is connected in series, and the output side of each module is connected in parallel. If the devices and components of the individual modules are well matched, the paralleled outputs will force the input side power, and thus the voltage sharing to be balanced.

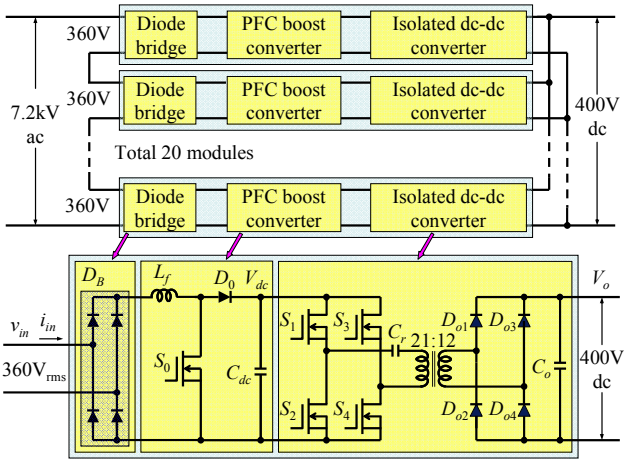


Fig. 1. Block diagram of 7.2-kV modular front-end converter using 20 modules and the circuit configuration of individual modules.

Considering the off-the-shelf power semiconductor devices, 1200-V rated SiC power MOSFETs and Schottky diodes are the most suitable and readily available at different current ratings. In this 7.2-kV input example, the number of modules is selected to be 20, and thus the input voltage for each module is

360 V rms or 509 V peak. To accommodate the typical utility grid voltage variation (10%) and the boost converter output voltage margin (25%), the dc bus voltage is 700 V, which is still well below 1200 V and should allow small mismatch of devices and components among all 20 modules.

To reduce the number of components, a 3-level ac-dc boost converter is proposed to replace the above PFC stage. Fig. 2 shows the block diagram of the proposed modular 3-level front-end configuration and the circuit diagram of the individual module. The subsequent high-frequency isolated dc-dc converter is a half-bridge type LLC resonant converter. Using the 1200-V devices, the dc bus voltage for individual boost converter remains 700 V, but for the overall three-level dc bus, it becomes 1400 V. The input voltage of the diode bridge is then doubled at 720 V rms for the 7.2-kV MV input. Therefore the total number of module becomes 10. This allows significant reduction on the interconnection between modules.

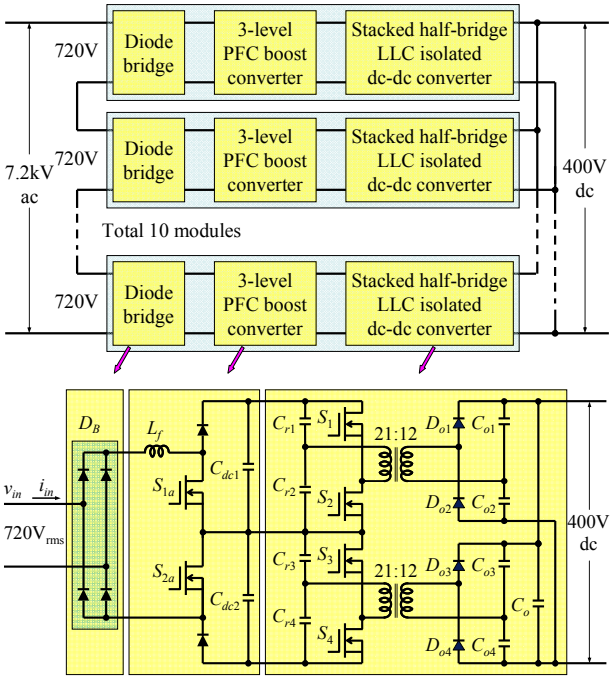


Fig. 2. Block diagram of 7.2-kV modular 3-level front-end converter using 10 modules and the circuit configuration of individual modules.

Notice that for the rectifying diode bridge DB, a relatively slow reverse recovery type diode can be used. Therefore a high-voltage rated silicon diode module can be used. The dc-dc converter is a half-bridge LLC based converter. The switches of the input side half-bridge circuit are the same SiC MOSFET used in the PFC boost stage. High-frequency rated polypropylene film capacitors are used as the resonant capacitor. The secondary diode bridge nominal voltage output is 400-V dc, which can be adjusted to 380 V for data center or 500 V for EV fast charger applications. The two boost converters of the three-level PFC circuit are interleaving to reduce the switching current ripple. In addition, all 10 modules are phase-shifted to further reduce the input current ripple.

The input series and output parallel structure tends to suffer from balancing problem under no-load condition. To solve this problem, two main approaches were taken. The first approach is to construct high frequency transformers uniformly with consistent leakage and magnetizing inductances. The second approach is to supply the auxiliary power by the 400-V output bus. With well-uniformly constructed high frequency transformers, the input voltage sharing can be balanced with a small loading coming from the auxiliary power that supplies gate drives, sensors, control, and optical fiber interface circuits, which sums to about 100-W for the complete front-end boost converter stage. The proposed combined stage with integration of front-end ac-dc and isolated dc-dc was designed in a configuration that allows simple stacking for the increased voltage level

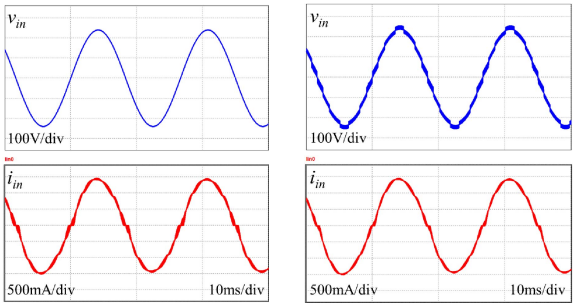
B. The new control board:PWM delay reduction

In order to generate multiple PWM signals, the previous version of our IUT uses a CPLD. The previous DSP used was a TI TMS320F28335 that did not have enough PWM outputs. The CPLD was used to transfer the interleaved signals using a delay. As a result, the closed loop of the system had an additional CPLD delay, resulting in poor control performance due to reduced phase margin. The new control board has been developed in house using a TI TMS320F28377D DSP, which has 12 PWM output ports. The outputs of DSP are connected directly to fiber optic transmitters, which then feed signals to the individual stages without incurring the CPLD delay.

III. INPUT EMI FILTER DESIGN

A. Line impedance effect and measurement

A PWM output generates a large amount of noise in the line's voltage and current when a line impedance exists. Line impedance appears in both the line cable and the line transformer. There is magnetizing and leakage inductance present in the transformer, with the leakage inductance connected in series. As a result, the leakage inductance has a critical effect on noise.



(a) Ideal voltage source (b) Source with line impedance

Fig. 3. Simulation comparison of line impedance effect.

Fig. 3. shows the effects of line impedance through simulation. In Fig. 3(a), the ideal voltage source does not have switching ripple, however a voltage source with 0.5mH line impedance has a switching ripple as shown in Fig. 3(b). In order to attenuate the switching noise, filters are necessary.

B. *EMI filter design and Damping method*

Typically an EMI filter consists of an inductor and capacitor. Line impedance is unavoidable, so it can be used as the inductor of an LC EMI filter. A inductor with high voltage isolation is big and expensive, so using the line impedance is advantageous. However, a LC filter with line impedance can interact with the SST when an undamped filter is connected to the input port. A simple damping resistor can solve this problem, but excessive power dissipation across the damping resistor and voltage isolation is an issue. A paralleled RC setup can be a better solution for damping and loss reduction.

Fig. 4. Photograph of the modular multilevel front-end converter under testing.

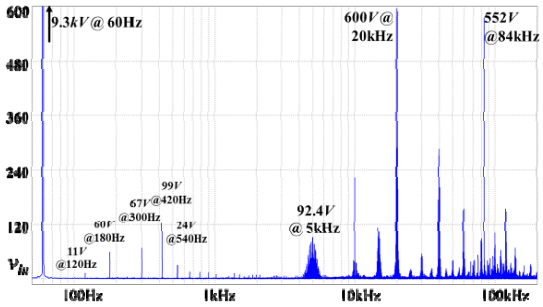


Fig. 5. Frequency analysis of 6.6kV line voltage without filter under testing.

Fig. 4 shows a photograph of the entire modular multilevel front end and the LLC dc-dc stage. The overall size of this setup is 6-ft in height, 3-ft in width, and 1-ft in depth. The background of the photograph shows a 240-V to 8-kV, 50 kVA conventional transformer, which provides the high-voltage input power for testing. The transformer has a 39-H magnetizing and 44-mH secondary leakage inductance. The ratio is about 0.1%, so it is very well wound transformer. The input voltage is measured through a 100:1 ratio potential transformer (PT), and the current is directly measured with a oscilloscope probe. The harmonic spectrum of the input voltage is calculated using data stored from the experiment, and the result is shown in Fig. 5. The 3rd, 5th and 7th harmonic content is mainly caused by the source voltage. The 20-kHz harmonic is the result of two 10-kHz PWM signals in interleaved operation, and the 84-kHz harmonic is from LLC resonant converter. Two of series class X1 1-uF 1.5-kV capacitors are used for DM filter, and also two of series same capacitors and 1-Ω resistor are used for RC damping network in each module. The cutoff frequency of DM filter and a line impedance can effectively attenuate switching noise presented in Fig. 5. For the CM coke, 3-mH 3-kV is implemented in each module, but y-cap is not implemented.

C. *Parastic estimation and simulation*

In order to estimate the common mode EMI path, the parasitic components need to be defined. Each switching device has a thermal pad and isolation material, which is comprised of a Glastic plate, and is placed between the module heatsink and the frame ground as shown in Fig. 6.

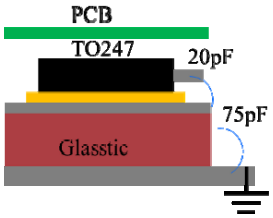
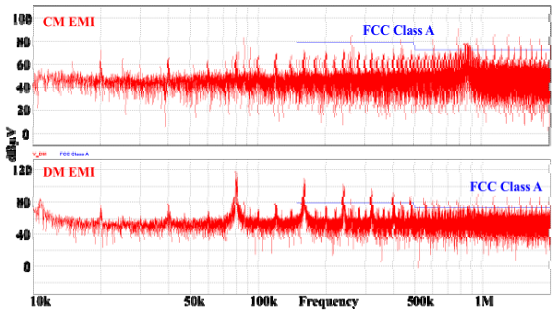


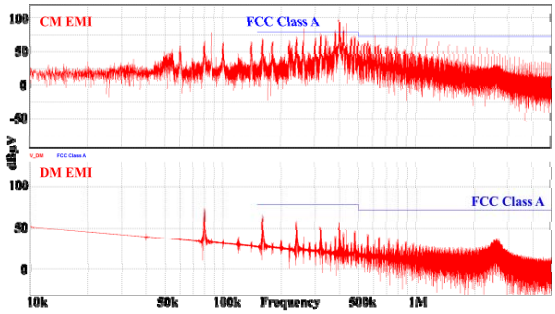
Fig. 6. Parasitic components in power stage.

The parasitic capacitance of the Glastic panel can be calculated using area of common plane, height, and material permeability as shown:

$$75pF \approx \frac{0.0886\varepsilon_\gamma A}{h} = \frac{0.0886 \cdot 2.1 \cdot 525}{1.3} \text{ [10].} \quad (1)$$



(a) without EMI filter



(b) with EMI filter

Fig. 7. EMI simulation results

A conducted EMI measurement is performed using simulation tools to verify filter operation. Two series modules are used for the power circuit and the operating power is set at

250W, with a 200V input voltage. The conducted EMI is then measured using a line impedance stabilization network (LISN).

Fig. 7. shows the EMI simulation results. CM and DM are both higher than the FCC Class A standard allows for without a filter, shown in Fig. 7(a). As shown in Fig. 7(b), DM noise is much below than the standard, and 20kHz and 84kHz are significantly reduced using x-cap.

IV. Input Disturbance Compensation

A. Current reference generation

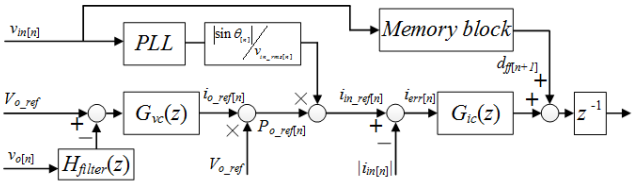


Fig. 8. The proposed control diagram of the SST.

Fig. 8. shows the control diagram of the SST. The outer loop is an output voltage control loop and controls the 20 paralleled outputs of the dc-dc converters. In the output voltage feedback, a digital notch filter is implemented to reject the double line frequency, so that the input current is not distorted by the double line frequency with higher voltage loop bandwidth. The current phase lead is caused by the double line frequency in the output voltage, since the double line frequency is fed back into the voltage controller, affecting the current reference. The input current reference is obtained through the loop by dividing the output power reference by the input RMS voltage, which is 7.2kV. The current reference is each module's individual reference regardless of the number of modules in series. The inner loop is the input current control loop, which generates the duty output. The final duty is the sum of the ideal duty feed-forward and the current controller output. Since the sampling frequency is 20kHz, a digital delay is unavoidable, so the ideal duty feed-forward is a future value greater than 1.5 times the sampling time. The final duty goes to each PWM module and is compared with a phase shifted carrier in order to interleave the PWMs of the AFE. The whole control block is similar to that of conventional average mode control.

B. Phase Lock Loop (PLL)

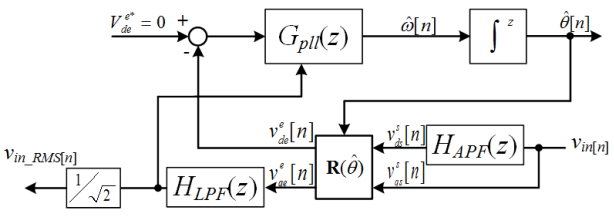


Fig. 9. Diagram of the phase lock loop.

A phase lock loop (PLL) is implemented for processing information given an angle and a magnitude of the input voltage. Fig. 9 shows a diagram of the PLL. In the diagram, the original input voltage and the delayed input voltage is shown frozen in time. A digital all pass filter (APF) is used for a 90 degree phase shift. The rotation frame of v_{qe} represents the peak value of the input voltage, however it can contain distortion from the grid, so a digital low pass filter is adopted for a stable peak value and a RMS value. The v_{qe} is kept updated for the variable gain of the PLL controller, which lets us achieve the same controller crossover frequency at different voltage levels. Too high of a crossover frequency follows input distortion, whereas too low of a crossover frequency follows input frequency.

C. Duty Feedforward

An ideal grid voltage waveform contains only the fundamental frequency, but a real world grid voltage waveform contains harmonics due to nonlinear loads present. In order to feed forward the right duty, the real world input voltage with distortion must be used. However, digital sensing and updates result in a delay, so the distortion compensation still has a mismatch. The delay can be compensated by phase shift using the PLL, but it does not contain all harmonic contents.

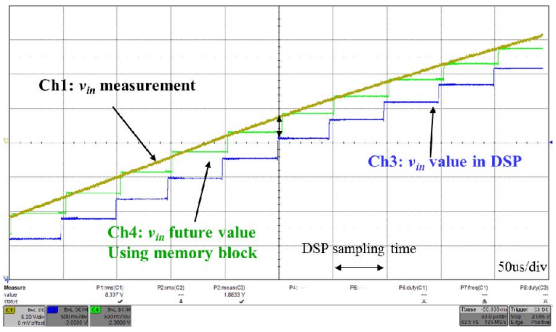
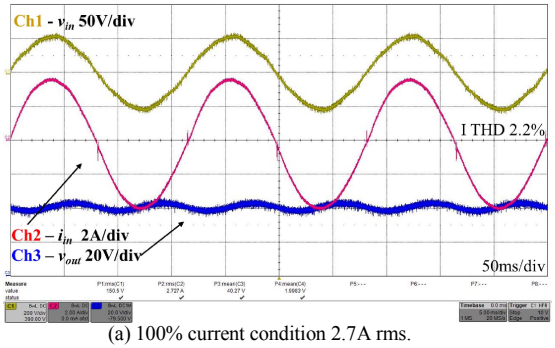


Fig. 10. Comparison of measured, delayed and compensated input voltage.

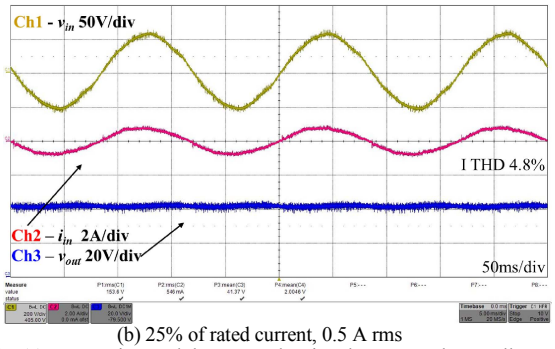
Fig. 10. shows the result using a memory block containing one period's previous value, which updates the value one sample ahead at a given time. The time division has the same sample period, and the DSP value has a delay from measuring v_{in}. However, the future value is already exactly matched with the measurement value. By using one sample ahead value, the zero crossing and input voltage distortion can be compensated.

V. Experimental Result

The SST is consisted with 10-modules for 7.2kV input, and the individual module is designed for 720V input. However, the control scheme and EMI filter were tested in low voltage condition with 2-modules at this time.



(a) 100% current condition 2.7A rms.



(b) 25% of rated current, 0.5 A rms

Fig. 11. Two series module test result using the proposed controller.

Fig. 11 shows two series module test results. The converter output voltage is controlled to 40V, which is also 10% of the nominal voltage. The switching frequency of PFC and DCDC converter are 20 kHz and 84 kHz. The controller bandwidth of voltage and current are 200 Hz and 1.8 kHz. Fig. 11 (a) shows the rated current condition, i_{in} THD is 2.2% under 2.3% of v_{in} THD, which means v_{in} distortion is fully compensated and some of from zero crossing distortion. Fig. 11 (b) shows 25% of the rated current, i_{in} THD is 4.8% which is still good under light load condition.

VI. Conclusion

The input voltage harmonic measurement has been showed under 6.6kV condition, and EMI filter was designed for attenuating the switching noise and the interaction of line impedance. The EMI simulation showed CM and DM noised is much reduced by the filter. The proposed controller SST has been explained and verified. The input voltage harmonics were significantly reduced in the current waveforms both light load and full load condition in two series module test.

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