A Behavioral Transient Model of IGBT for Switching Cell Power Loss Estimation in Electromagnetic Transient Simulation

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***Abstract*— The paper presents an improved Behavioral Transient Model (BTM) of IGBT with anti-parallel freewheeling diode. This model combines advantages of both existing physical and behavioral model considering the dynamic behavior of IGBT and the reverse recovery characteristics of the diode. Power Loss Estimation Method (PLEM) for switching cell is further proposed to obtain the loss table under various operating conditions. In addition to traditional modeling techniques which only uses ideal switch for the circuit simulation, this paper uses PLEM to replicate the loss behavior of semiconductor devices. This results faster simulation speed and at the same time guarantees higher accuracy. This approach is promising for high frequency power loss estimation, cooling system design optimization and semiconductor selection. The proposed model is implemented in PSCAD/EMTDC and look-up table is used for power loss estimation in circuit simulation. The parameters for the model are mainly extracted from the device datasheet. Further, this has been verified by experimental results using double pulse test bench.**

Keywords—IGBT; Power loss; Behavioral Transient Model;

I. INTRODUCTION

Power semiconductors are critical components in a power electronics (PE) system. Among conventional power semiconductor switches, IGBT is widely used in medium-frequency PE converters ranging from medium to high power [1], [2]. In a PE converter, an IGBT is paired with a Diode in order to provide current commutation, this is called a Switching Cell (SC) as shown in Fig. 1. During transition, switching losses are generated in both the IGBT and the Diode. They dominate the semiconductor loss in the high switching frequency applications, and they are not easy to be estimated. Thus, PE engineers and researchers require an accurate model to study the SC dynamic behavior, and thereby predict device power dissipation to optimize the overall system design [3].

The majority of Electromagnetic Transient Simulation (EMTS), such as PSCAD, in PE converter employ ideal switch or two-state resistor for semiconductor such as diodes, IGBT, thyristors[4]. For system level electrical behavior simulation, it is accurate enough, for instant of simulating system control response. However, for simulating efficiency of power apparatuses, the estimation of switching loss has to consider the detail physics switching process of SC, which requires nanoseconds time-step and could be overly time consuming [5]. Thus, it is not generally to be used.

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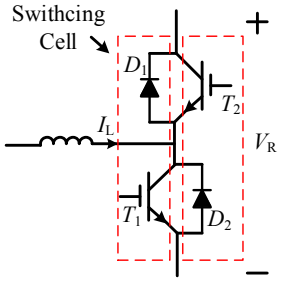

Fig. 1 IGBT Module and Switching cell.

Physical models are typically used to model the characteristics and behaviors of IGBTs, such as Hefner model [6], Kuang Sheng model [7] and Kraus model [8]. Those models describe electric carrier behavior and solve complex current transport equations to obtain higher accuracy. This poses huge computational resources during large multi-device PE system simulation and complicated parameters extraction procedure. Behavior models [9], [10] are another type of model that have relatively faster simulation speed. However, they only consider the external behaviors of the device and neglect the interaction between IGBT and diode.

For accurate estimation of power loss, one approach is using specially defined functions obtained by measurement [11] or defining power losses as a function of voltage, current and temperature through look up table and curves fitting [12]-[13]. However, these methods require devices test as well as small time step in simulation. Another way is deriving the simple function of losses based on the typical waveforms [14]. In this way, the accuracy is totally depends on the waveforms which may change under different operation conditions. Hence, it is still approximate and only suitable for roughly estimation.

This paper proposes a Behavior Transient Model (BTM) to achieve high accuracy of static and dynamic behaviors of SC. The model takes into account the various factors including tailing current, miller plateau voltage, nonlinear parasitic parameters of IGBT and reverse recovery current of diode. The PLEM for the switching cell proposed in this paper extends the previous approaches based on the BTM simulation waveforms. Most of the model parameters are obtained from the device datasheet. Further the model was implemented in PSCAD/EMTDC and verified by the experimental results using double pulse test bench as well as comparison with published loss curves by the manufacturer.

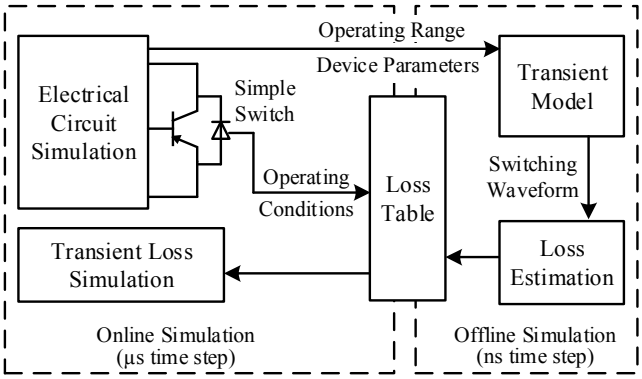

Fig. 2 Block diagram of online simulation of power semiconductor losses in PSCAD.

II. Development of Device Model

A. Statergy of Online Simualtion of Power Semicodncutor Losses

The model depicted schematically in Fig. 2, adds additional loss table to simple switch model for power loss estimation under online simulation. For obtaining the loss table which is a function of various operating voltage, current, the BTM and PLEM are applied in the offline simulation with nanosecond time step. The system operating conditions and device parameters extracted from datasheet are the inputs of BTM for simulating detailed switching waveforms. Based on that, the power losses can be calculated by the PLEM presented below. Hence, the completed loss table under the operating range is an interface between the system online simulation and device offline simulation. Through look up table, PE system simulation considering device transient power loss is relatively achieved with fast speed and high accuracy.

B. Behavioral Transient Model of IGBT Module

IGBT consists of an N-channel MOSFET (MOS) and a PNP Bipolar Junction Transistor (BJT) whose base current is controlled by the gate MOS voltage [15]. Based on the physical structure, the schematic of the proposed BTM is shown in Fig. 3. $I_{m\text{-}b}$ is the total current flowing through the MOS and BJT. I_{re} is the reverse recovery current of the free-wheeling diode (FWD). C_{ies} and L_s are the input parasitic capacitor and inductor, V_{miller} and V_{cesat} are the equivalent miller plateau voltage source and IGBT collector-emitter saturation voltage source, R_g and R_D are the gate resistor and the forward conducting resistor of diode.

$$I_{\mathrm{m-b}} = \begin{cases} 0, V_{\mathrm{ge}} \le V_{\mathrm{T}} \\ K\left(V_{\mathrm{ge}} - V_{\mathrm{T}} - 0.5V_{\mathrm{ce}}\right), V_{\mathrm{ce}} \le V_{\mathrm{ge}} - V_{\mathrm{T}} \\ 0.5K\left(V_{\mathrm{ge}} - V_{\mathrm{T}}\right)^2, V_{\mathrm{ce}} > V_{\mathrm{ge}} - V_{\mathrm{T}} \end{cases} \quad (1)$$

The static characteristics of IGBT in the regions of cut-off active and saturation can be described by the following equations [16]. Instead of the trans-conductance K_p in MOS and current gain β in BJT, this paper uses the equivalent trans-conductance, K, where $K=(1+\beta)K_p$, which the same as threshold voltage V_T can be extracted directly from the output and transfer characteristics. V_{ce} and V_{ge} are the collector-emitter voltage and gate-emitter voltage of IGBT [17].

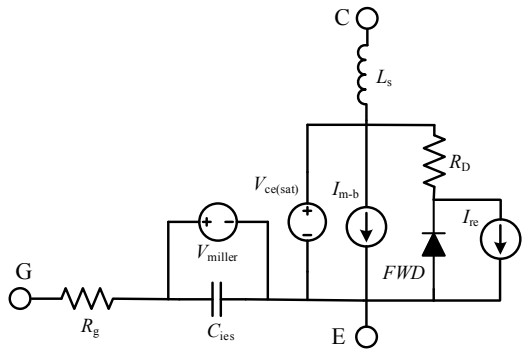

Fig. 3 The transient model circuit of IGBT and anti-parallel diode.

Besides the conventional equations, an additional set of equations are derived to completely describe the nonlinear characteristics in BTM. During the IGBT turn-off transient, the excess base carrier recombination makes the shutdown current tailing time longer. In the calculation, the tailing current can be described by the exponential function (2) . τ is the carrier transit time. t is the simulation time and t_0 is the initial time of the tailing current. I_{tail0} is the collector current at the start of the tailed stage.

$$I_{\mathrm{m-b}} = I_{\mathrm{tail0}} \times e^{-\frac{t-t_0}{\tau}}, (V_{\mathrm{ge}} < V_{\mathrm{T}}, \text{Turn off}) \quad (2)$$

As for the nonlinear characteristics of parasitic capacitors in IGBT, the input capacitor C_{ies} and feedback capacitor C_{res} are common parameters in the datasheet. According to the capacitor curve and gate charging curve in datasheet, the value of C_{ge} (so called miller capacitor) will change a lot depends on the collector-emitter voltage V_{ce}. This results the gate-emitter voltage V_{ge} constant in a period called miller plateau. During this period the IGBT keeps conducting and operates in saturated region. Hence, V_{ce} keeps saturated value V_{cesat} and the voltage value of miller plateau can be derived as shown in (3), where I_L is the conducting load current [18].

$$V_{\mathrm{miller}} = \sqrt{\frac{I_{\mathrm{L}}}{K}} - V_{\mathrm{t}} \quad (3)$$

In Fig. 3, the BTM of diode consists of an ideal diode, forward conducting resistor R_D and an current source I_{re} which represents the reverse recovery characteristic. Because of the minority carrier storage on both sides of the PN junction, the diode cannot switched off immediately and will turn into reverse recovery. In Fig. 4, I_F is the forward conducting current, di_F/dt is the slope of forward current, t_{rr} is reverse recovery time, I_{rm} is the peak current and Q_{rr} is the reverse recovery charge. The time at which current enters reverse recovery phase is t_{re}. At t_{rm} current reaches the peak I_{rm} [19].

In a switching cell, current will go through IGBT and diode alternatively. Hence, every time the diode turns off and starts reverse recovery, an additional over current will add to the paired IGBT. This interaction is expressed in (4) and the parameters are calculated by (5) according to the datasheet. The decay time constant of the reverse recovery τ_{re} and R_D can be extracted from diode curve using curve fitting.

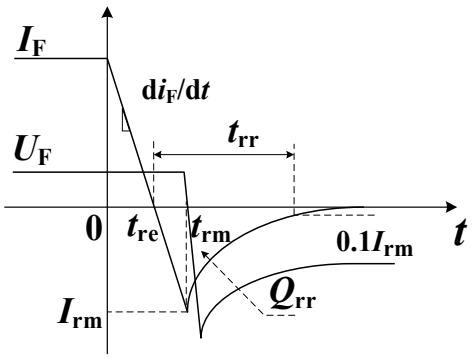

Fig. 4 The reverse recovery characteristic of diode.

$$I_{re}=\begin{cases}\frac{di_f}{dt}(t-t_{re}), t_{re}<t<t_{rm}\\ I_{rm}e^{-\frac{t-t_{rm}}{\tau_{re}}}, t>t_{rm}\end{cases} \tag{4}$$

$$\begin{cases}\tau_{re}=\frac{1}{\ln 10}(t_{rr}-\frac{I_{rm}}{\frac{di_f}{dt}})\\ I_{rm}=\sqrt{Q_{rr}\cdot di_f/dt}\\ t_{rr}=2\sqrt{Q_{rr}/di_f/dt}\end{cases} \tag{5}$$

III. Estimation of Power Loss

The analysis and calculation of the power losses of the switching cell are based on the diode-clamped inductive load test in Fig. 5 and the typical switching waveform in Fig. 6. V_{cc} is the dc link voltage. For simplicity, the voltage and current are assumed piecewise linear changing except in region t_3 to t_4 and t_7 to t_8. The tailing time, t_{tail}, is defined as the time period when I_L decreases from 10% to 1%. In addition, the diode reverse recovery is very short after t_7 and the loss is neglected. All the following switching period in the expressions can be obtained in the BTM simulation [20], [21].

A. Turn off power loss

The main part of the power loss at turn off are occurring from t_1 to t_3 and the tailing current period in Fig. 6. The total turn-off power loss includes the voltage slope loss E_{offV}, the current slope loss E_{offI} and the tailing current loss, E_{offT}.

In the interval [t_1, t_2], the current i_c keeps the same value as I_L and the voltage v_{ce} increase from 0 to V_{cc}. Therefore, the power loss during this period t_{offV} is given by

$$E_{offV}=0.5I_LV_{cc}t_{offV} \tag{6}$$

If v_{ce} is assumed constant during the interval [t_2, t_3], the resulting power loss is

$$E_{offI}=\frac{I_LV_{cc}}{2}\times t_{offI}+0.5L_sI_L^2 \tag{7}$$

Assuming the current starts tailing when it is 10% of I_L and the time constant τ equals to t_{tail}/ln100 , thus the power loss caused by the tailing current of IGBT during the period t_{tail} can be estimated as

$$E_{offT}=V_{cc}\int_0^{t_{tail}}e^{-\frac{t}{\tau}}dt=\frac{0.456I_LV_{DC}}{t_{tail}} \tag{8}$$

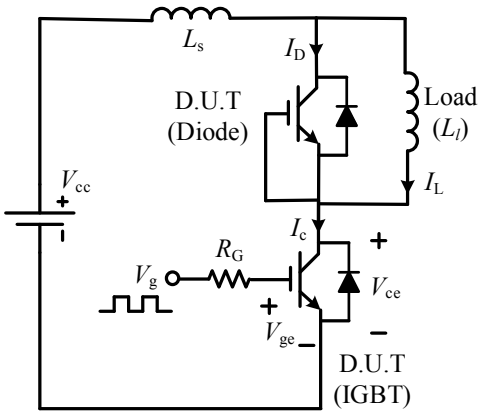

Fig. 5 The diode-clamped inductive load test circuit.

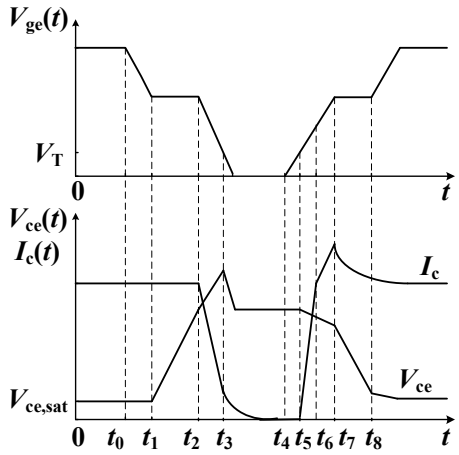

Fig. 6 Switching waveform of IGBT.

B. Turn on power loss

A similar analysis is carried out to calculate the turn on power loss from t_5 to t_8. The total turn-on power loss includes the current slope, E_{onI}, during the voltage slope, E_{onV}, and the reverse recovery loss E_{onirr}.

The power loss for the interval [t_5, t_6] characterized by increasing collector current can be expressed as

$$E_{onI}=0.5I_LV_{cc}t_{onI}-0.5L_sI_L^2 \tag{9}$$

Assuming that the current i_c=I_L during the voltage slope interval [t_7, t_8], thus the power loss becomes

$$E_{onV}=0.5I_LV_{cc}t_{onV} \tag{10}$$

As for the diode reverse recovery power loss during the period t_{rr}, we assume it is very short comparison to the voltage slope interval. Under this assumption, the power loss caused by the reverse recovery charge Q_{rr} is given by

$$E_{onirr}=(V_{cc}-\frac{L_sI_L}{t_{onI}})(I_Lt_{rr}+Q_{rr}) \tag{11}$$

C. Conduction loss

From the output characteristics of IGBT and diode in datasheet, the on-state voltage can be represented in terms of on-

state zero current collector-emitter voltage V_{ce0} and on-state resistor r_c in (12).

$$v_{ce} = V_{ce0} + r_c i_c \tag{12}$$

Hence, if the average current is I_{cav} and the rms value is I_{crms}, then the average conduction loss of IGBT are following, where f_{sw} is the switching frequency of IGBT.

$$P_{cIGBT} = f_{sw} \int_0^{1/f_{sw}} v_{ce} i_c dt = V_{ce0} I_{cav} + r_c I_{crms}^2 \tag{13}$$

D. Summary of Power Semiconductor Losses

The total switching power loss E_{ts} can be estimated as the sum of the loss equations above, and the total IGBT power loss is expressed in (15).

$$E_{ts} = E_{offV} + E_{offI} + E_{offT} + E_{onI} + E_{onV} + E_{irr} \tag{14}$$

$$P_t = P_{cIGBT} + E_{ts} f_{sw} \tag{15}$$

From the observation of the set of equations above, V_{cc} and I_L are the key parameters affecting the power loss. In addition, the effects of diode reverse recovery current, parasitic stray inductance and tailing current must be also be considered at high switching frequency.

IV. Simulation and Experimental Results

The developed BTM and PLEM in this paper are aimed to analyze the semiconductor power dissipation of the PE system when operating into an electrical network.

A. Transient model and loss estimation menthod validation

Based on the circuit in Fig. 5, a double pulse test bench is designed and implemented in the lab for testing IGBT and diode which includes DC power supply, IGBT driver control, DC capacitors, inductive load, protection circuit and the semiconductors under test as in Fig. 7. The Infineon IKW40T120 IGBT device (600V, 40A), is chosen for the study and test. The corresponding parameters of the model and the test bench are listed in Table I. The experimental results are measured and plotted for comparison with the proposed model simulation in PSCAD/EMTDC.

The plots for turn on and turn off of IGBT collector current and collector-emitter voltage are shown in Fig. 8 to Fig. 9. The switching details such as current and voltage spikes, tailing current, which because of the dynamic characteristic of IGBT, interaction of diode reverse recovery and the effect of parasitic inductor and capacitors are clearly seen from the transient waveforms. The model is not consider the small oscillation in current after IGBT totally turning on which is because of the parasitic parameters of the test bench board. The simulation results show good agreement with the experimental results.

The calculated power losses by PLEM are also compared with the measured results which are obtained by integrating the product of measured voltage and current during switching process in Fig. 12 and Fig. 13. A series of load voltage and current can be set to obtain the power loss table by the multiply-run function in PSCAD/EMTP as shown in Fig. 14. As can be seen, the simulation results have reasonable accuracy with variation of voltage and current.

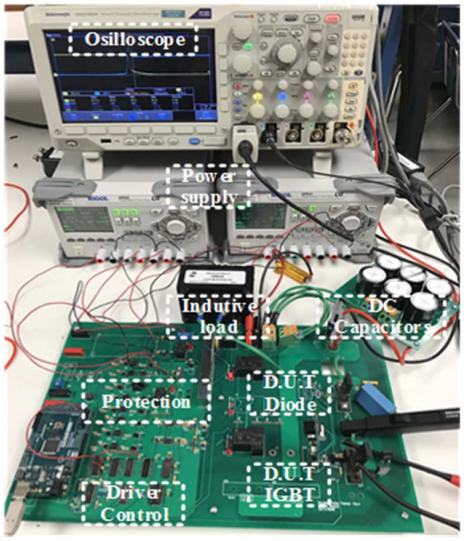

Fig. 7 Double pulse test bench.

TABLE I PARAMETERS OF IGBT MODULE AND TEST BENCH.

Parameter	Value	Parameter	Value
R_g	6Ω	C_{ies}	2500pF
V_t	5.8V	C_{res}	110pF
K	2.834 A/V^2	V_{cesat}	2.3V
t_{rr}	410ns	Q_{rr}	8.8μC
V_{cc}	0-1kV	L_l	5mH
I_L	0-80A	L_s	180nH
I_{rm}	36A	R_G	15Ω

B. Application

The loss table can be applied to different specific PE application such as buck, boost converter, Power Factor Correction (PFC) for semiconductor loss estimation. As in Fig. 15, a simple boost converter application is implemented in PSCAD/EMTDC using conventional semiconductor switch model with additional loss table obtained above. The input system voltage V_s is 300V, inductor L is chosen as 10 mH for a relatively small current ripple, and capacitor is 200 μF. For the rated operating point (V_L=600V and I_L=40A), the load resistor is 15 Ω and the IGBT is controlled by the gate signal T with 50% duty cycle and 10 kHz frequency.

The load voltage and current waveform as well as IGBT power loss waveforms can be seen in Fig. 16. It is noted that the circuit simulation can operates under the same large time step (50μs) with additional semiconductor transient power loss through look up table. The output voltage and current gradually reach the desired value, At the same time, the proportions of switching loss and conducting loss is changing with the variation of operating voltage and current. The switching loss is smaller than the conduction loss at beginning, and then it becomes the dominant loss. It is obvious that the switching loss can not be neglect especially for high frequency application. In this way, the power loss can be estimated which is promising for cooling system design optimization and semiconductor selection.

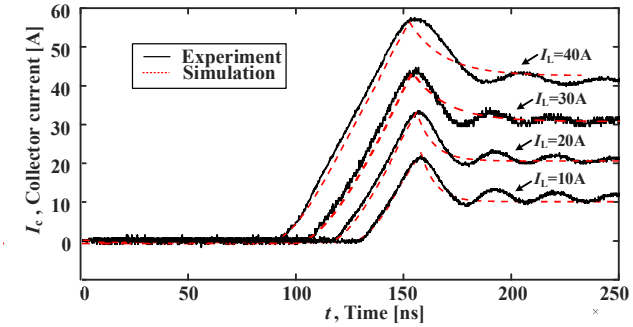

Fig. 8 IGBT turn on collector current waveform.

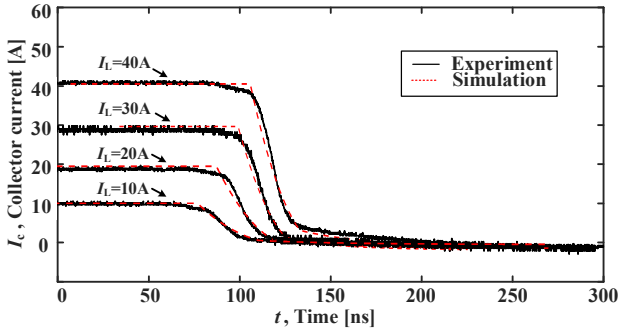

Fig. 9 IGBT turn off collector current waveform.

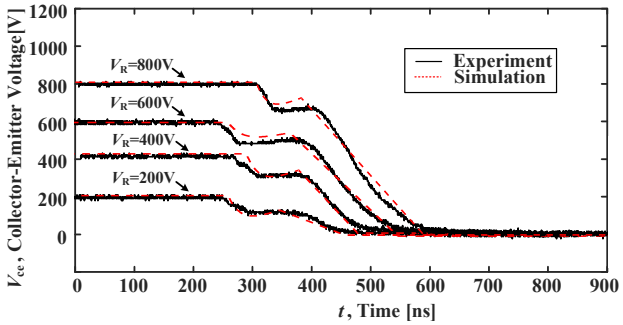

Fig. 10 IGBT turn on collector-emittor voltage waveform.

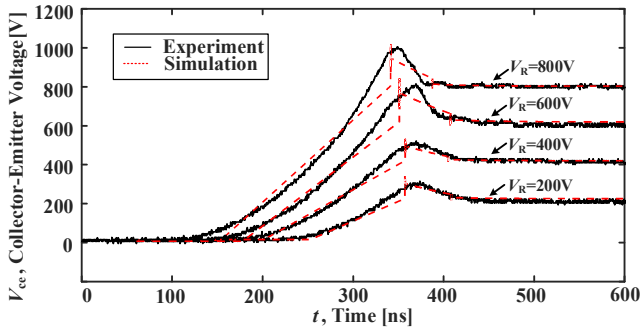

Fig. 11 IGBT turn off collector-emitter voltage waveform.

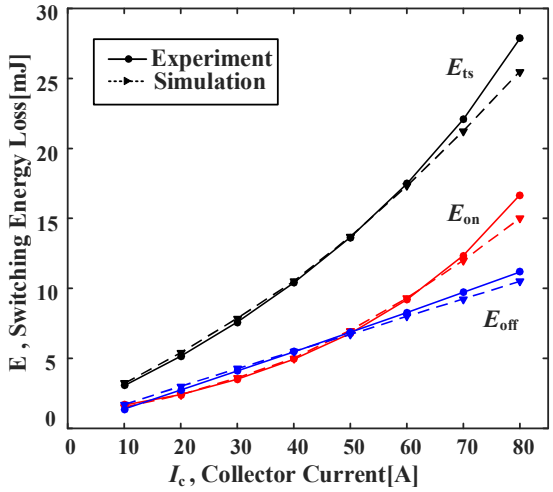

Fig. 12 Switching loss vs collector current.

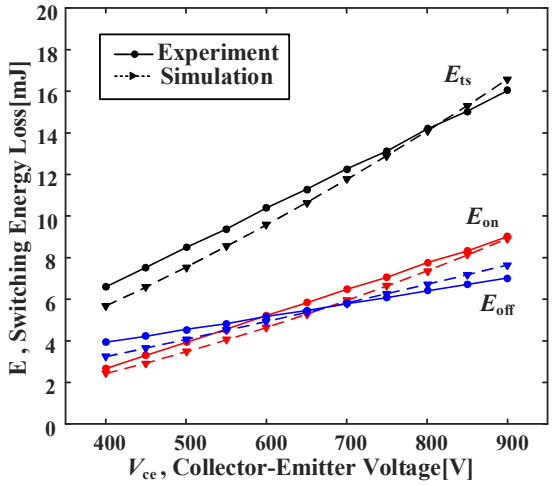

Fig. 13 Switching loss vs collector-emitter voltage.

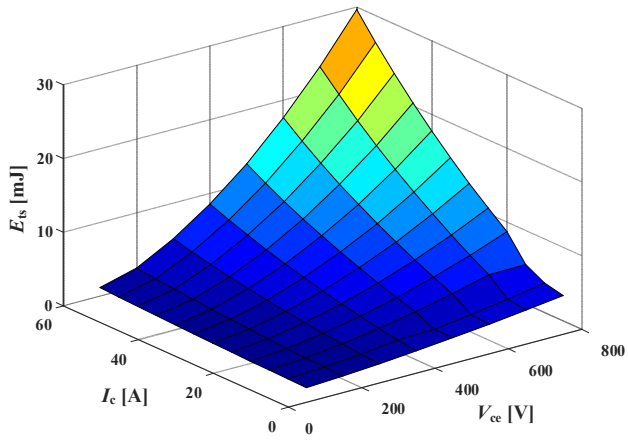

Fig. 14 Switching loss vs current and voltage.

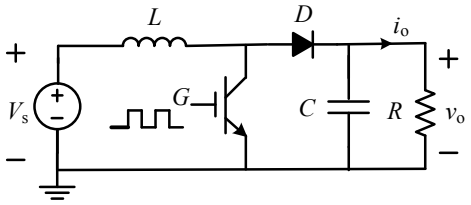

Fig. 15 Simple boost converter circuit.

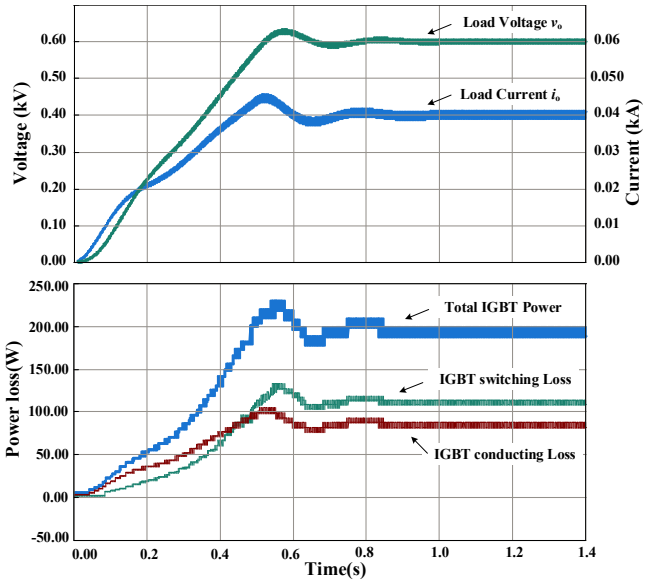

Fig. 16 Variation of power loss in boost application.

V. CONCLUSION

The major contributions of this paper are improving the existing models of semiconductor switch model in electromagnetic transient simulation to illustrate the important phenomena characteristic of IGBT and diode, and a detailed analysis of the power loss calculation based on the detailed features of switching waveforms. Through look up table, the power loss table generated in device offline simulation is applied to the system online simulation for loss estimation.

The behavioral transient model of IGBT with anti-parallel diode as well as the method of power loss estimation has been proposed, implemented in PSCAD/EMTDC and experimentally verified. This model incorporates the nonlinear capacitors and the effect of excess base carrier recombination of the IGBT as well as the reverse recovery of the diode. The power loss look-up table is obtained from the proposed model, which can further be extended to estimate the semiconductor losses in circuit level EMTDC simulation without requiring excessively small time steps. The parameters of the model can be extracted from the device datasheet and loss calculation mainly based on the transient switching waveforms from the demonstrated model.

The thermal network modeling for the thermal impedances among the junction , case, heatsink and open air which can be combined with the proposed power loss table for temperature prediction as well as more complex high frequency PE applications will be the main future work.

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