Analytic Model for Power MOSFET Turn-Off Switching Loss under the Effect of Significant Current Diversion at Fast Switching Events

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***Abstract*— The conventional method to evaluate switching loss of power MOSFETs is commonly based on the existence of the plateau gate-voltage region in the gate-charge plot. However, a very different behavior of the MOSFET with disappearance of the plateau region is observed under significant current diversion between channel and parasitic capacitances when a large gate drive current is applied to turn off the MOSFET. As the modern power converter is pursuing higher switching frequency, the gate drive current becomes larger accordingly to turn on and off the power MOSFET faster. Hence, this paper proposes an analytical model to predict the timing pattern and the switching loss more precisely in such conditions. Simulation and measurement have been conducted to validate this model, showing an accurate estimate of the switching loss at fast switching transition and a good match with the conventional model at slow switching transition. Moreover, non-linearity of the MOSFET's output capacitance is considered in this model, suggesting a handy graphical method to determine the timing pattern and the switching loss properly in practice.**

Keywords—Current diversion, MOSFET parasitic capacitors, MOSFET switching loss, power MOSFET modelling

I. INTRODUCTION

Nowadays, the switching frequency of switch-mode power converters is continuously increasing in order to achieve higher power density. As a result, fast on and off switching is required for the operation of power MOSFETs to reduce the switching loss. Prediction of MOSFET switching loss under such conditions, in which the current diversion between channel and parasitic capacitances is significant, becomes more complex and crucial [1 - 3]. However, the conventional method based on the plateau gate voltage [2 - 5] is no longer correct under such conditions. Therefore, an insightful analysis and an effective computational model of transients at switching events are essentially required when a large gate drive current is applied. In this paper, a more precise and generalized method is proposed to calculate the switching loss under such conditions.

II. GENERALIZED MODEL OF MOSFET SWITCHING LOSS

To simplify the calculation of switching loss and gain understanding of the gate charge process under the effect of current diversion, the parasitic inductance is assumed to be negligible in the following equations. Parasitic inductance can be considered as a separate effect [6]. Applying KCL at drain and gate nodes of the MOSFET in Fig. 1, the following equations are obtained for saturation mode:

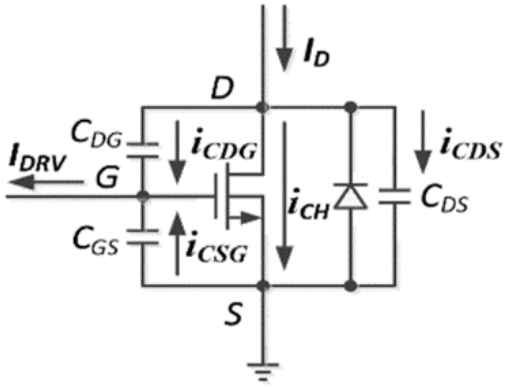

Fig. 1. Model of the MOSFET

$$\begin{aligned} & i_{CDS} = I_D - i_{CH} - i_{CDG} \\ & \Leftrightarrow C_{DS}\frac{dv_D}{dt} = I_D - \frac{1}{2}\mu_n C_{OX} v_{ov}^2 - C_{DG}\left(\frac{dv_D}{dt} - \frac{dv_G}{dt}\right) \end{aligned} \quad (1)$$

$$\begin{aligned} & I_{DRV} = i_{CDG} + i_{CSG} \\ & \Leftrightarrow I_{DRV} = C_{DG}\left(\frac{dv_D}{dt} - \frac{dv_G}{dt}\right) - C_{GS}\frac{dv_G}{dt} \end{aligned} \quad (2)$$

Where,

$v_{ov} = v_G - V_{TH}$: overdrive gate voltage

μ_n: charge mobility of the process

I_D, I_{DR}, i_{CDG}, i_{CSG}, i_{CDS}, i_{CH}: currents in Fig. 1

C_{OX}: oxide capacitance per area

$C_{OSS} = C_{DS}+C_{DG}$: output capacitance

$C_{RSS} = C_{DG}$: miller capacitance

$C_{ISS} = C_{GS}+C_{DG}$: input capacitance

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After some math manipulation, the following differential equation can be derived:

$$\frac{1}{2}\mu_n C_{OX}\left[v_{OV}^2-\left(I_D-\frac{C_{OSS}}{C_{RSS}}I_{DRV}\right)\frac{2}{\mu_n C_{OX}}\right]=-\left(\frac{C_{ISS}C_{OSS}}{C_{RSS}}-C_{RSS}\right)\frac{dv_{OV}}{dt} \quad (3)$$

For simplicity, assume that I_D and I_{DRV} are constant during a short interval of saturation mode, which primarily determines the switching loss. At a turn-on event, I_{DRV} is negative because its direction is reversed as in Fig. 1. As a result, there is always a plateau region starting from the time when $dv_{ov}/dt = 0$ so that v_G is constant until C_{DS} is fully discharged. This plateau region occurs when v_{ov} reaches the following value:

$$V_{OVP}=V_P-V_{TH}=\sqrt{\frac{2}{\mu_n C_{OX}}(I_D-\frac{C_{OSS}}{C_{RSS}}I_{DRV})}$$

$$or \qquad I_{CHP}=(I_D-\frac{C_{OSS}}{C_{RSS}}I_{DRV}),\ equivalently \quad (4)$$

Where,

V_{OVP}: overdrive plateau voltage

V_P: plateau voltage

I_{CHP}: channel current at plateau region.

On the other hand, at a turn-off event, I_{DRV} becomes positive, then the value of I_{CHP} in (4) can be negative, depending on the ratio between I_D and I_{DRV}. If this expression is negative, the MOSFET is indeed cut off before the formation of plateau region since i_{CH} cannot be negative in reality. The condition for a plateau to appear at turn-off is defined by:

$$\frac{I_D}{I_{DRV}}\geq\frac{C_{OSS}}{C_{RSS}} \quad (5)$$

In contrast, the plateau region can be avoided when (5) is not met. Since the beginning of the plateau region at turn-off is the moment that the MOSFET ends its triode mode to enter the saturation mode [4, 5], elimination of the plateau voltage intuitively implies that the MOSFET switches off before it goes deeply to saturation mode, thus v_D is kept small until $v_G = V_{TH}$. More precisely, the MOSFET slightly enters saturation and v_D rises to a small value V_{DOFF} by the time $v_G = V_{TH}$. This value is found by integrating both sides of (2) and rearranging its terms:

$$V_{DOFF}=\frac{I_{DRV}}{C_{RSS}}\Delta t-\frac{C_{ISS}}{C_{RSS}}(V_{SP}-V_{TH}) \quad (6)$$

Where, V_{SP} is switching-point voltage, at which the MOSFET starts to enter saturation mode. Δt is the interval of time from that point until $v_G=V_{TH}$ and determined by solving (3). Since the gate charge of the plateau region is a large portion of the total charge, Δt is substantially shortened when the plateau region is eliminated, V_{DOFF} is hence so low that switching loss is smaller compared to the conventional plateau-based estimation. In this scenario, v_D rises and i_{CH} falls at the same time. Turn-off switching loss is thus given by:

$$P_{SWoff,\,non-plateau}=\frac{1}{6}I_D V_{DOFF}\Delta t f_{SW} \quad (7)$$

Where,

$P_{SWoff,\ non\text{-}plateau}$: turn-off switching loss when the plateau region does not exist

f_{SW}: switching frequency

III. Effect of Voltage Dependent Capacitance

As a result of equations (4) and (5), the ratio C_{OSS}/C_{RSS} determines whether there is a plateau region as well as the value of plateau voltage V_P. It is noteworthy that C_{OSS} and C_{RSS} are both functions of v_D, which is time-varying at switching events. Consequently, there are 3 different possibilities during the switching events. Fig. 2 is a graphical method to determine the operating point of a MOSFET, taking BSZ042N06NS [7] as an example:

- Case1, $(I_D/I_{DRV})C_{RSS} < C_{OSS}$ at any V_D: No plateau region
- Case 2, $(I_D/I_{DRV})C_{RSS} = C_{OSS}$ at V_{Dcross}: The MOSFET starts working in the case 3 (described below) from $v_D = 0$ V to $v_D = V_{Dcross}$. From this point forward, the MOSFET turns to operate in the case 1 from $v_D = V_{Dcross}$ to the maximum voltage applied to the drain terminal.
- Case 3, $(I_D/I_{DRV})C_{RSS} > C_{OSS}$ at any V_D: Plateau voltage V_P is determined by (4). In fact, there is a slope at plateau region because of the variance of (C_{OSS}/C_{RSS}).

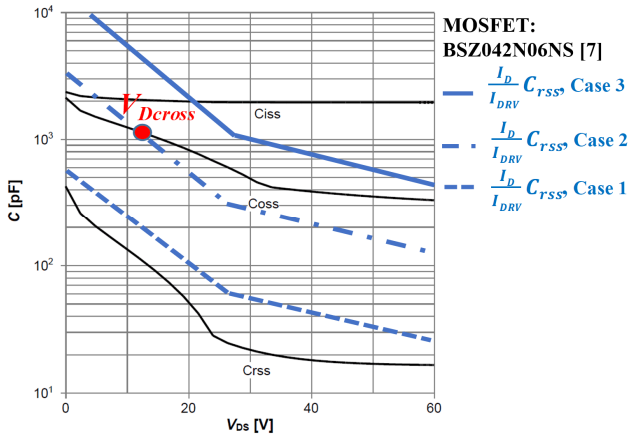


Fig. 2. Different scenarios at turn-off event

After the operating point has been determined by the graphical method, the turn-off switching loss of the device can be estimated appropriately. If the MOSFET works entirely in case 1, equations (6) and (7) are employed to find the switching loss. In contrast, the conventional method based on the plateau voltage [5] can be applied for case 3, in which inequality (5) holds true over the whole range of v_{DS}. In both case 1 and case 3, average values of the MOSFET's parasitic capacitances over the operating range of v_{DS} are used in analytic equations to simplify the calculation. Eventually, if the

operating point falls into case 2, both methods presented in case 3 and case 1 should be applied for two different regions: $v_{DS} \le V_{Dcross}$ and $v_{DS} > V_{Dcross}$, respectively. For simplicity, the following approximation is employed in case 2:

$$P_{SWoff,case2} = \frac{V_{Dcross}}{V_{Dmax}} P_{SWoff,case3} + \left(1 - \frac{V_{Dcross}}{V_{Dmax}}\right) P_{SWoff,case1} \quad (8)$$

Where,

$P_{SWoff, case\ 1}$, $P_{SWoff, case\ 2}$, $P_{SWoff, case\ 3}$: turn-off switching loss calculated in case 1, case 2, and case 3, respectively

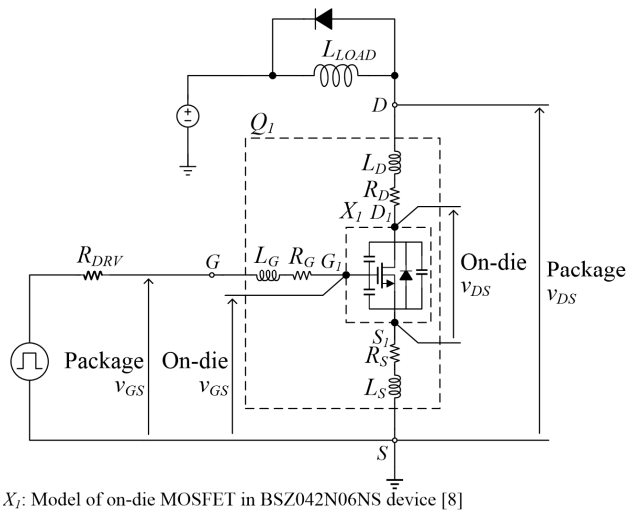
V_{Dcross}: v_D at the crossing point of case 2 in Fig. 2

V_{Dmax}: Maximum voltage seen at the drain

IV. Simulation and Experimental Results

A. Simulation Results

To validate the proposed model, formation of the plateau region is observed when I_D/I_{DRV} is varied in a circuit simulation, as illustrated in Fig. 3, where MOSFET Q_1 drives an inductive load L_{LOAD}, which is a common application in practice. In this figure, Q_1 is an electrical circuit representation of the PSPICE model of MOSFET BSZ042N06NS, provided by its manufacturer Infineon Technologies [8]. The simulation presented below has taken into account parasitics of the device package included in the given PSPICE model. When the MOSFET is switched off rapidly, there is a big difference between the waveforms at the package pins and at on-die pads because of parasitic inductance of the connections. Fig. 4 illustrates the simulated waveforms when turning off the MOSFET. It is noteworthy that waveforms of V_{GS} at package pins are quite different from on-die pads, suggesting that a real hardware measurement would not show the exact waveforms at the on-die gate. The simulation verifies the three cases



X_1: Model of on-die MOSFET in BSZ042N06NS device [8]
Q_1: Full model of BSZ042N06NS device including parasitics of package [8]

Fig. 3. Simulation test bench with manufacturer's electrical model of BSZ042N06NS [8]

predicted by the proposed model. In case 1, the plateau region disappears at I_D = 2.8 A. While in case 2 and 3, the plateau region exists.

B. Experimental Results

Measurement has been also conducted to verify the energy loss at switch-off events in an active-clamp forward converter (ACFC) power block [9]. Fig. 5 (a) shows the circuit diagram of the ACFC power block, wherein Q_M is the device under test (DUT). Fig. 5 (b) shows a photograph of the ACFC circuit board and the control board.

The turn-off switching loss is determined from the overlapping area of v_D and i_D waveforms during their rise/fall time. While the v_D waveform across MOSFET Q_M can be

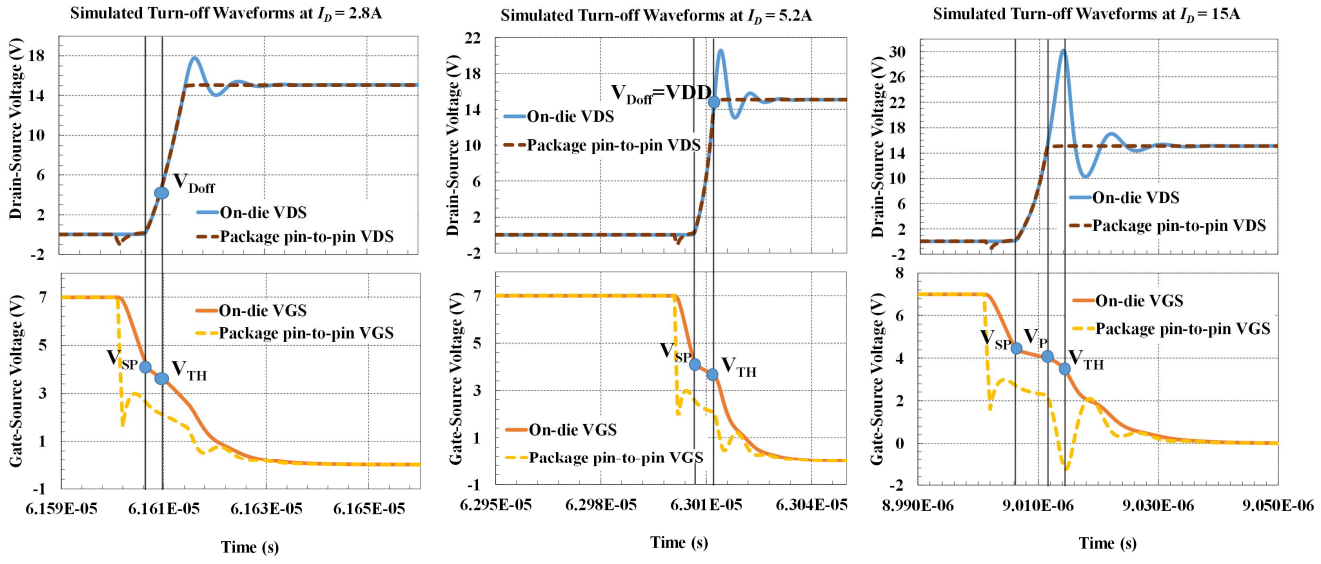
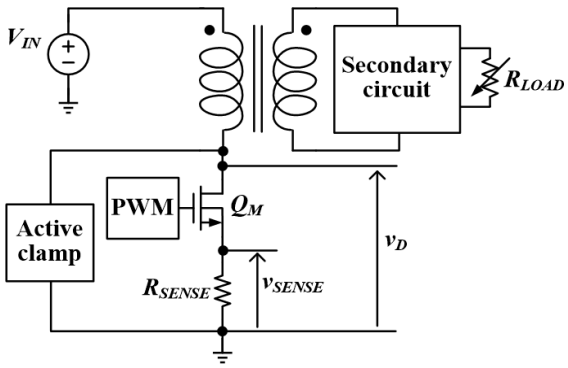
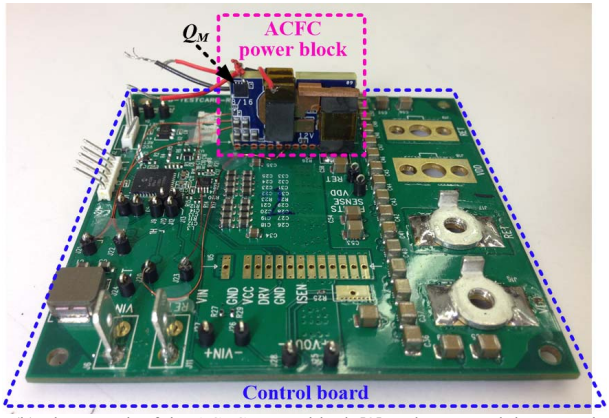


Fig. 4. Simulation results validate the three cases predicted by the proposed method (I_{DRV} = *1.1 A*)



Q_M: Main power MOSFET BSZ042N06NS

(a) Block diagram of the ACFC power block [9] with Q_M as the DUT



(b) Photograph of the ACFC power block [9] under test and the control board

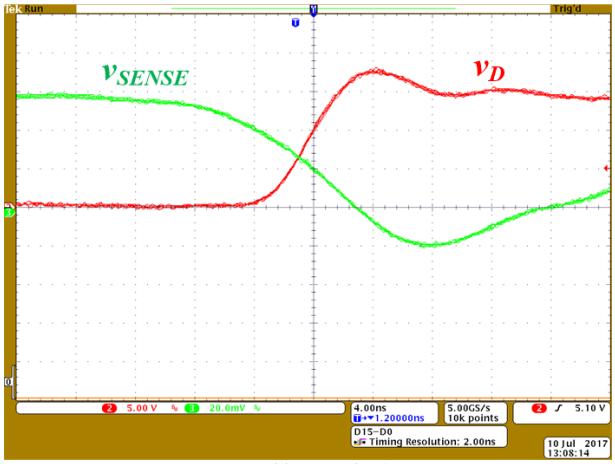
Fig. 5. Implementation of hardware test

directly captured with a voltage probe, the i_D waveform is otherwise derived from the voltage v_{SENSE} across R_{SENSE}, between Q_M's source and ground. The value of R_{SENSE} is chosen to be very small (i.e. 16.5 mΩ) so that v_D is approximately the same as v_{DS} across Q_M as v_{SENSE} is negligible compared with v_D during turn-off (i.e. $v_{SENSE} \leq 1.5\% V_{IN}$ over the whole range of I_D in the experiment).

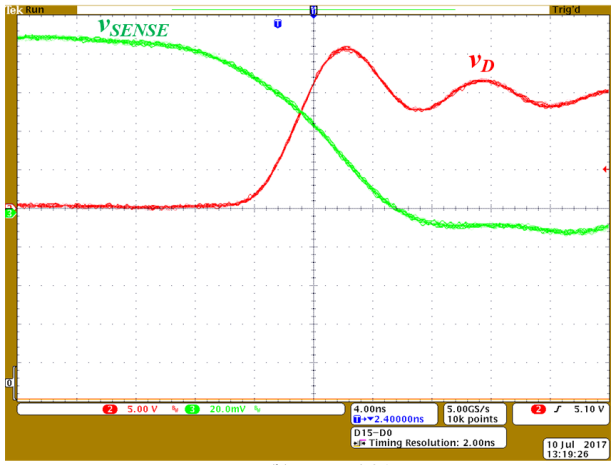
On the other hand, the total energy resulting from the overlapping area of I_D and V_{DS} at turn-off consists of two terms: the real switching loss due to the channel current of Q_M and the energy to charge up C_{OSS} of Q_M as v_D rises. Since C_{OSS} is charged by an inductive current from the transformer, it does not cause energy loss. However, it is still included in the measurement because the total current I_D is the sum of the channel current and the capacitor-charging current. Therefore, it is necessary to evaluate the charging energy E_{OSS} by the following integral:

$$E_{OSS} = \int_{v_{DS}} C_{OSS} v_{DS} dv_{DS} \tag{9}$$

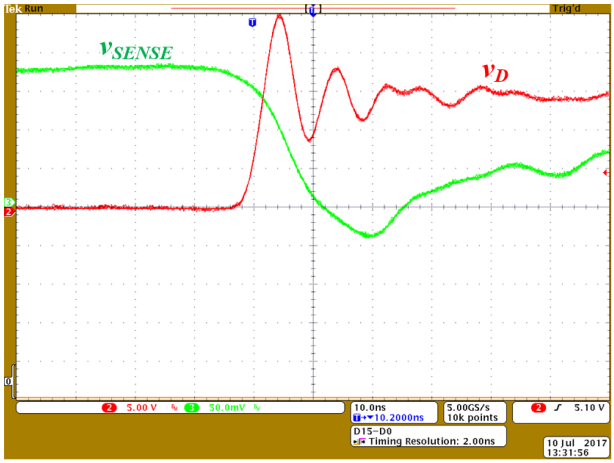
It is noteworthy that C_{OSS} is a non-linear function of v_{DS}, as seen in Fig. 2. Therefore, a piecewise method has been applied to approximate the function $C_{OSS}(v_{DS})$ from the datasheet plot shown in Fig. 2, and then it is plugged into equation (9) to calculate E_{OSS}. This energy is added to the switching loss



(a) I_D = 3.5A



(b) I_D = 4.9A



(c) I_D = 10.9A

Fig. 6. Measurement waveforms at varied I_D

energy computed by the proposed model to predict the total turn-off energy at a given ratio of I_D/I_{DRV}, in which I_D is calculated from V_{SENSE} in the measurement and I_{DRV} is estimated from the driving voltage and output resistance of the PWM generator as well as the internal gate resistance of Q_M.

On the other hand, the total turn-off energy is determined from the measurement by the following equation:

$$E_{OFF} = \int_{t_{OFF}} i_D v_{DS} dt = \int_{t_{OFF}} \frac{v_{SENSE}}{R_{SENSE}} v_{DS} dt$$
$$\approx \sum_i \frac{v_{SENSE}(i)}{R_{SENSE}} v_D(i)\big(t(i+1) - t(i)\big) \quad (10)$$

Where, $v_{SENSE}(i)$, $v_D(i)$, and $t(i)$ are data points of respective waveforms acquired from a digital oscilloscope. Some examples of measured waveforms are shown in Fig. 6 at I_D = 3.5 A, 4.9 A and 10.9 A. Fig. 7 shows a comparison of turn-off energy, which consists of switching loss and C_{OSS} charging energy, among the proposed method, the conventional method and the measurement result. The conventional method [5] approximately double the energy loss at I_D = 4.9 A as compared to measurement while the proposed method gives an error of only 20%. The measurement is significantly affected by parasitic inductance in the hardware test at high current since large inductive energy is added to the measurement, thus causing the measured energy to be much higher than the analysis at I_D = 10.9 A. As seen in Fig. 6 (c), a large inductive spike occurs in the v_D waveform during the switch-off time at I_D = 10.9 A, which results in a high peak voltage up to 25 V compared with the settled level at 16 V expected in the analysis. Consequently, this voltage peak causes the integral in equation (10), which is the outcome of the measurement, to increase substantially. Ideally, v_D should be clamped to 16 V by the active clamp circuit [9], but parasitic inductances including the leakage inductance of the transformer, stray inductance on PCB routes, package inductance of Q_M, as well as inductance from the probe cable have made the waveform of v_D largely overshoot as shown in Fig. 6 (c). Although the proposed model can be used in conjunction with the method presented in [6] to take into account the effect of parasitic inductance, de-embedding the inductive energy from the measurement requires extracting the values of these parasitic inductances, which is beyond the scope of this paper. However, it can be seen that the proposed method matches well with the conventional method at high current.

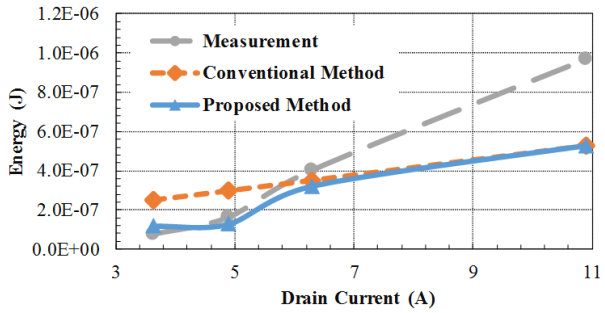


Fig. 7. Comparison of turn-off energy

V. CONCLUSIONS

This paper proposes an analytic model to evaluate the turn-off switching loss under the effect of significant current diversion when the gate drive current is comparable to the drain current. It is verified by simulation and measurement which shows that errors of turn-off energy loss predicted by this model are reduced by a factor of 4 - 5 times as compared with the conventional model [5] in such conditions.

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