

A Single Mode Load Tracking Voltage Mode Controller With Near Minimum Deviation Transient Response

Tom Moiannou, Yanhui Liu, Aleksandar Prodic
 Laboratory for Power Management and Integrated SMPS,
 ECE Department University of Toronto
 Toronto, Ontario, CANADA

Aleksandar Radic
 Appulse Power
 Toronto, Ontario, CANADA

Abstract: This paper introduces a practical single-mode quasi constant-frequency controller that provides practically minimum output voltage deviation during load transients. This control scheme eliminates the need for two separate controllers for steady-state and transient operation and the associated potential mode transition problems which are characteristic of numerous fast response solutions. The controller only relies on the detection of changes in the output capacitor current polarity and a simple PI compensator to provide fast transient response and tight voltage regulation. The effectiveness of this mixed-signal controller is demonstrated with a 600 kHz, 15 W single-phase buck converter based experimental prototype. During load transients, the inductor current is shown to be corrected within one switching cycle with near-minimum output voltage deviation.

Keywords—transient; minimum deviation; fast; time-optimal; control; digital control

I. INTRODUCTION

Modern switch-mode power supplies (SMPS), especially those used in point-of-load (PoL) applications, need to meet challenging requirements for both steady state and dynamic voltage regulation [1], [2]. In targeted applications, for converters processing from a fraction of a watt to tens of watts, the dynamic performance of SMPS controllers have a dominant influence on the sizing of the output filter capacitor [3]. As required output voltages decrease and load currents increase, meeting output voltage regulation requirements during transients requires greatly increased output capacitance [3] - [5]. Power supplies in portable applications have already been shown to consume a significant portion of PCB real estate [3]. Driven in large part by increasing output filter capacitance requirements this number has been growing and is likely to continue to grow [5]. Therefore, it is important to improve the dynamic performance of controllers as much as possible to limit this growth in area consumption.

In recent years, numerous fast load-transient response controllers have been proposed. Examples include time-optimal [6] - [10] and minimum deviation controllers [11] - [13]. For direct energy transfer converters, such as a buck converter, the usage of such controllers results in what is practically the minimum achievable voltage deviation for a given converter and load-step [11]. This presents the

This work of the Laboratory for Power Management and Integrated SMPS is supported by Würth Elektronik eiSos GmbH & Co, Germany

opportunity to drastically reduce the output capacitor volume. Still, the presented approaches suffer from a few drawbacks that have slowed down their wider adoption in targeted applications. Time-optimal controllers suffer from relatively high computational complexity [11], making them impractical in targeted hardware-limited low-cost applications. Minimum deviation controllers solve this issue and provide practically minimum output voltage deviation without increasing the computational burden on the digital, PID based, voltage mode controllers. Also, at the expense of increased voltage recovery time, minimum deviation controllers result in a significantly lower peak inductor current than time-optimal solutions, allowing for the use of smaller inductors. However, both minimum-deviation and most time-optimal solutions operate in two modes [6] - [13]. They combine a linear compensator for steady-state regulation with additional transient suppression circuits, which detect and respond to load transients. This two-mode operation is usually not preferable. This is mostly due to potential stability problems during mode transitions and/or additional hardware required to ensure seamless transitions [6], [7], [11].

The main goal of this paper is to introduce the practical single-mode minimum-deviation concept based controller of Fig. 1. Unlike previous solutions, it uses only one mode of operation for both steady state operation and during transients,

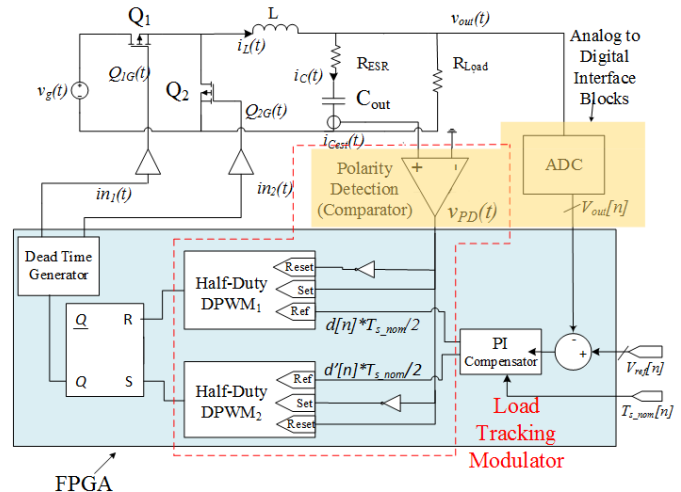


Fig. 1 A buck converter regulated by a single mode load tracking minimum deviation controller.

eliminating potential mode transition related stability problems while also further simplifying the hardware implementation requirements.

II. PRINCIPLE OF OPERATION

The introduced controller is shown in Fig. 1. It is a modification of a voltage mode controller where the conventional pulse width modulator (PWM) is replaced by the *load tracking modulator* block. This block consists of two *half duty digital pulse width modulator* blocks (DPWM₁ and DPWM₂) and one capacitor current polarity detection block. The half-duty modulators use information about the capacitor current polarity to gate the power transistors (Q_1 and Q_2) such that the inductor current is made to match the load current cycle by cycle while also reconstructing the desired inductor current ripple. It does this by splitting both the on-time (Q_1 on, Q_2 off, inductor charging) and the off-time (Q_1 off, Q_2 on, inductor discharging) into two separate phases each. These are called the “current correction phase” (CCP) and “ripple reconstruction phase” (RRP).

The functionality of the controller can be better understood with the help of Figs. 2 and 3. Fig. 2 depicts the operation of a buck converter running with the introduced control scheme in steady-state. At **point 0**, the converter enters its on-state. Q_1 is on, Q_2 is off, and the inductor current is charging up. This first segment is its on-state current correction phase (CCP). This phase runs until the inductor current equals (or otherwise exceeds) the load current (**point 1** in Fig. 2), which in turn

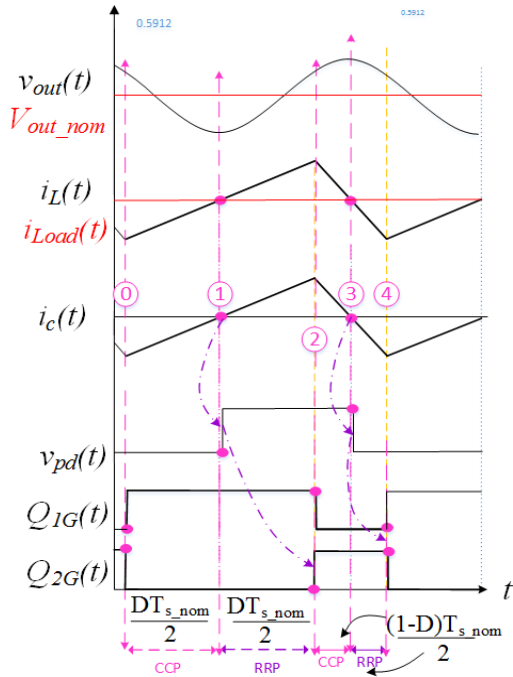


Fig. 2 Key steady-state waveforms of the single mode minimum deviation controller. Top to Bottom: output voltage, nominal output voltage, inductor current, load current, capacitor current, output of zero-current polarity detector output and gating signals of power transistors..

causes the capacitor current polarity to change and become positive. This sends the output of the polarity detector, $v_{pd}(t)$ high. This “sets” the half-duty modulator DPWM₁ which marks the beginning of the on-time ripple reconstruction phase (RRP). Once set, DPWM₁ keeps the converter in its on-state for an additional $DT_{s_nom}/2$ in order to reconstruct its ripple. At this point the output of DPWM₁ will go high and push the converter into its off-state. This is marked by **point 2** in Fig. 2. Now, Q_1 is turned off, Q_2 is turned on and the inductor current is discharging. The first portion of its off-state is again a current correction phase. It will remain in its current correction phase until the instantaneous inductor current equals (or otherwise is less than) the load current. Which occurs at **point 3**. The capacitor current again experiences a change in polarity, setting $v_{pd}(t)$ low. The converter is again in a ripple reconstruction phase. This activates DPWM₂ which keeps the converter in its off-state for an additional $(1-D)T_{s_nom}/2$ to reconstruct the ripple. This is **point 4** in Fig. 2. The output of DPWM₂ then goes high, putting the converter back into its on-state, and the cycle repeats.

In the event of a transient, the controller still operates just as it does in steady-state. However, the load-tracking modulator will extend either the on-time or the off-time (depending on the transient) and thus the period for that cycle to address the transient. This is shown in Fig. 3 for a light-to-heavy transient. As the output of the polarity detector cannot go high until the inductor current equals (or exceeds) the load current, the duration of the CCP of the on-state is automatically extended. Once the inductor current has increased to the point that it equals the load current, the converter enters its RRP and the controller proceeds as before. Heavy to light transients are addressed similarly, however it is the CCP of the off-state that is extended as opposed to that of the on-state. From this it can be seen that this control method requires no special blocks to

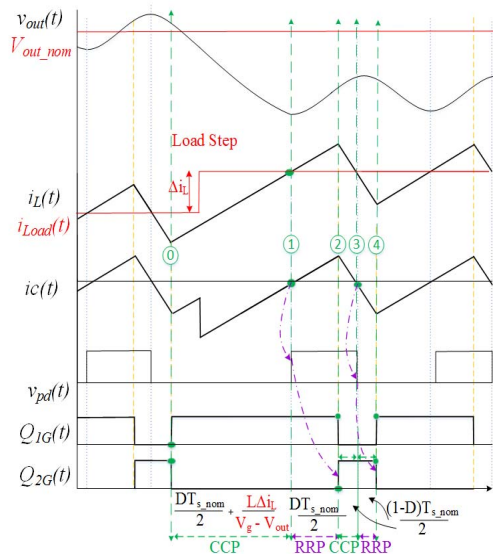


Fig. 3 Relevant signal waveforms during a load transient where the inductor current is corrected. Showing output voltage, nominal output voltage, inductor current, load current, capacitor current, polarity detector output and gating signals.

detect load transients, it simply responds to them as part of its normal operation.

As shown in Fig. 3, there will be an error in the voltage even after the inductor current has been corrected. This happens because some charge is lost before the inductor current is corrected. Voltage recovery is handled by the compensator afterwards as shown in Fig. 4, this is similar to conventional voltage mode control. The speed of this recovery depends on the compensator implemented. This controller may be thought of as a voltage mode controller with one major difference, it is capable of correcting inductor current within a single cycle thus achieving near minimum output voltage deviation. Experimental results taken from a physical prototype are presented in section IV.

A. Analysis of switching period variation

For the converter's on-time, the duration of the current correction phase can be determined by Eq. 1.

$$T_{ON} = \frac{DT_{s_nom}}{2} + \frac{\Delta i_{L_trans}}{\left(\frac{V_g - V_{out}}{L}\right)} \quad (1)$$

Where Δi_{L_trans} is the magnitude of any load step that may have occurred. During steady-state operation $\Delta i_L = 0$, thus the converter's on-time, which is equal to the sum of its CCP and RRP during steady-state operation is found by Eq. 2.

$$T_{ON_SS} = \frac{DT_{s_nom}}{2} + \frac{DT_{s_nom}}{2} = DT_{s_nom} \quad (2)$$

Similarly, in the absence of load-steps, the CCP and RRP of the off-time have equal durations of $((1-D)T_{s_nom})/2$. The sum of these provide the off-time.

$$T_{OFF_SS} = \frac{(1-D)T_{s_nom}}{2} + \frac{(1-D)T_{s_nom}}{2} = (1-D)T_{s_nom} \quad (3)$$

Hence the effective steady-state period T_{SW_SS} , defined as the duration required to complete steps 0 through 4 in the absence of disturbances, will be equal to T_{s_nom} .

$$T_{SW_SS} (1-D)T_{s_nom} + DT_{s_nom} = T_{s_nom} \quad (4)$$

In the case of a load change between points 0 and 1, shown in Fig. 3, the switching period of the converter changes over one switching cycle. In this case, the switching period can be calculated using the same procedure and taking non-zero value of Δi_{L_trans} into account, i.e.

$$T_{SW_trans} = (1-D)T_{s_nom} + DT_{s_nom} + \frac{\Delta i_{L_trans}}{\left(\frac{V_g - V_{out}}{L}\right)}. \quad (5)$$

Similar calculations can be made for a negative load transient. In general the period of the converter will be extended only when a transient occurs. Otherwise, it will be equal to T_{SW_SS} .

B. Extension to Multi-Phase Operation

This control scheme can be extended to multi-phase converters. This is most easily accomplished by comparing the

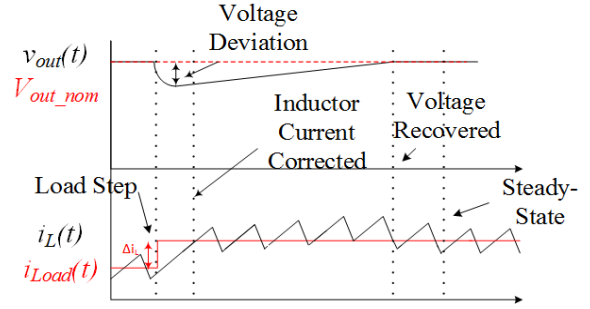


Fig. 4 Relevant signals waveform during the voltage recovery phase neglecting output voltage ripple

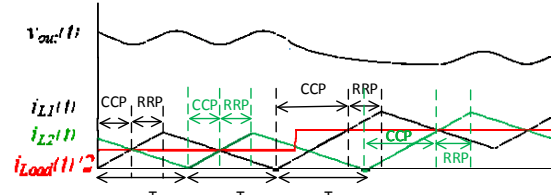


Fig. 5 Output voltage, inductor currents, and load current for control scheme applied to 2-phase buck

inductor current in each phase to half of the load current as opposed to using the estimated capacitor current. Fig. 5 shows key waveforms for the two-phase case where the period is $2T_s$. The modulator behaves much the same as it does in the single-phase case, however instead of using the zero crossing point of the capacitor current (which corresponds to a shift in polarity) it uses the point where the inductor current equals half the load current. Furthermore, the second phase may not enter its on-state until T_s has elapsed after the first phase entered its on-state. Following this approach this control scheme may be extended to n-phases by comparing the current in each phase to the load current divided by n. An added benefit of this control scheme is that it ensures currents are shared equally in multi-phase converters. However, unlike the single-phase implementation, it cannot be implemented with a single non-intrusive sensor. Simulation results for the 2-phase example are provided in section IV.

III. EXPERIMENTAL PROTOTYPE AND PRACTICAL IMPLEMENTATION

A single-phase buck converter based prototype was made with a switching frequency of 600 kHz. Several properties of this prototype are shown in Table 1. As described in section II. This control scheme makes use of the capacitor current. More specifically, this controller requires the accurate detection of changes in the polarity of the output capacitor current. To avoid placing an intrusive sensor in series with the capacitor an estimation circuit is used. This is done by placing an RC circuit in parallel with the output capacitor whose time constant is matched with that of the output capacitor and its ESR [14] - [16]. This is shown in Fig. 6. Previous implementations have demonstrated that auto-matching implementations of this

TABLE I SINGLE-PHASE PROTOTYPE PARAMETERS

Parameter	Value
C_{out}	100 μ F
Power	15W
R_{esr}	10 m Ω
L	3.3 μ H
$F_{SW nom}$	600kHz
V_G	12V
V_{out}	3.3V

approach can accurately detect the capacitor current polarity and zero current crossing points with a low silicon area [16].

Fig. 7 depicts a block diagram of the half-duty DPWM cell. It consists of a counter and a digital comparator. The set pin is triggered by a pulse of any duration. It causes the counter to begin counting up. The output of the half-duty DPWM cell goes high once the counter exceeds the value of the reference supplied to it. The reset pin can also be triggered by a pulse of any duration, and causes the counter to reset to zero. After a reset, the counter will not count until another set pulse has been received. The counter may only be set if the output of the DPWM is low and only reset if the output of the DPWM is high.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To verify the effectiveness of the introduced method an experimental prototype was made based on the diagrams of Figs. 1, 6 and 7. Important parameters of this prototype are shown in Table I. The digital controller is implemented using an FPGA

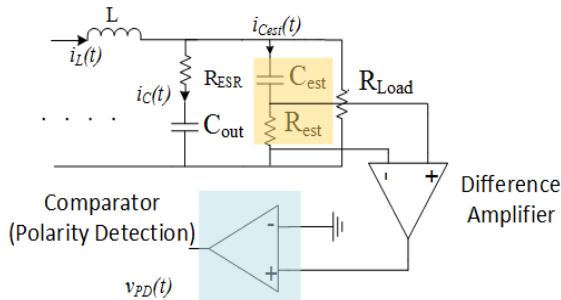


Fig. 6 Capacitor current estimation circuit and polarity detector (simply an analog comparator). The time constant $R_{est}C_{est}$ equals that of $R_{ESR}C_{out}$.

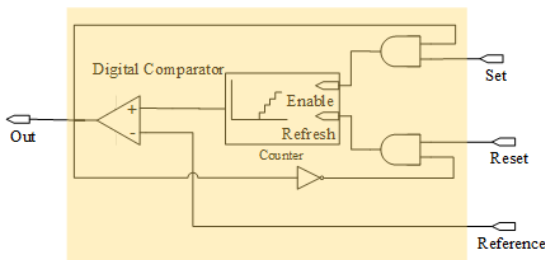


Fig. 7 The structure of the “half-duty” DPWM block that is being used

based system, while the additional analog components, shown in Figs. 1 and 6 are implemented using off-the-shelf ADCs, comparators and operational amplifiers. Fig. 8 depicts simulation results whereas Figs. 9-12 are physical measurements. Fig. 8 shows a simulation of the controller responding to a 4 A, 15% to 100% light to heavy load step. Fig. 9 shows experimental results taken from the prototype for the same transient, while Fig. 10 shows its response to an opposite transient. As in Fig. 8, it can be seen that after the current has been corrected, the voltage ceases to change. This indicates that the current has been correctly adjusted. It can be seen in both Figs. 9.b and 10.b that the inductor current does not change significantly after the initial correction. The compensator then works to recover the lost voltage.

Fig. 11 shows the response of the controller for consecutive load transients. After the first 1.2 A transient occurs the voltage begins to drop, the drop ceases occurring once the current has been corrected. A second 1.6 A transient then occurs which causes the voltage to again drop until the current is corrected. Fig. 12 shows the output voltage during a reference voltage step. This transition occurs smoothly indicating the controller’s stability.

It can be seen that the single mode controller reconstructs the inductor current to its new steady state value over a single switching cycle with near minimum output voltage deviation. Also, it can be seen that due to the single mode of operation a smooth settling of the voltage is achieved without toggling problems often existing in dual mode solutions

Lastly, Fig. 13 shows simulation results for a load-step on a 2-phase converter utilizing the introduced control scheme. In this simulation the control scheme is implemented as described in section II.b. It can be seen that the sum of the inductor currents are made to match the load in just one switching action (per phase) while otherwise causing the converter to behave like a conventional 2-phase interleaved buck converter.

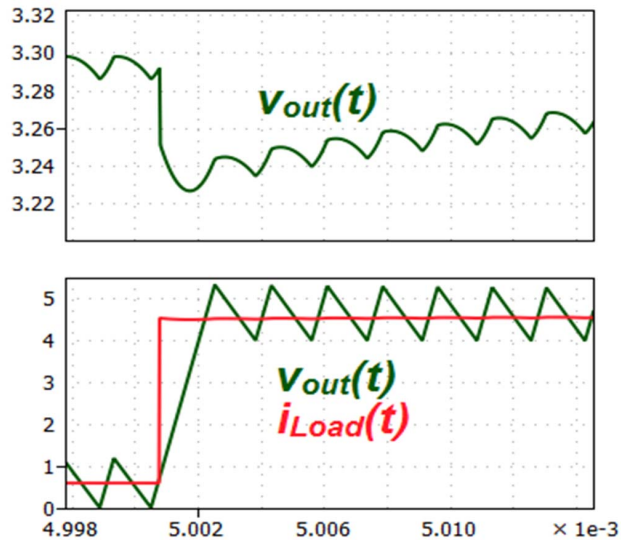


Fig. 8 Simulation results showing the transient response in a single-phase buck converter

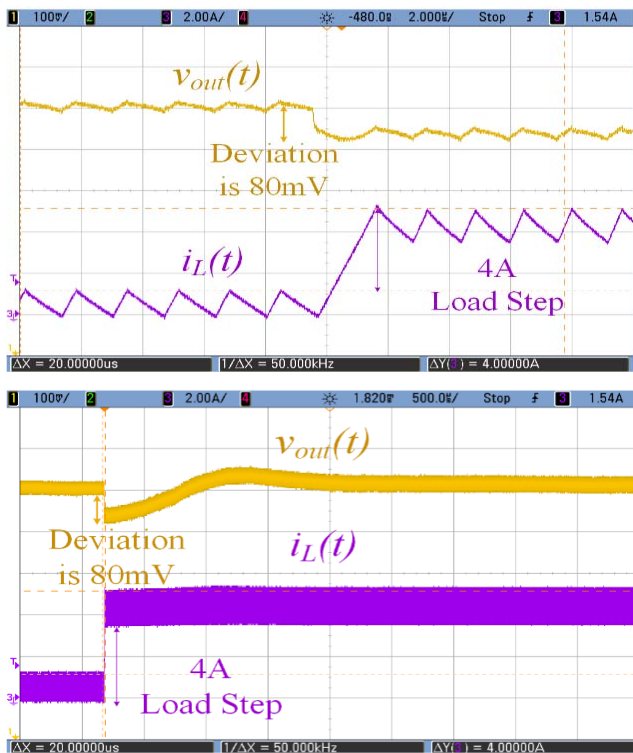


Fig. 9a Oscilloscope screenshot showing output capacitor voltage and inductor current after 4 A light to heavy load step, ($I_{Load} 0.6 \rightarrow 4.6A$). Voltage is 100 mV/div and current is 2 A/div. Timescale is 2 us/div. 9b. Depicts a zoomed-out version of the same load step, showing the voltage recovery phase, timescale set to 500 us/div.

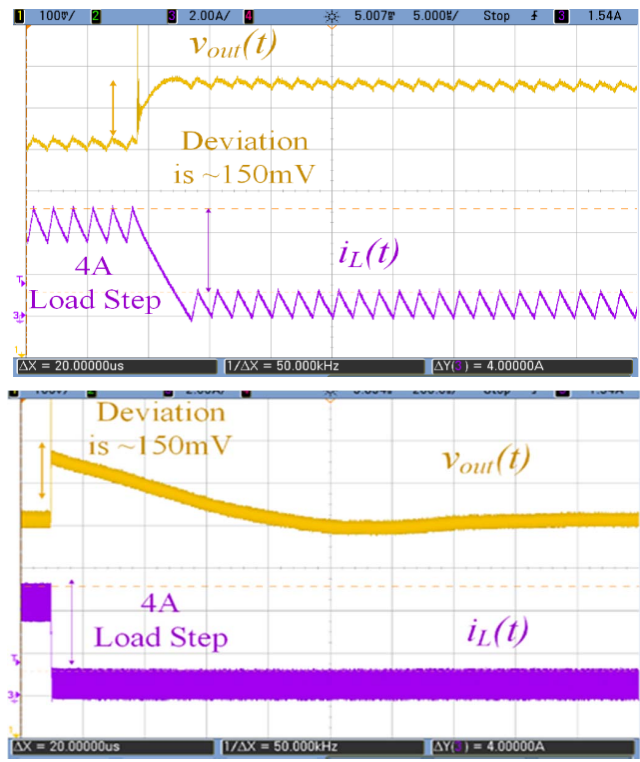


Fig. 10a Oscilloscope screenshot showing the output capacitor voltage and inductor current after load step of 4 A, ($I_{Load} = 4.6 A \rightarrow 0.6A$) The current and voltage scales are 2 A/div and 100 mV/div respectively. Timescale is 5 us/div. 10b. Depicts a zoomed out version of the same load step, showing the voltage recovery phase, timescale is 200 us/div.

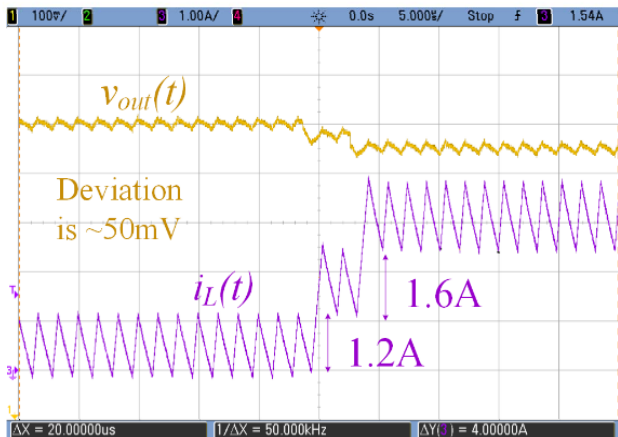


Fig. 11 Oscilloscope screenshot of inductor current and output voltage for consecutive load steps of 1.2A and 1.6 A ($I_{Load} = 0.6A \rightarrow 1.8A \rightarrow 3.4A$). The current scale is 1 A/div, the voltage scale is 100 mV/div, the timescale is 5 us/div.

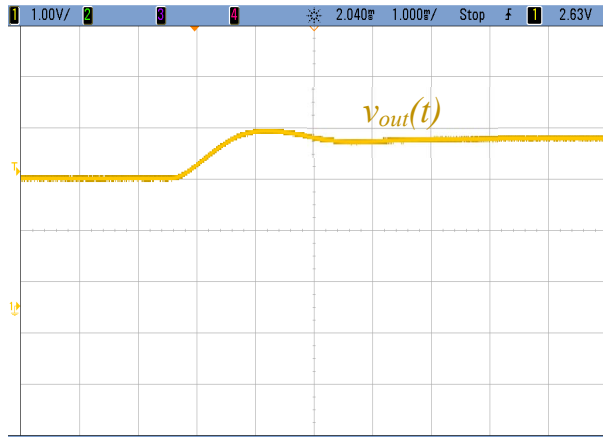


Fig. 12 Oscilloscope screenshot of output voltage shown for a 800mV reference step, the voltage scale is 1V/div whereas the timescale is 1ms/div.

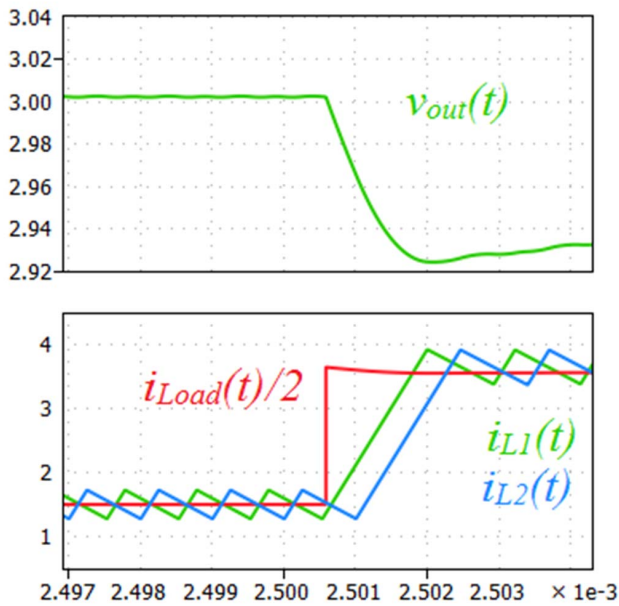


Fig. 13 Simulation results showing the load-transient response for a 2-phase buck converter.

V. CONCLUSIONS

A simple single mode quasi constant-frequency near minimum-deviation control method and its implementation have been presented. The introduced controller provides recovery of the inductor current to its new steady state value in a single switching cycle and, thus, results in nearly the minimum possible output voltage deviation for direct energy transfer converters. The key new element of the controller is load-tracking modulator, which replaces a conventional PWM of a voltage mode controller with two half-duty DPWMs and a capacitor polarity detector. The controller operates in the same manner both in steady-state and during transients eliminating the need for two separate control blocks and, consequently, avoiding mode toggling problems. The effectiveness of the control method has been verified experimentally.

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