Zero-Voltage-Switching Single-Phase Inverter with Active Power Decoupling

Zhengyu Ye, Yenan Chen, Dehong Xu
Institute of Power Electronic
Zhejiang University
Hangzhou, China
21510176@zju.edu.cn

***Abstract*—Active Power Decoupling (APD) is used for single-phase inverter to cope with the double-line frequency power pulsation in the inverter DC side. In this paper, zero-voltage switching (ZVS) for the single-phase inverter with APD is introduced. A ZVS SPWM scheme for single-phase inverter with APD is proposed. The operation of the ZVS single-phase inverter with APD is analyzed and ZVS conditions are derived. Finally, a 500kHz 1.5kW prototype is built to verify the theoretical analysis.**

Keywords—single-phase inverter; Zero-Voltage-Switching; Active Power Decoupling

I. INTRODUCTION

Single-phase inverters are widely used in residential photovoltaic power generations applications. Since there is double-line frequency power pulsation in the DC side of inverter, generally a large electrolytic capacitor is needed at DC bus of PV inverter. It not only decreases the power density, but also may affect the reliability of the inverter due to the short expectancy of the electrolytic capacitor. Various Active Power Decoupling (APD) methods have been investigated by predecessors [1]-[5]. APD composes power converter and smaller capacitor to take the function of power buffer for double-line frequency power pulsation, therefore it decouples double-line frequency power coupling between grid and DC bus of inverter. Among them a buck-type topology [5] is widely used, shown in Fig. 1.

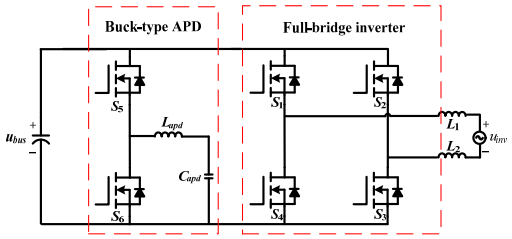


Fig. 1. Single-phase inverter with buck-type APD

Soft switching has been studied to increase the power density and efficiency of inverters. Soft switching was originally introduced to the inverter by using the resonant DC link concept by Prof. Deepak Divan [6][7]. Later ZVS SVM is invented for the three-phase grid inverter, which combines advantage of PWM inverter and soft-switching concept [8]. A ZVS single-phase inverter is proposed in [9] and a ZVS-SPWM scheme is proposed in [10]. With introduction of soft switching and SiC MOSFET, higher efficiency and filter size reduction for the grid inverter are obtained [11]. Up to now, there is no report about soft-switching technology for single-phase ZVS inverter with APD.

In this paper, soft switching technique for single-phase ZVS inverter with APD is studied. Novel ZVS SPWM modulation scheme for single-phase inverter with APD is proposed. By introducing one auxiliary circuit, all switches in both inverter stage, APD stage and auxiliary branch realize ZVS. The operation of the ZVS inverter with APD is analyzed and the ZVS conditions are derived. Finally, experimental results of a 500kHz 1.5kW ZVS APD inverter with inductive load are presented to verify the proposed ZVS modulation scheme.

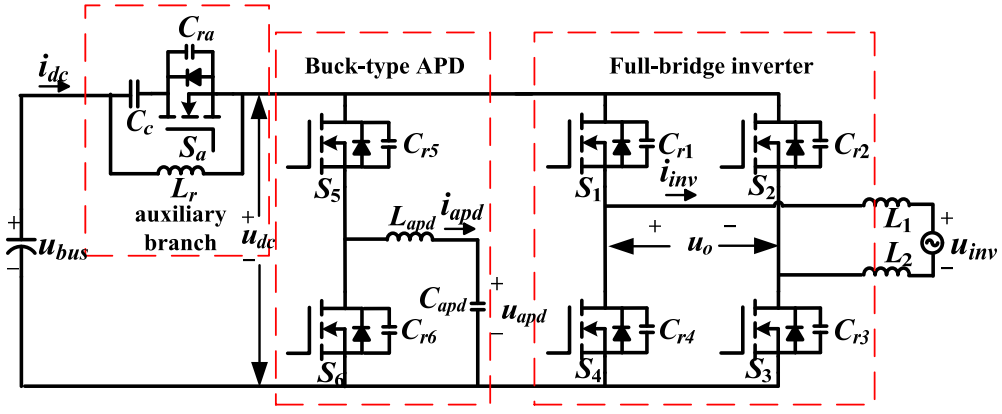


Fig. 2. Proposed ZVS inverter with APD

This work was supported by the National Natural Science Foundation of China (51337009).

II. Circuit and Zero-Voltage-Switching Modulation for Inverter with APD

The ZVS inverter with APD is shown in Fig. 2. An auxiliary branch is introduced to the single-phase inverter with buck-type APD. The auxiliary branch consists of auxiliary switch S_a, clamping capacitor C_c and resonant inductor L_r. Resonant capacitors C_{r1}~C_{r6} and C_{ra} are paralleled respectively to S_1~S_6 and S_a

The output voltage and current of the single-phase inverter $u_{inv}(t)$ and $i_{inv}(t)$ can be expressed as

$$u_{inv}(t) = Usin(\omega t) \quad i_{inv}(t) = Isin(\omega t + \Phi) \quad (1)$$

U is the voltage amplitude , I is the current amplitude, $\omega = 2\pi f$, f is the fundamental frequency, Φ is the power factor.

According to [5], the voltage of APD capacitor u_{apd} and current of APD inductor i_{apd} are represented by:

$$u_{apd}(t) = \sqrt{\frac{UIsin(2\omega t + \Phi)}{2\omega C_{apd}} + \left(\frac{u_{bus}}{\sqrt{2}}\right)^2}$$

$$i_{apd}(t) = \frac{\frac{1}{2}UIcos(2\omega t+\Phi)}{\sqrt{\frac{UIsin(2\omega t+\Phi)}{2\omega C_{apd}} + \left(\frac{u_{bus}}{\sqrt{2}}\right)^2}} \quad (2)$$

In hard switching case, the inverter stage and APD stage may be controlled as shown in Fig. 3. The inverter stage is controlled by double-frequency SPWM. The modulation waveform of the inverter stage is $u_{inv}(t)$ and $-u_{inv}(t)$. The triangular carrier waveform is u_{c1}, and its amplitude is $-u_{bus}$~$+u_{bus}$. The modulation waveform of APD stage is $u_{apd}(t)$. The triangular carrier is u_{c2}, and its amplitude is 0~u_{bus}. The frequency of u_{c2} is twice of u_{c1}.

There are two kinds of current commutation in switch bridge. One type of the commutation is from the body diode of a MOSFET to the another MOSFET in the same phase leg shown in Fig. 4 (a). It can cause higher loss in both the MOSFET to be turned on and the diode to be turned off. The another type of the commutation is from a MOSFET to the body diode of the another MOSFET in the same phase leg as

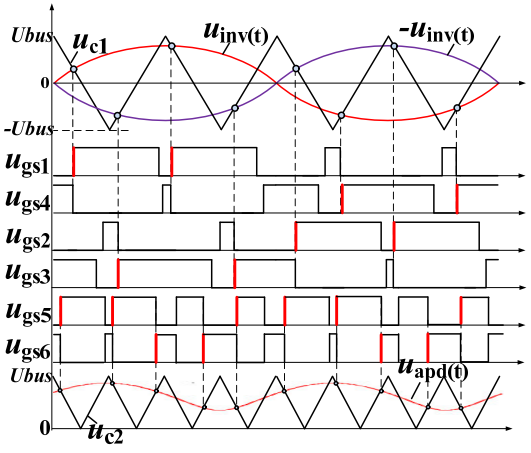


Fig. 3. Hard switching drive signals for inverter and APD

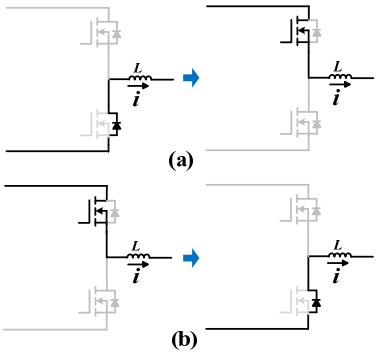


Fig. 4. Current commutation (a) from body diode to MOSFET and (b) from MOSFET to body diode

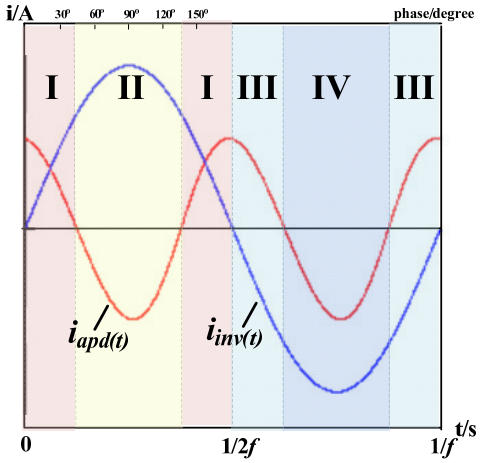


Fig. 5. Polarity of inverter current i_{inv} and APD current i_{apd} in one grid cycle

shown in Fig. 4 (b). Actually ZVS turn-off is realized for the MOSFET to be turned off and ZVS turn-on is realized for the body diode to be turned on. Therefore switching loss is significantly reduced.

The commutation from body diode to MOSFET in inverter stage and APD stage is different according to the polarity of inverter output current i_{inv} and APD inductor current i_{apd}. One grid cycle of inverter output current i_{inv} can be divided into four regions, as shown in Fig. 5, and the commutation process from body diode to MOSFET in different regions is summarized in Table I.

TABLE I COMMUTATIONS FROM BODY DIODE TO MOSFET

Region	i_{inv}	i_{apd}	inverter	APD
I	>0	>0	D_4 to S_1 D_2 to S_3	D_6 to S_5
II		<0		D_5 to S_6
III	<0	>0	D_1 to S_4 D_3 to S_2	D_6 to S_5
IV		<0		D_5 to S_6

In Fig. 3, it is observed that the commutation instants from the body-diode to the MOSFET (marked with red color) of APD stage and inverter stage are not synchronized with symmetrical triangular carrier. In order to realize ZVS turn-off of body diode and ZVS turn-on of MOSFET, the DC side voltage u_{dc} should be discharged to zero by the auxiliary

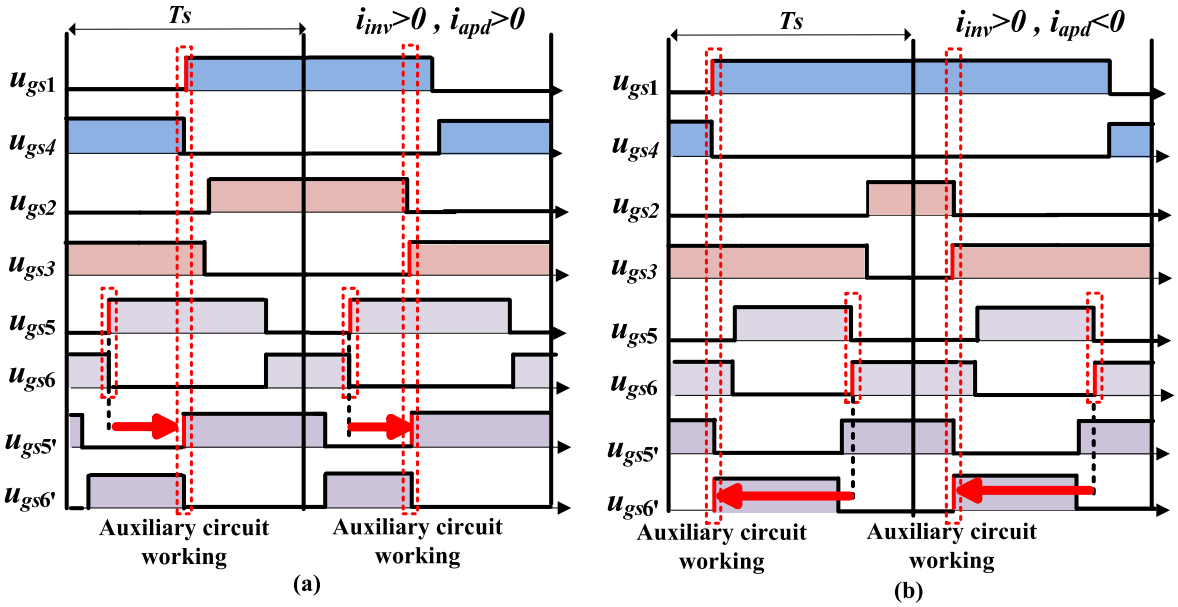


Fig. 6. Synchronize PWM edge of APD stage with inverter stage in (a) Region I and (b) Region II

branch and the switching action of S_a is activated during every commutation from body-diode to MOSFET. The auxiliary branch has to operate multiple times to realize ZVS turn-on of all switches because the commutations with the body-diode in inverter stage and APD stage are asynchronous.

In order to reduce the switching action of auxiliary switch S_a, the commutation from the body diode to the MOSFET in APD stage is synchronized with inverter stage by shifting PWM edge of u_{gs5} and u_{gs6} to u_{gs5}' and u_{gs6}'. The process in Region I and Region II is shown in Fig. 6 (a)(b), T_s is the switching period. The carrier frequency of APD stage is twice of inverter stage. Without changing the pulse width of both the inverter stage and APD stage, ZVS SPWM modulation ensures that the auxiliary branch only needs to operate once during each switching period.

III. Analysis of ZVS Condition

The equivalent circuits in a switching period in Region I ($i_{inv} > 0$, $i_{apd} > 0$) are shown in Fig. 7, and the key waveforms are shown in Fig. 8. u_{sc} is the short-circuit signal added to all switches in Stage 5. The operation stages are analyzed as follows.

Stage 1 (freewheel, t_6~t_1): the output current i_{inv} is freewheeling through the main switches S_3 and S_4. APD inductor current i_{apd} is freewheeling through S_6. This stage is finished by turning off the main switch S_4 and S_6.

Stage 2 (freewheel, t_1~t_2): the main switch S_4 and S_6 are turned off at t_1 by SPWM. Output current i_{inv} is freewheeling through D_4 and S_3, i_{apd} is freewheeling through D_6. This stage is finished by turning off the auxiliary switch S_a.

Stage 3 (resonance, t_2~t_3): The auxiliary switch S_a is turned off at t_2. The resonance among the resonant inductor L_r, the resonant capacitors C_{r1}, C_{r2}, C_{r5} and C_{ra} begins. C_{ra} is charged by L_r, while C_{r1}, C_{r2} and C_{r5} are discharged by L_r. Stage 3 ends when the voltage across capacitors C_{r1}, C_{r2} and C_{r5} is discharged to zero.

Stage 4 (clamping, t_3~t_4): the voltage of C_{r1}, C_{r2} and C_{r5} is resonated to zero. D_1, D_2 and D_5 turn on at t_3. u_{dc} is clamped to zero. The ZVS turn-on condition of main switches S_1, S_2 and S_5 is achieved. Stage 4 ends when all main switches are turned on by ZVS SPWM.

Stage 5 (short-circuit, t_4~t_5): all main switches are ZVS turned on by short-circuit signal at t_4. The resonant inductor starts to store energy, the current in L_r increases lineally. The duration of Stage 5 (t_4~t_5) must be long enough to satisfy the ZVS condition. By the end of this stage, the current of L_r i_{Lr} reaches i_{sc}. Stage 5 ends when main switches S_2, S_4 and S_6 are turned off by ZVS SPWM.

Stage 6 (resonance, t_5~t_6): S_2, S_4 and S_6 are turned off at t_5. Then there begins a resonance among the resonant inductor L_r, the resonant capacitors C_{r2}, C_{r4}, C_{r6} and C_{ra}. C_{ra} is discharged, C_{r2}, C_{r4} and C_{r6} are charged by L_r. Stage 6 ends when the voltage across capacitor C_{ra} is discharged to zero.

Stage 7 (clamping, t_6~t_7): the voltage across capacitor C_{ra} is discharged to zero at t_6. The ZVS on condition of auxiliary switch S_a is achieved. Stage 7 ends when the auxiliary switch S_a is turned on by ZVS SPWM.

Stage 8 (t_7): The auxiliary switch S_a is zero-voltage turned on at t_7. At the end of this stage, the commutation from D_6 to S_5 and D_4 to S_1 is finished. ZVS turn-on of both main switches and auxiliary switch realizes.

From t_7 to t_8, the commutation from MOSFET to body diode of S_3 to D_2 and S_5 to D_6 is triggered by PWM signal, and these processes do not need to resonant u_{dc} to zero.

To realize ZVS turn-on of all switches, the short-circuit current i_{sc} in Stage 5 should meet certain conditions, and can be derived as follows:

The clamping capacitors voltage u_{Cc} can be obtained by using the voltage-second balance principle of the resonant inductor:

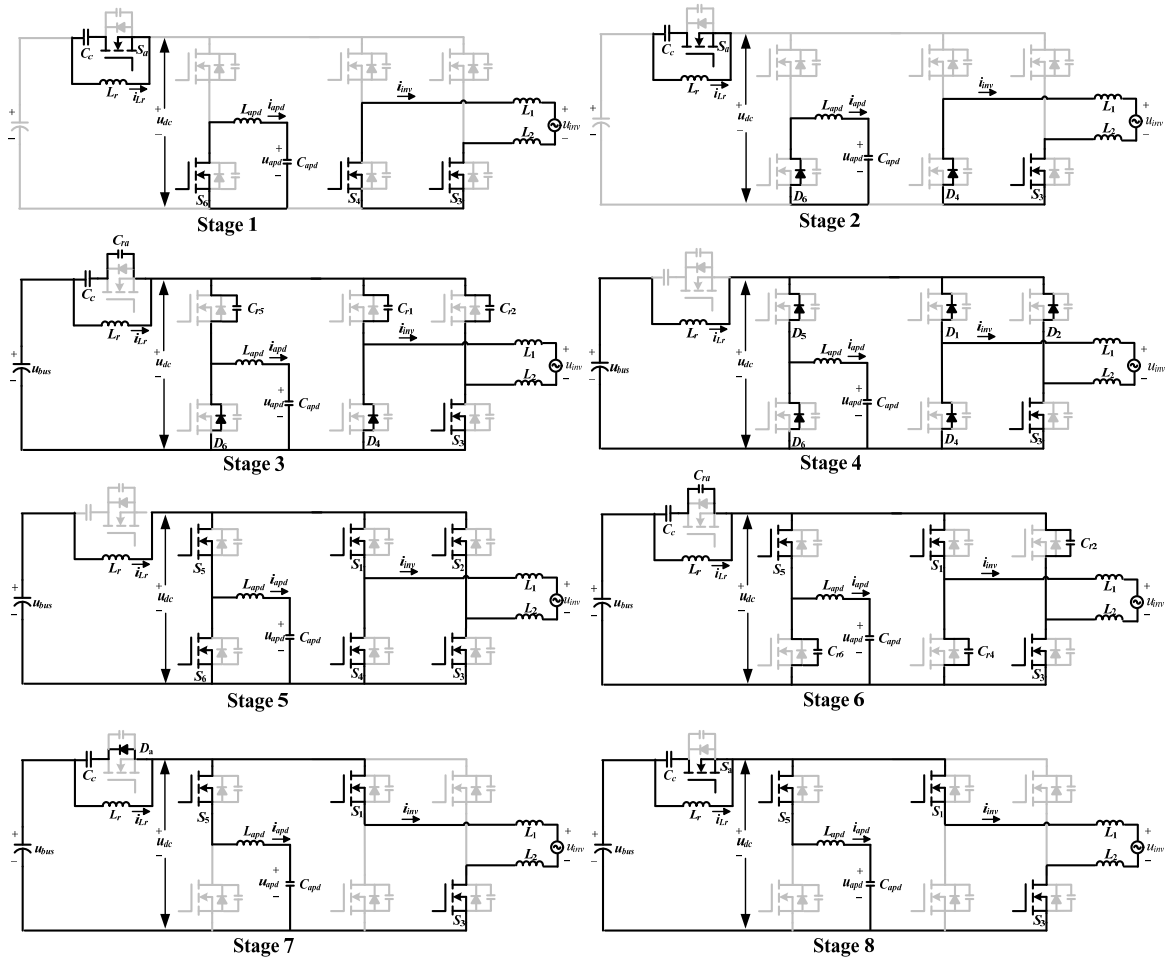


Fig. 7. Equivalent circuits of ZVS stages

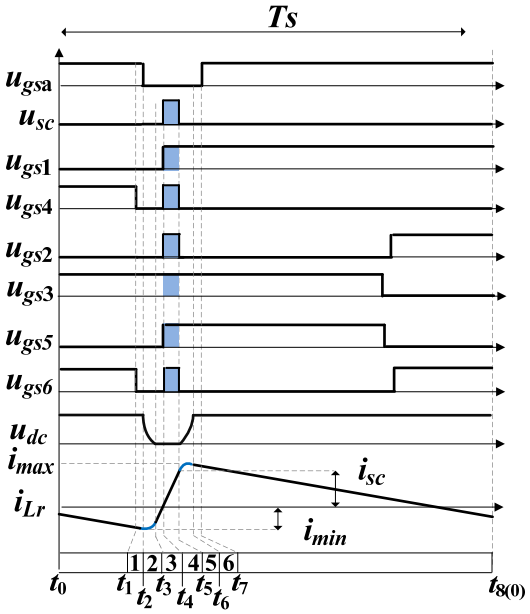


Fig. 8. Key waveforms of ZVS inverter with APD

$$u_{Cc} = \frac{1-D_a}{D_a} u_{bus} \quad (3)$$

Where D_a is the duty cycle of S_a. In order to reduce the voltage stress of all switches, u_{Cc} is always designed much smaller than u_{bus}.

The paralleled capacitors meet the following assumption:

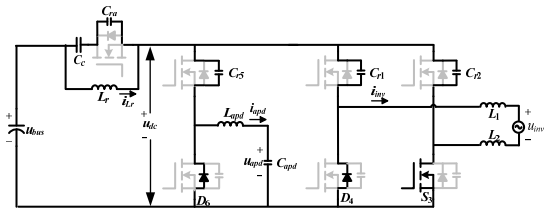
$$C_{r1} = C_{r2} = C_{r3} = C_{r4} = C_{r5} = C_{r6} = C_{rm} = C_{ra} \quad (4)$$

The equivalent circuit of the first resonance progress (Stage 3) in Region I is shown in Fig. 9 (a), and its simplified equivalent circuit is shown in Fig. 9 (b).

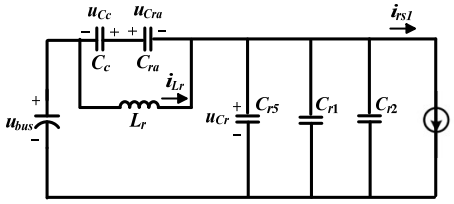
In Fig. 9 (b), i_{rs1} is defined as the current that flows through dc bus at t_2. Its value is given in Table II. The definition of i_{rs1} simplifies later derivations.

TABLE II VALUE OF i_{rs1} AND i_{rs2}

Mode	With APD		Without APD
	$i_{apd} > 0$	$i_{apd} < 0$	
i_{rs1}	0	i_{apd}	0
i_{rs2}	$i_{apd}+\lvert i_{inv}\rvert$	$\lvert i_{inv}\rvert$	$\lvert i_{inv}\rvert$



(a)



(b)

Fig. 9. (a) Equivalent circuit and (b) simplified equivalent circuit of first resonance progress from t_2 to t_3

The resonant equation of this stage is:

$$\begin{cases} u_{Cr}(t) = u_{Cc}cos\omega_r t + [i_{min} - i_{rs1}]Z_r sin\omega_r t + u_{bus} \\ i_{Lr}(t) = -\frac{u_{Cc}}{Z_r} sin\omega_r t + [i_{min} - i_{rs1}]cos\omega_r t + i_{rs1} \end{cases} \quad (5)$$

$$where\ \ \omega_r = 1/\sqrt{L_r C_r},\ \ Z_r = \sqrt{L_r/C_r},\ \ C_r = 3C_{rm} + C_{ra} \quad (6)$$

i_{min} is the initial resonant current of L_r, C_{rm} is the paralleled capacitance of main switches. The minimum value of $u_{cr}(t)$ in (5) must be less than zero to realize the ZVS on operation. We have:

$$i_{min} \le -\sqrt{\frac{u_{bus}^2 - u_{Cc}^2}{Z_r^2}} + i_{rs1} \quad (7)$$

The equivalent circuit of the second resonance progress (Stage 6) in Region I is shown in Fig. 10 (a), and its simplified equivalent circuit is shown in Fig. 10 (b).

Like the definition of i_{rs1}, i_{rs2} is defined as the current that flows through dc bus at t_5. Its value is given in Table II.

The resonant equation of this stage is:

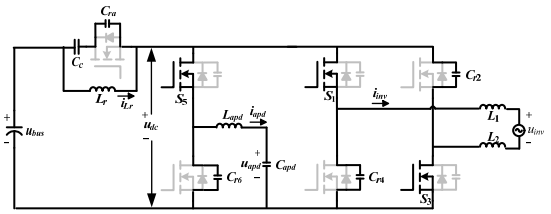
$$\begin{cases} u_{Cra}(t) = u_{Cc} + u_{bus}cos\omega_r t - (i_{sc} - i_{rs2})Z_r sin\omega_r t \\ i_{Lr}(t) = \frac{u_{bus}}{Z_r} sin\omega_r t + (i_{sc} - i_{rs2})cos\omega_r t + i_{rs2} \end{cases} \quad (8)$$

i_{sc} is the short-circuit current of L_r. The minimum value of $u_{cra}(t)$ in Eq. (8) must be less than zero to realize the ZVS on of S_a:

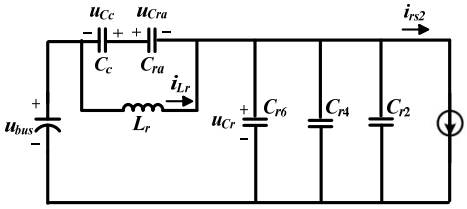
$$u_{Cc} \le \sqrt{{u_{bus}}^2 + (i_{sc} - i_{rs2})^2 Z_r^2} \quad (9)$$

(9) is permanently established because $u_{Cc} \ll u_{bus}$. At the end of Stage 6, the current of L_r i_{Lr} reaches its maximum value i_{max}:

$$i_{max} = \sqrt{\frac{{u_{bus}}^2 - {u_{Cc}}^2}{{Z_r}^2} + (i_{sc} - i_{rs2})^2} + i_{rs2} \quad (10)$$



(a)



(b)

Fig. 10. (a) Equivalent circuit and (b) simplified equivalent circuit of second resonance progress from t_5 to t_6

The average current through the clamping capacitor C_c in a switching period should be zero according to the ampere-second balance of C_c. Therefore, the average current through L_r should be equal to the input current of DC link:

$$\frac{i_{max} + i_{min}}{2} \approx i_{dc} = \frac{p_0}{u_{bus}} \quad (11)$$

Where $p_0 = u_{bus} i_{dc}$ is the total output power.

Combining (7), (10) with (11), the short-circuit current $i_{sc}(t)$ should satisfy following condition:

$$i_{sc} \ge \sqrt{\left[2\frac{p_0}{u_{bus}} - i_{rs1} - i_{rs2}\right]^2 + 4\frac{p_0}{Z_r} - 2\frac{u_{bus}}{Z_r}[i_{rs1} + i_{rs2}]} + i_{rs2} \quad (12)$$

IV. Resonant Parameter Design

An 1.5kW inverter prototype is designed to verify the theoretical derivation,. The DC input voltage is 380V and the modulation ratio 0.82 (output voltage is RMS 220V) . The switching frequency of inverter stage is 250kHz and the switching frequency of APD stage is 500kHz. The output ripple frequency is 500 kHz. The resonant parameters design is discussed as follows [10].

A. Duty cycle of S_a

S_a is turned off from Stage 3 to Stage 6 and the duty cycle of S_a can be derived as:

$$D_a \approx 1 - L_r \frac{i_{max} - i_{min}}{u_{bus} T_s} \quad (13)$$

where T_s is the switching period.

The voltage of DC bus voltage in Stage 4 and Stage 5 is clamped to zero and the energy cannot be delivered from DC link to the load. The duty cycle of auxiliary switch S_a is excepted to be greater than 0.85 to minimize duty cycle loss.

B. Resonant time

The duration of Stage 3 (t_2~t_3) and Stage 6 (t_5~t_6) must be longer than one fourth of a resonant period to guarantee the

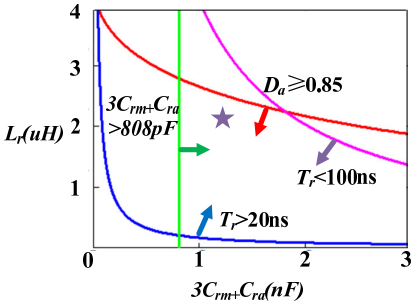


Fig. 11. Resonant parameter design region

completion of a resonant progress. The resonant time T_r is designed to be longer than the turn-off time of SiC MOSFET to reduce the turn-off loss, which is less than 20 *ns*. Its upper limit is expected to be less than 100 *ns* when T_s = 2 *us* to reduce the duty cycle loss. So the limit of the resonant time is given by:

$$20ns \le T_r = \frac{\pi\sqrt{L_r(3C_{rm}+C_{ra})}}{2} \le 100ns \qquad (14)$$

C. Selection of resonant capacitor

SiC-MOSFET C2M0080120D used has output capacitance C_{oss} of 202 *pF*. So the resonant capacitance has a lower limit:

$$3C_{rm} + C_{ra} \ge 4C_{oss} = 808pF \qquad (15)$$

Combining above mentioned design rules, the solution region can be determined as shown in Fig. 11. Finally the resonant inductor L_r is chosen as 2.2 *uH* and each paralleled capacitor for the main switches is 100pF. The auxiliary switch has no external paralleled resonant capacitor.

TABLE III SPECIFICATION OF PROTOTYPE

u_{bus}	380V
inverter modulation ratio	0.82
f_s	500kHz
C_{dc}	20uF
C_{apd}	125uF
MOSFET	C2M0080120D
L_r	2.2uH
C_c	33uF
C_{r1}~ C_{r6}	100pF
L_1&L_2	50uH
C_{inv}	470nF
L_{apd}	175uH
R_o	32Ω / 46Ω/ 95Ω

V. EXPERIMENTAL RESULTS

The circuit and control diagram are shown in Fig. 12. The specification of the prototype is presented in Table. III. The prototype operates with RLC load. The duty ratio of inverter d_{inv} and the duty ratio of APD d_{apd} are calculated by inverter control loop and APD control loop [5] respectively. i_{sc} is

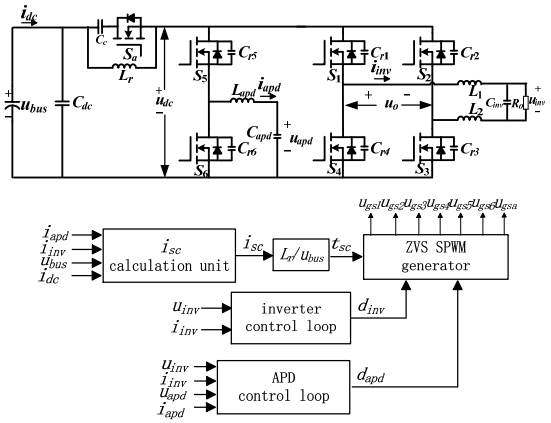


Fig. 12. Experimental circuit and control diagram

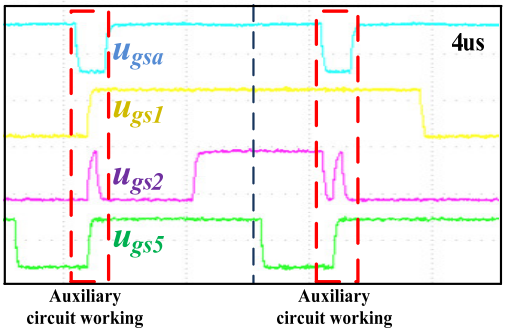


Fig. 13. ZVS SPWM modulation drive signals

calculated by i_{sc} calculation unit using (12). The short-circuit time t_{sc} (t_5-t_4 in Fig. 8) is calculated using

$$t_{sc} = L_r \frac{i_{sc}}{u_{bus}} \qquad (16)$$

d_{inv}, d_{apd} and t_{sc} are sent to ZVS SPWM generator to form the drive signals of u_{gs1}~u_{gs6} and u_{gsa}.

Fig. 13 shows the drive signals of S_a, S_1, S_2 and S_5 in Region I. It can be seen that the drive signal of APD stage (S_5) is synchronized with inverter stage (S_1, S_2) and the auxiliary switch (S_a).

Fig. 14 (a) shows the theoretical resonant inductor short-circuit current i_{sc}, the theoretical maximum resonant inductor current i_{max} and the theoretical minimum resonant inductor current i_{min} of every switching cycle during one fundamental period under 1.5kW operation. Fig. 14 (b) shows the experimental resonant inductor current $i_{Lr}(t)$ during one fundamental period. With control of short-circuit current $i_{sc}(t)$, the maximum and minimum current of resonant inductor $i_{Lr}(t)$ meet the theoretical analysis.

Fig. 15 shows inverter voltage u_{inv} and input current i_{dc} without APD (a) and with (b) APD. It can be seen that the double-line frequency current ripple is greatly reduced with the APD stage.

Fig. 16 shows the resonant inductor current i_{Lr}, the DC-link voltage u_{dc}, the drain-source voltage of S_6 u_{ds6}, the output voltage of inverter stage u_o at different inverter output phase. The DC-link voltage u_{dc} is resonated to zero in each switching period. The duty ratio of both APD stage and inverter stage

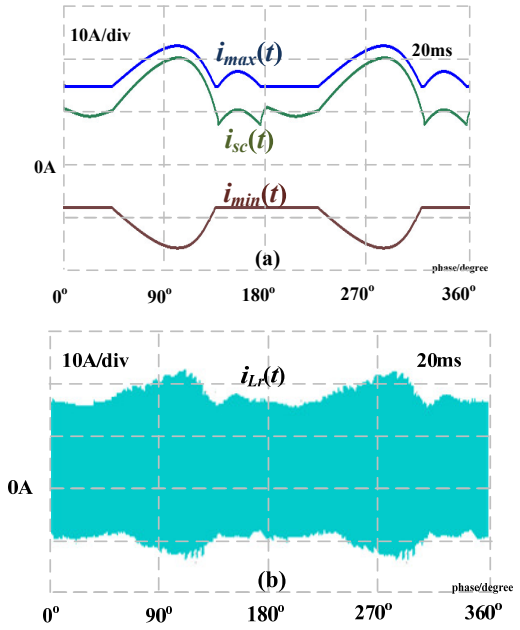


Fig. 14. (a) Theoretical and (b) experimental resonant inductor current

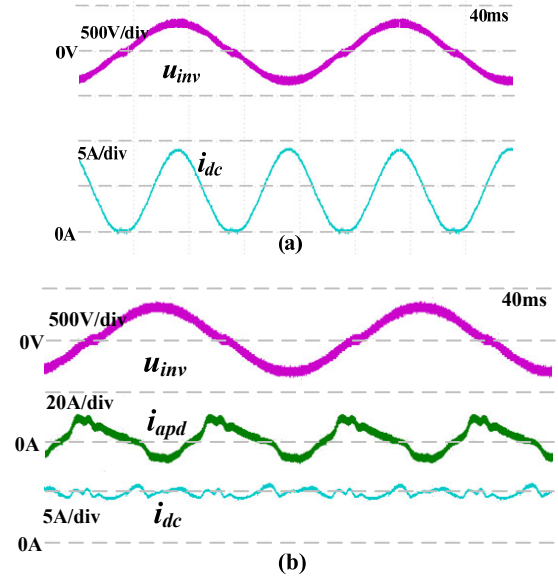
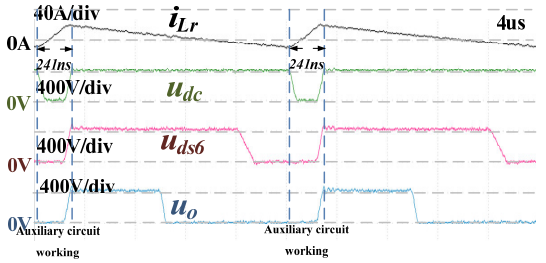


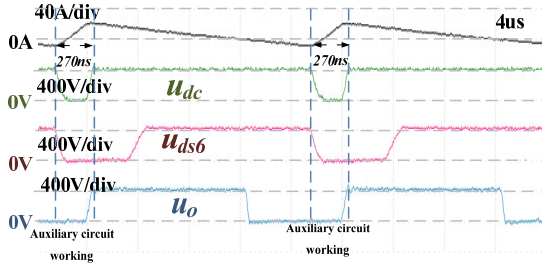
Fig. 15. (a) inverter voltage u_{inv} and input current i_{dc} without APD (b) inverter voltage u_{inv}, APD inductor current i_{apd} and input current i_{dc} with APD

with ZVS SPWM remains the same with traditional PWM. The working time of auxiliary circuit varies because t_{sc} changes with different output phase. According to Table I, if i_{apd} is positive (at 30° & 150°), the commutation of APD stage needs ZVS is D_6 to S_5, the turn-off of D_6 accomplishes during the zero-voltage state of the DC link, as shown in Fig. 16(a) and (d). If i_{apd} is negative (at 60° & 120°), the commutation of APD stage needs ZVS is D_5 to S_6, so the falling edge of u_{ds6} is aligned with the falling edge of u_{dc}.

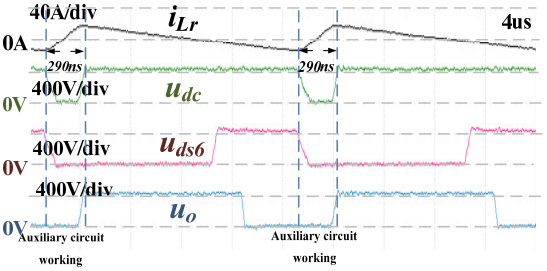
The drive signal of APD switch u_{gs5}, the drain-source voltage of S_5 u_{ds5} and the drain-source voltage of S_2 u_{ds2} with output phase of 30 ° (Region I) is shown in Fig.17 (a), and the driver signal of auxiliary switch u_{gsa} and drain-source voltage u_{dsa} is shown in Fig. 17 (b). The drive signals of S_5 and S_a rise



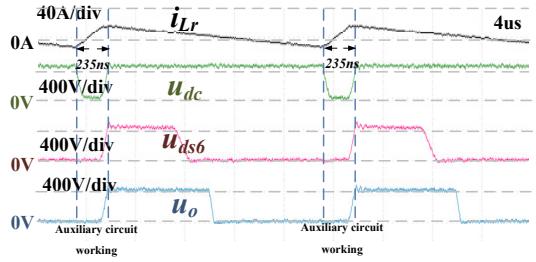
(a) 30° (Region I)



(b) 60° (Region II)



(c) 120° (Region II)



(d) 150° (Region I)

Fig. 16. Resonant inductor current i_{Lr}, dc-link voltage u_{dc}, drain-source voltage of S_6 u_{ds6}, inverter output voltage u_o with different inverter output phase, (a) 30°, (b) 60°, (c) 120°, (d) 150°

after their drain-source voltage is resonated to zero respectively, and ZVS on is realized. The drive signal of APD switch u_{gs6}, the drain-source voltage of S_6 u_{ds6} and the drain-source voltage of S_2 u_{ds2} with output phase of 60 ° (Region II) is shown in Fig. 18 (a), and the driver signal of auxiliary switch u_{gsa} and drain-source voltage u_{dsa} is shown in Fig. 18 (b). The drive signals of S_6 and S_a rise after their drain-source voltage is resonated to zero respectively, and ZVS on is realized.

The efficiency comparison under different load conditions between soft-switching and hard-switching is shown in Fig.19. The efficiency of ZVS inverter with APD is higher than hard-

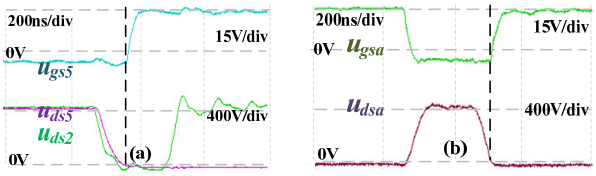


Fig. 17. ZVS realization with 30° inverter output phase
(a) main switches, (b) auxiliary switch

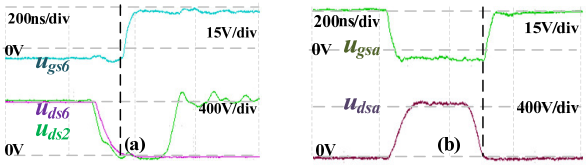


Fig. 18. ZVS realization with 60° inverter output phase
(a) main switches, (b) auxiliary switch

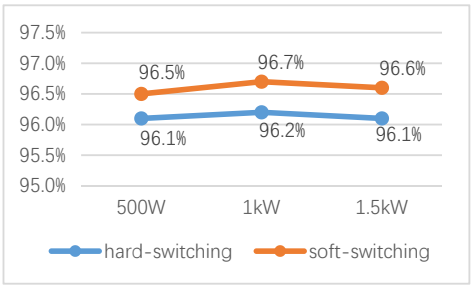


Fig. 19. Measured efficiency of ZVS single-phase inverter with APD

switching inverter under different load conditions, and the highest efficiency of soft-switching is 96.8% under 1kW load condition.

VI. Discussion

The commutation from the MOSFET to the body diode in Fig.4 (b) can realize ZVS turn-on of MOSFET with sufficient dead time. However, the conduction loss of SiC MOSFET's body diode during the dead time is not negligible due to higher voltage drop of the body diode. Shorter dead time can reduce the conduction loss of the body diode, however the turn-off of MOSFET may not be finished with small load current. As shown in Fig.20 (a), the turn-off of S_6 is still proceeding and S_5 is hard-switching turned on at the end of dead time, which happens when instant load current is near zero. Longer dead time ensures ZVS turn-on, shown in Fig.20 (b), but increases conduction loss of the body diode. During the current commutation from the MOSFET to the body diode, dead time needs to be carefully selected when i_{apd} and i_{inv} are near zero. The tradeoff between the conduction loss of body diode and switching loss will be considered in the future work.

The inverter stage operates in open-loop mode with fixed modulation ratio. The short-circuit time t_{sc} is pre-calculated using ideal conditions with theoretically i_{apd} and zero i_{dc} ripple. According to Fig.15 (b), in the experiment APD inductor current i_{apd} is not fully sinusoidal, and there is current ripple in i_{dc}. Therefore, the ZVS turn-on condition is not fully realized at some phase degrees, which causes higher loss. To realize ZVS conditions in all range, close-loop control of inverter and real-time computation of short circuit time t_{sc} is needed. In addition, the resonant inductor should be more carefully designed to minimize inductor loss due to its flowing current i_{Lr} with high frequency and high amplitude.

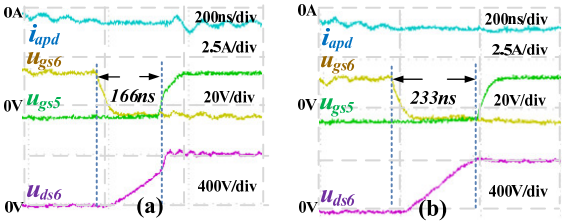


Fig. 20. Commutation from the MOSFET to the body diode
(a) with shorter dead time, S_5 hard-switching turned on, (b) with longer dead time, S_5 ZVS turned on

VII. Conclusion

A ZVS modulation scheme for single-phase inverter with APD is proposed. The stage analysis is provided and the ZVS condition is derived. The theoretical analysis is verified on a 500 kHz 1.5kW prototype with RLC load with open loop control. The double-line frequency ripple of DC input current is reduced and ZVS is realized.

Up to now, the conversion efficiency is lower than we expect. Further study is required such as operation range vs. ZVS condition. Since the APD inductor current waveform is not sinusoidal, it affects the ZVS switching condition of APD leg. There is higher loss in resonant inductor and its optimization is needed.

Reference

[1] Z. Qin, Y. Tang, P. C. Loh and F. Blaabjerg, "Benchmark of AC and DC active power decoupling circuits for second-order harmonic mitigation in kW-scale single-phase inverters," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 2514-2521.

[2] H. Li, K. Zhang, H. Zhao, S. Fan and J. Xiong, "Active Power Decoupling for High-Power Single-Phase PWM Rectifiers," in IEEE Transactions on Power Electronics, vol. 28, no. 3, pp. 1308-1319, March 2013.

[3] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin and P. Wang, "Decoupling of Fluctuating Power in Single-Phase Systems Through a Symmetrical Half-Bridge Circuit," in IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 1855-1865, April 2015.

[4] X. Lyu, N. Ren, Y. Li and D. Cao, "A SiC-Based High Power Density Single-Phase Inverter With In-Series and In-Parallel Power Decoupling Method," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 3, pp. 893-901, Sept. 2016.

[5] D. Neumayr, D. Bortis and J. W. Kolar, "Ultra-compact Power Pulsation Buffer for single-phase DC/AC converter systems," 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, 2016, pp. 2732-2741.

[6] D. M. Divan, "The resonant DC link converter-a new concept in static power conversion," IEEE trans. Industrial Applications, vol. 25, no. 2, pp. 317-325, Mar/Apr. 1989.

[7] D. M. Divan, and G. Skibinski, "Zero-switching-loss inverters for high power applications," IEEE trans. Industrial Applications, vol. 25, no. 4, pp. 634-643, Jul/Aug. 1989.

[8] R. Li and D. Xu, "A Zero-Voltage Switching Three-Phase Inverter," in IEEE Transactions on Power Electronics, vol. 29, no. 3, pp. 1200-1210, March 2014.

[9] M. Mezaroba, D. C. Martins and I. Barbi, "A ZVS PWM full-bridge inverter with active clamping technique using the reverse recovery energy of the diodes," IEEE 2002 28th Annual Conference of the Industrial Electronics Society. IECON 02, 2002, pp. 621-626 vol.1.

[10] Y. Chen et al., "A ZVS Grid-Connected Full-Bridge Inverter With a Novel ZVS SPWM Scheme," in IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3626-3638, May 2016.

[11] Y. Li, Zhengyu Ye, Ning He, Junxiong Wu, Changsheng Hu and D. Xu, "Efficiency improvement of a SiC-MOSFET 500 kHz ZVS inverter," 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Vancouver, BC, 2016, pp. 1-8.