A Common-Ground Single-Phase Five-Level Transformerless Boost Inverter for Photovoltaic Applications

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***Abstract* — This paper presents a transformerless five-level boost inverter with common ground connection for single-phase photovoltaic (PV) systems. It consists of nine switches, two capacitors, and an LC filter at the output. The topology eliminates common mode (CM) leakage current by connecting the negative terminal of the PV directly to the neutral point of the grid, which bypasses the PV array's stray capacitance. As compared to the conventional flying capacitor (FC) multilevel inverter and the cascaded H-bridge (CHB) multilevel inverter, the proposed topology achieves an output voltage that is up to four-times higher given an equivalent dc-link voltage. This reduces the dc-link voltage requirement to one fourth of the values used in conventional multilevel inverters (FC, CHB, NPC, ANPC) and one half of the conventional H-bridge topologies. The following manuscript presents the operation principles and theoretical analysis of the proposed topology, which are supported by simulation and experimental results. A 1 kW prototype was constructed; it achieves 96 % efficiency operating at an output of 240 V_{AC}, 60 Hz, and 973 W.**

Keywords— Common mode (CM) current; photovoltaic (PV) system; switched capacitor; transformerless inverter; virtual DC bus.

I. INTRODUCTION

The rate of solar energy deployment has increase rapidly due to concerns for the environment and a reduction in the system level costs of photovoltaic (PV) systems. In residential applications, the cost of this hardware has decreased 61 % between 2010 and 2017 [1]. Yet, there are still many opportunities for improvement, especially in the power electronics used in these systems.

It is typical to use a transformer in PV applications to provide galvanic isolation between the panel and grid as well as to achieve a high voltage conversion ratio. However, the transformer adds additional weight and cost to the hardware and it decreases its efficiency [2]. For these reasons, researchers have examined various transformerless topologies as a means of mitigating these concerns [2] – [5].

Multilevel inverters exhibit some interesting advantages compared to two-level voltage source inverters (VSIs), especially for higher voltage power conversion, where lower switch voltage stress and lower harmonic content exist [6]-[10]. For grid connected applications, multi-level topologies are more common due to their advantages of improved output current, lower switching losses and reduced electromagnetic interference (EMI). In multi-level topologies, low voltage switches can be used instead of high voltage switches as in two-level inverters. Low voltage switches are normally smaller and cheaper and can handle higher switching frequencies. In addition, the conduction losses are reduced due to a lower forward-voltage drop, and the switching loss is reduced due to the smaller dv/dt. Furthermore, two-level topologies need to switch more often than multi-level topologies to achieve the same output quality. Thus, the switching frequency can be reduced in multi-level topologies and thereby, the associated switching losses. Furthermore, multi-level topologies offer more than two voltage levels and this improves the output voltage waveform by better approximating a sine-wave.

Despite the advantages listed above, the main drawback of multilevel inverters is the requirement of a higher dc-link voltage (two times the peak ac output voltage for most of the NPC, ANPC, FC family topologies). This requires an additional front-end step-up dc-dc converter, or a string of series connected PV modules to lift the dc-link voltage from 400 V - 800 V for active power control to the grid. While this can be done with an inductive based boost converter, switch-capacitor circuits also offer boost functionality while being able to maintain a higher power density over converters that employ magnetic elements [11]-[12]. Recently, the advantages of switched-capacitor topologies have been demonstrated in PV applications [13]-[15].

Considering these aspects, a novel common ground type five-level single phase boost inverter is investigated in this paper for PV applications. It reduces the dc-link voltage requirements up to ¼ of the value in conventional multilevel topologies and ½ of the value in traditional H-bridge inverter. The common mode leakage current to the grid is eliminated by connecting the negative terminal of the PV directly to the neutral point of the inverter.

The structure of the rest of the paper is as follows. In Section II, the operating principles for the proposed topology are reviewed. Section III provides detailed analysis of each of the switching states. The capacitor sizing requirements are presented in Section IV. This is followed by simulation results in Section V. In Section VI, experimental results are provided for the inverter at rated voltage and power. The conclusions to this work are in Section VII.

II. Operating Principles of Proposed Topology

A. Principle of operation

The proposed topology works on the principle of a 'flying capacitor', which is illustrated in Fig. 1. The capacitor C_{FC} is charged to V_{DC} when the switches are in *position 1*. When the switches are in *position 2*, it produces an equal and opposite polarity across the terminal *ab*. During this state, the capacitor is typically discharged. This concept of a flying capacitor has been utilized in various modern common-ground transformerless inverters [2]. The utilization of only capacitors as the primary energy storage elements is beneficial in terms of the overall cost and weight of a power converter in contrast to the utilization of both capacitors and inductors.

B. Proposed topology

The proposed topology is a transformerless, five-level boost inverter. As shown in Fig. 2a, it utilizes nine switches and two flying capacitors to realize five discrete output voltages: 2 V_{DC}, V_{DC}, 0, V_{DC}, - V_{DC} and -2 V_{DC}. To accomplish this, S_1 must be bidirectional blocking. It can be implemented using a back-to-back connection, or a device with a reverse blocking diode as shown in Fig. 2a. During the inverter's operation, the flying capacitors are charged in parallel and discharged in series or parallel depending on the magnitude of the output voltage. Additionally, it is implemented with a common ground connection between the negative terminal of the photovoltaic panel (PV) and the neutral connection of the grid. This eliminates the common mode leakage current since the PV's parasitic capacitance is bypassed.

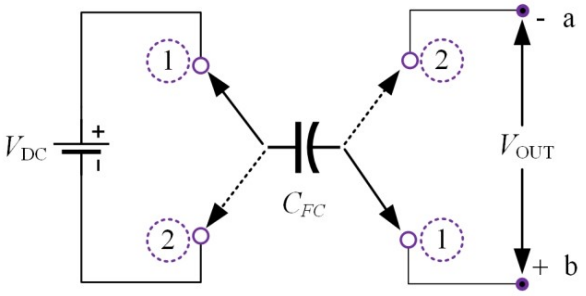


Fig. 1 Principle of operation of virtual DC bus capacitor.

The control strategy for the inverter is shown in Fig. 2b. A traditional multi-carrier approach is used where the switching signals are generated by comparing four carrier waves (v_{P2}, v_{P1}, v_{N1}, and v_{N2}) to a reference waveform (v_{REF}):

$$v_{REF}(\theta) = 2m_a \sin(\theta), \tag{1}$$

where $\theta = \omega_c \cdot t$, ω_c is the angular frequency, and m_a is the modulation index. Thus, the RMS value of output voltage (V_{OUT}) for the proposed topology is:

$$V_{OUT} = \frac{2 \cdot m_a \cdot V_{DC}}{\sqrt{2}}. \tag{2}$$

The operation of the inverter can be broken up into four regions that correspond to a specific range of values for the reference waveform. The relationship is given in Table I and illustrated in Fig. 2b. For each region of operation, the inverter switches between two different states. Most of the switches are

TABLE I. Region of Operation for the Propose Topology

Region	v_{REF}	Low State	High State
1	$1 < v_{REF}(\theta) \le 2$	A (+ V_{DC})	B (+ 2V_{DC})
2	$0 < v_{REF}(\theta) \le 1$	C (0)	A (+ V_{DC})
3	$-1 < v_{REF}(\theta) \le 0$	D (- V_{DC})	C (0)
4	$-2 < v_{REF}(\theta) \le -1$	E (-2 V_{DC})	D (- V_{DC})

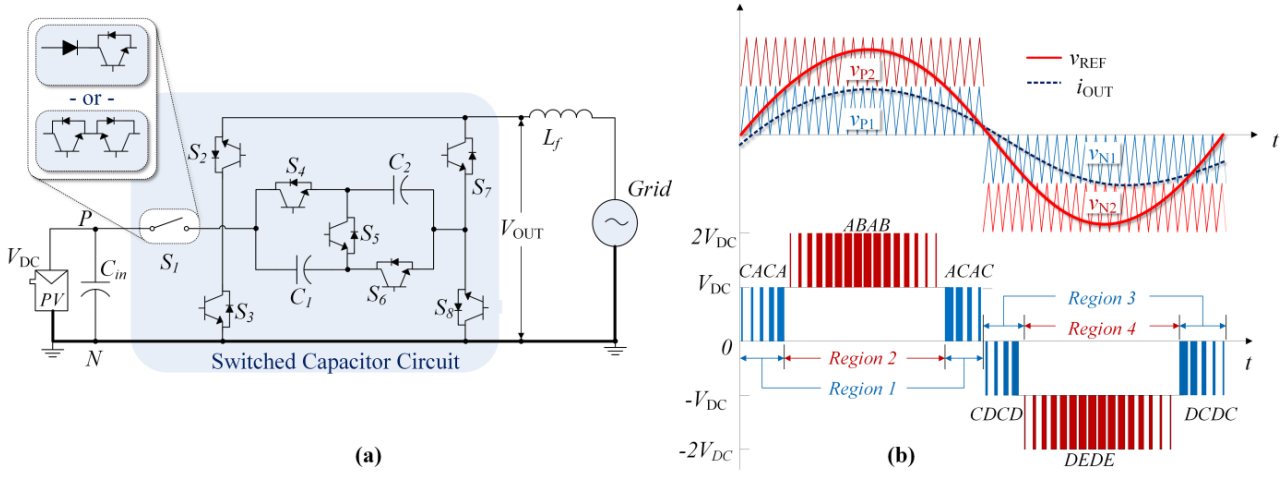


Fig. 2 The proposed 5-level transformerless inverter's (a) circuit diagram and (b) the corresponding PWM modulation scheme.

static while either two or three are modulated using SPWM to produce the output. During *Region 1*, S_2 and S_7 are complimentary and the remaining switches are static. The inverter switches between 0 and V_{DC}. In *Region 2*, S_4 and S_6 switch together and are compliments of S_5. During *Region 3*, S_3 and S_8, are complimentary. In *Region 4*, S_4 and S_6 are compliments of S_5 just like *Region 2*.

The capacitors are fully charged once per cycle. As explained in the next section, charging occurs during *State A* and *State C* when the output voltage is + V_{DC} and 0 V_{DC}, respectively. However, to realize the + 2 V_{DC} output and the negative output states, the capacitors will function as a virtual DC bus [3]. Furthermore, it can be seen that charging does not occur during *Region 4*. Therefore, the capacitors' voltage will decrease during this time, and the capacitors will need to be sized according to the output power, the fundamental frequency, and the capacitor's ripple voltage requirements

III. Operating Modes of the Proposed Topology

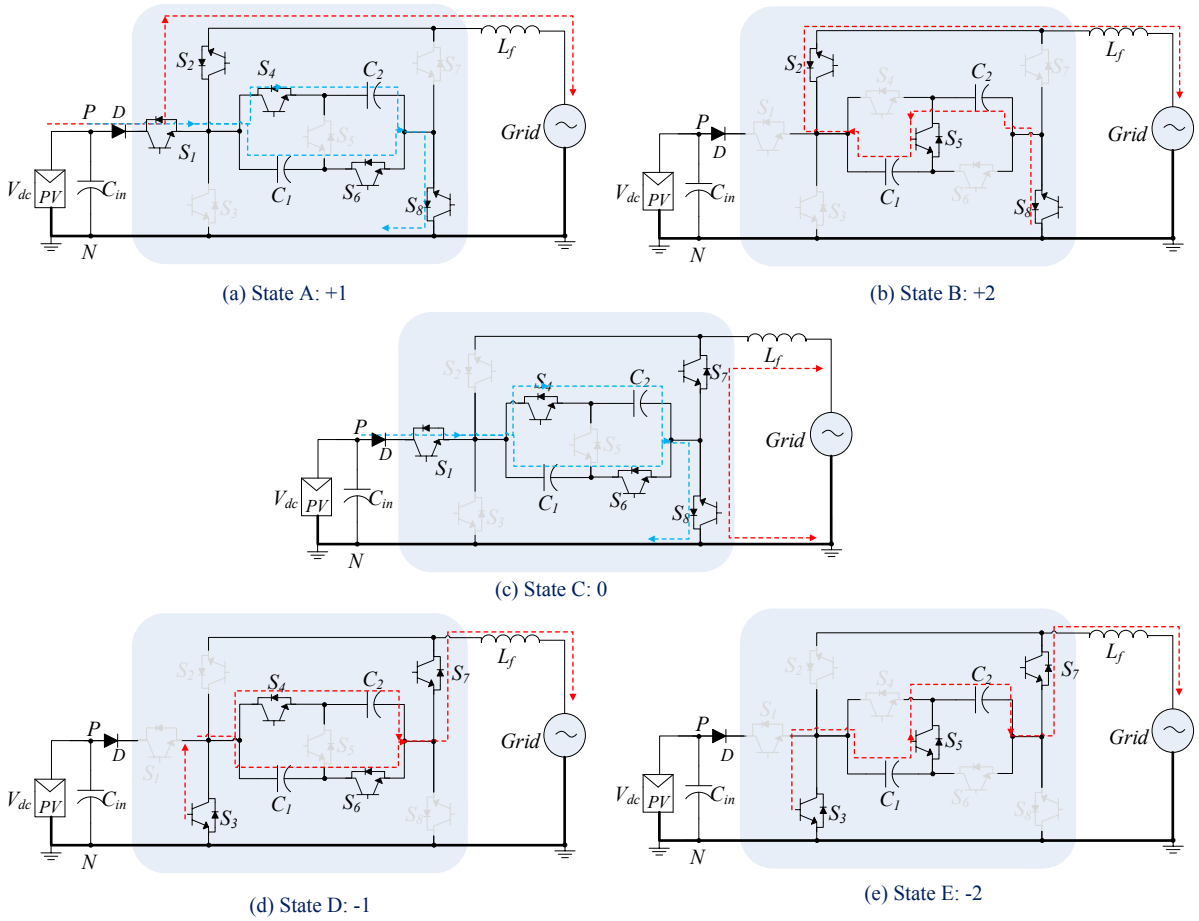
The proposed inverter has five operating states as shown in Fig. 3. The status of the switches during each state and the corresponding output voltage is given in Table II. Each state will be described in the subsections to follow.

A. State A (+1 level):

Fig. 3a shows *State A*. In this state, the output of the inverter before the filter is + V_{DC}. The capacitors C_1 and C_2 are charged in parallel through the switches S_1, S_4, S_6 and S_8. During this state, C_1 and C_2 also act as an additional dc-link capacitor. In *Region 1*, *State A* occurs when v_{REF} is greater than v_{P1}. In *Region 2*, it occurs when v_{REF} is less than v_{P2}.

B. State B (+2 level):

State B is shown in Fig. 3b; it is only utilized in *Region 2*. It produces a voltage level of +2 V_{DC} at the filter's input by connecting the pre-charged capacitors (C_1 and C_2) in series via S_5. To prevent a short circuit to the capacitors, S_4 and S_6 are off. It is active when v_{REF} is greater than v_{P2}.



(a) State A: +1

(b) State B: +2

(c) State C: 0

(d) State D: -1

(e) State E: -2

Fig. 3 Five switching states of the proposed 5-level transformerless inverter.

TABLE II. FIVE SWITCHING STATES OF THE INVERTER.

State	V_{OUT}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	$+V_{DC}$	1	1	0	1	0	1	0	1
B	$+2V_{DC}$	0	1	0	0	1	0	0	1
C	0	1	0	0	1	0	1	1	1
D	$-V_{DC}$	0	0	1	1	0	1	1	0
E	$-2V_{DC}$	0	0	1	0	1	0	1	0

C. State C (0 level):

State C, shown in Fig. 3c, is utilized in *Regions 1* and *3*. The switches S_7 and S_8 are closed to form a bidirectional path for current to flow during both the positive and negative cycle zero states. This leads to a zero voltage being applied before the output filter. The switch S_2 is off during this state, which allows the capacitors to be charged in parallel through switches S_1, S_4, S_6 and S_8. S_5 is off in this state to prevent short circuit of the capacitors. In *Region 1*, *State C* occurs when v_{REF} is less than v_{P1} and in *Region 3*, it is active when v_{REF} is greater than v_{N1}.

D. State D (-1 level):

Fig. 3d shows *State D* in which the capacitors C_1 and C_2 are connected in parallel to provide a dc-link voltage of $-V_{DC}$. During this mode, S_3, S_4, S_6 and S_7 are on, and S_5 and S_8 are off. Assuming C_1 and C_2 are equal, the grid current (I_{OUT}) splits equally between the two capacitors. Switch S_1 is off during this state to prevent a short on the DC input. Switch S_2 remains off for the complete negative cycle. In *Region 3*, *State D* is active when v_{REF} is less than v_{N1} and in *Region 4*, it takes place when v_{REF} is greater than v_{N2}.

E. State E (-2 level):

This switching state (see Fig. 3e) is similar to *State B* in which the capacitors are connected in series to boost the voltage level. However, S_1, S_2, and S_8 are off, S_3 and S_7 are on, and the capacitors are connected with reverse polarity to the output filter. As in *State B*, by turning off S_4 and S_6 and turning on S_5, the capacitors are connected in series rather than parallel to the output filter, doubling the voltage. During this mode, the current in C_1 and C_2 is equal to I_{OUT}. The result is $-2\ V_{DC}$ is applied to the output filter. *State E* occurs during *Region 4* when v_{REF} is less than v_{N2}.

F. Voltage Stress on Transistors:

The voltage stress on the transistors is not symmetrical. Upon examining the schematics for *State B* and *State E*, it can be seen that some of the transistors have to block two times V_{DC}. On the other hand, some of the transistors must only block V_{DC}. The ratings for each switch are summarized in Table III.

TABLE III. SWITCHING STRESS FOR EACH TRANSISTOR

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
V_{DC}	$2\ V_{DC}$	$2\ V_{DC}$	V_{DC}	V_{DC}	V_{DC}	$2\ V_{DC}$	$2\ V_{DC}$

IV. CAPACITOR SIZING

To successfully implement a flying capacitor topology, the capacitor(s) must be sized appropriately. In the proposed topology, their size is a function of the average discharging current in the capacitor, the fundamental frequency, the output power, the dc-link voltage, and the voltage ripple requirements of the capacitor. To determine this value, the following analysis makes three assumptions. First, the output current is purely sinusoidal, which is a reasonable assumption if the corner frequency of the output filter is well below the switching frequency. Second, the capacitor is completely charged when it moves from *Region 3* to *Region 4*. While the capacitors will be discharged some, it will typically be small because charging and discharging does occur simultaneously in *Region* 3. Additionally, the load current is small in *Region 3* when the power factor is close to one. Third, the capacitance of C_1 and C_2 are equal.

To begin the analysis, the duration of *Region 4* needs to be defined. Equation (1) is manipulated to determine the angle (θ_1) where the inverter moves into *Region 4*:

$$\theta_1 = \sin^{-1}\left(\frac{1}{2 \cdot m_a}\right) + \pi . \tag{3}$$

Due to quarter-wave symmetry, π is dropped from (3) with the understanding that the results are not changed and the analysis is simplified. The voltage ripple on the capacitor (Δv_{C_i}) is approximated by using the discharge time (t_{DIS}), the average current (I_{AVG}) out of the capacitor, and the size of the capacitor (C_i):

$$\Delta v_{C_i} = \frac{I_{AVG} \cdot t_{DIS}}{C_i} . \tag{4}$$

The discharge time is determined using the result from (3):

$$t_{DIS} = \frac{\pi - 2 \cdot \theta_1}{\omega_c} . \tag{5}$$

This is also the amount of time that the inverter operates in *Region 4*. Next, the average current in the capacitors ($I_{AVG,C,R4}$) during *Region 4* is determined:

$$I_{AVG,C,R4} = \frac{1}{\pi - 2 \cdot \theta_1} \int_{\theta_1}^{\pi - \theta_1} i_{C,R4}(\theta) d\theta . \tag{6}$$

The instantaneous current through the capacitor ($i_{C,R4}$) is determine by whether the inverter is in *State D* or *State E*. It can be represented as:

$$i_{C,R4}(\theta) = \begin{cases} \frac{1}{2} I_{OUT}(\theta), & v_{N1}(\theta) \geq v_{REF}(\theta) \geq v_{N2}(\theta) \\ I_{OUT}(\theta), & v_{REF}(\theta) \leq v_{N2}(\theta) \end{cases} . \tag{7}$$

Here the negative sign associated with the Passive Sign Convention is dropped from (7) without loss of generality. To continue the analysis, (7) is rewritten as:

$$i_{C,R4}(\theta) = \frac{1}{2} I_{OUT}(\theta)\left(v_{REF}(\theta) - 1\right) + I_{OUT}(\theta)\left(2 - v_{REF}(\theta)\right) . \tag{8}$$

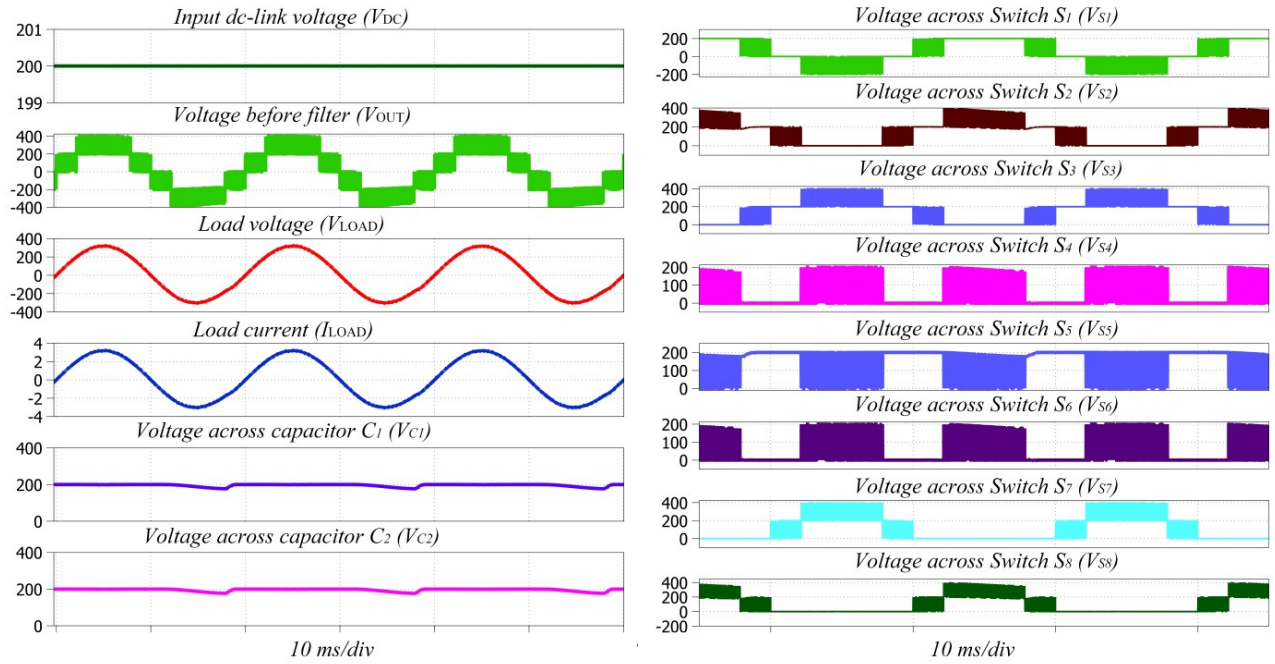


Fig. 4: Simulated waveforms of the proposed transformerless five-level boost inverter showing input/output voltage/current and voltage across capacitors and switches.

The load current (I_{OUT}) is:

$$I_{OUT} = I_{PK}\sin(\theta - \phi), \tag{9}$$

where I_{PK} is the peak output current and ϕ is the power factor angle. Assuming the voltage is constant in a grid-tied system, I_{PK} is a function of the output power (P_{OUT}), the grid voltage (V_{GRID}), and the power factor:

$$I_{PK} = \frac{\sqrt{2}\,P_{OUT}}{V_{GRID}\cos(\phi)}. \tag{10}$$

Thus, $I_{AVG,C,R4}$, is determined analytically by substituting (8), (9), and (10) into (6), which yields:

$$I_{AVG,C,R4} = \frac{I_{PK}\cdot m_a}{2(\pi - 2\theta_1)}\left((\pi - 2\theta_1)\cos(\phi) + \sin(2\theta_1 - \phi)\right). \tag{11}$$

Finally, the size of the flying capacitors is determined by substituting (5) and (11) into (4) and rearranging it to obtain:

$$C_i = \frac{I_{PK}\cdot m_a}{2\omega_c \Delta v_{C_i}}\left((\pi - 2\theta_1)\cos(\phi) + \sin(2\theta_1 - \phi)\right), \tag{12}$$

or

$$C_i = \frac{\sqrt{2}\,P_{OUT}\,m_a}{2\omega_c \Delta v_{C_i} V_{GRID}\cos(\phi)}\left((\pi - 2\theta_1)\cos(\phi) + \sin(2\theta_1 - \phi)\right). \tag{13}$$

From (13), it can be seen that the capacitors' size increases with larger power requirements, smaller fundamental frequencies, and increasing ripple voltage restrictions.

V. Simulation Results

The proposed topology was simulated using Matlab-Simulink and the PLECS toolbox in order to validate its performance. The waveforms are shown in Fig. 4. It can be seen that the inverter takes 200 V and is able to produce a five-level output voltage that can be filter to produce sinusoidal voltage and current waveforms. Furthermore, a small drop in the capacitors' voltage appears during *Region 4*.

Finally, the voltage stress for each of the switches is easily discernable. Several points should be considered. First, it can be seen that S_1 needs to block bidirectional voltage. Second, the voltage stress for each switch corresponds to the values

Fig. 5 Modular prototype inverter with two provisional capacitor banks.

TABLE IV. PARAMETERS AND COMPONENTS FOR SIMULATION AND EXPERIMENTAL PURPOSES

Parameter/Description	*Value*
Rated Power, P	1 kW
Input voltage, v_{in}	200 V_{DC}
Output voltage, v_{ac}	240 V_{RMS}
Modulation Index, m_a	0.8485
Switching frequency for SPWM, f_S	20 kHz
Line frequency	60 Hz
Load (Resistive)	~ 57 Ω
LC filter	0.37 mH, 2.4 µF
Flying Capacitors (C_1 & C_2)	(4) 100 µF Film (2) 820 µF Elect.
Power switches	Si MOSFET IPP60R125P6

given in Table III. Third, the switches do not change states continuously throughout the switching cycle, but rather remain turned on or off. This helps reduce the switching loss.

VI. EXPERIMENTAL RESULTS

A prototype developed to validate the operation principles of the inverter; it is shown in Fig. 5. The relevant parameters are given in Table IV. All nine power switches are implemented using 600 V Si MOSFETs. They are attached on the bottom side of the board to a common heatsink that is cooled with a small fan. The flying capacitors are implemented using a combination of film capacitors and electrolytic capacitors. The prototype was constructed to be modular so that the capacitor banks can be interchanged to evaluate the proposed topology in applications outside of grid-tied PV integration. The control signals were generated by a Texas Instruments Peripheral Explorer Kit that uses a TMS320F28335 digital signal processor (DSP).

Testing was performed at the rated power level (See Table IV and V). A resistive load bank was used in place of a grid tied connection to simplify the implementation. The experimental results are shown in Fig. 6 for the inverter

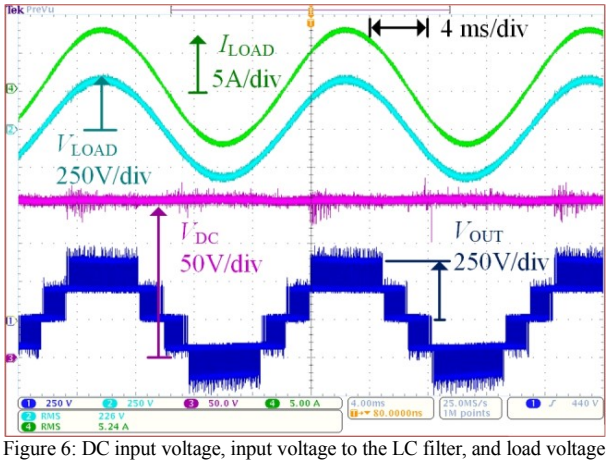


Figure 6: DC input voltage, input voltage to the LC filter, and load voltage and current measurements at 1,184 W.

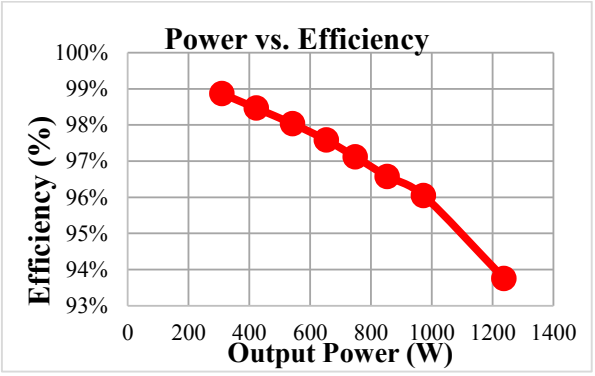


Figure 7: Plot of power vs. efficiency (V_{DC} = 200 V, V_{LOAD} = 240 V_{RMS}).

TABLE V. MEASUREMENTS FOR EFFICIENCY TESTING

V_{DC}	I_{DC}	P_{IN}	V_{OUT}	I_{OUT}	P_{OUT}	η
202.6	0.976	197.7	241.5	0.810	195.7	99.0%
202.6	1.552	314.4	240.5	1.292	310.8	98.9%
202.6	2.122	429.9	239.6	1.766	423.2	98.5%
204.1	2.712	553.5	240.5	2.256	542.6	98.0%
204.1	3.281	669.7	239.6	2.728	653.6	97.6%
205.4	3.756	771.5	240.3	3.118	749.2	97.1%
205.4	4.307	884.5	239.2	3.572	854.2	96.6%
207.6	4.879	1012.8	240.4	4.046	972.8	96.0%

operating at a load of nearly 1200 W. The figure shows DC input voltage (V_{DC}), the output voltage before (V_{OUT}) and after the filter (V_{LOAD}), and the load current (I_{LOAD}). It can be seen that the filtered voltage and current are clean sinusoidal waveforms. Additionally, the inverter's output shows five discrete levels with minimal change in the DC link voltage during region four. The results confirm that the inverter is able to operate at rated load and produce clean output waveforms.

Efficiency measurements were made from 300 W to 1200 W using a high precision power analyzer (p\n: Hioki PW3390) and two current clamps. The maximum efficiency was 99%; it occurred at 30 % of the load. At the rated power level of 1kW, the efficiency was 96 %. Beyond this point the efficiency begins to drop rapidly as some of the devices operate at the edge of their safe operating area. This was noticeable at 1200 W because the temperature on S_1 rose quickly. Table V includes the measurement values obtained using the power analyzer. They are plotted in Fig. 7.

VII. CONCLUSIONS

The following paper proposes a new topology for single-phase photovoltaic (PV) systems. It is a transformerless, 5-level boost inverter with common ground connection and two flying capacitors. The operating principles of the inverter are given for each of the five switching states. Next, the derivations were supplied to show how to size the flying capacitors for a given input voltage, output voltage, output power and capacitor ripple requirements. This was followed with basic simulation results. Finally, the paper concluded with experimental results at rated voltage and power. It was

demonstrated that the inverter can operate with very high efficiency (~99 %) at light loads while still achieving an efficiency of 96 % at 1 kW.

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