A High-Frequency Non-Isolated ZVS Synchronous Buck–Boost LED Driver with Fully-Integrated Dynamic Dead-Time Controlled Gate Drive

Qi Cheng and Hoi Lee

Department of Electrical and Computer Engineering, University of Texas at Dallas
Richardson, TX 75080, USA

***Abstract*—This paper presents a high-efficiency and high-frequency non-isolated ZVS synchronous buck–boost LED driver for automotive lighting applications. The synchronous gate driver IC with embedded high- and low-side ZVS detection is developed to generate dynamic dead-time with minimized detection delay. This enables high-frequency low-loss ZVS operation in the non-isolated synchronous converter topology over wide ranges of the input voltage and the output LED number. The buck–boost LED driver with eGaN FETs and the gate driver IC designed in a 0.5µm HV CMOS process can support up to 20 series-connected LEDs and achieve a peak power efficiency of 94.2% at 2.5-MHz switching frequency.**

I. Introduction

With the advantages of much higher luminous-efficacy and longer lifetime over traditional lighting technologies like incandescent lamps and compact fluorescent lamps, LED lamps have been widely used in automotive lighting applications. In this case, DC-DC based LED drivers are required to provide an average current passing through output multiple series-connected LEDs for having constant luminous intensity under both variations in the input voltage and the number of output LED [1]. In automotive systems, the battery input of the LED driver can change in a wide range from 5 V to 60 V resulting from cold cranking and load dump conditions [2], while the output voltage that is proportional to the number of series-connected LEDs can be either higher or lower than the input. This characteristic demands the LED driver have both capabilities to withstand wide input and output variations, and either buck or boost the input voltage.

An isolated Ćuk converter with advanced planar transformer technology was recently reported to achieve high power efficiency via ZVS operation in the MHz range [3]. However, the transformer size still occupies quite a significant portion of the total converter volume. In fact, the non-isolated buck-boost topology that adopts only one power inductor is considered as a better choice for high-frequency ZVS LED driver with smaller magnetic volume. However, unlike the Ćuk topology, the synchronous gate drivers which provide appropriate gate-drive signals for both high- and low-side power transistors are required. On the other hand, the required dead-time duration for ZVS operation will be changed according to different input/output conditions, and thus it should be controlled carefully to avoid extra power loss.

Therefore, this paper proposes a synchronous gate driver IC with embedded high- and low-side ZVS detection circuitry to provide dynamic dead-time for power FETs with nano-second-scale detection delays. The short-delay ZVS detection not only enables high-frequency operation for decreasing the required size of the inductor but also minimizes the body-diode conduction loss for better power efficiency over wide variations of input and output conditions.

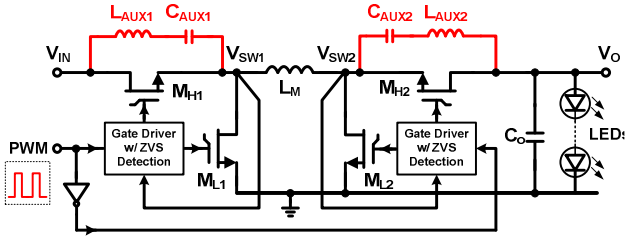

Fig. 1: Structure of the proposed non-isolated synchronous ZVS buck–boost LED driver.

In this work, the proposed LED driver is designed to provide an average output current of 350mA for LEDs with full-range ZVS operation over a wide input voltage range from 5V to 60V and output LED number from 1 to 20. This paper is organized as follows. Section II introduces the proposed non-isolated buck-boost LED driver and disadvantages of the fixed dead-time scheme with the necessity of the dynamic dead-time control. Section III discusses the design of the synchronous gate driver with the pulse-based level shifter and the high-speed embedded ZVS detection. Simulation verifications and performance comparisons among the proposed and state-of-the-art LED drivers with buck and boost capabilities are provided in Section IV. Finally, conclusions are given in Section V.

II. Proposed Non-Isolated Buck-Boost LED Driver with ZVS Operation

The structure of the non-isolated ZVS synchronous buck–boost LED driver is depicted in Fig. 1. There are two pairs of synchronous power switches (M_{H1}, M_{L1}) and (M_{H2}, M_{L2}), a main inductor L_M, and two pairs of small-value auxiliary inductors (L_{AUX1}, L_{AUX2}) and capacitors (C_{AUX1}, C_{AUX2}). Similar to [4], both auxiliary branches are used to generate transient currents to charge/discharge the parasitic capacitance at corresponding switch nodes (SW1 and SW2) during switching transitions to enable ZVS of all power switches when they are turned on. This removes the switching loss at both switching nodes, thereby improving the power efficiency of the converter especially under high input voltage condition.

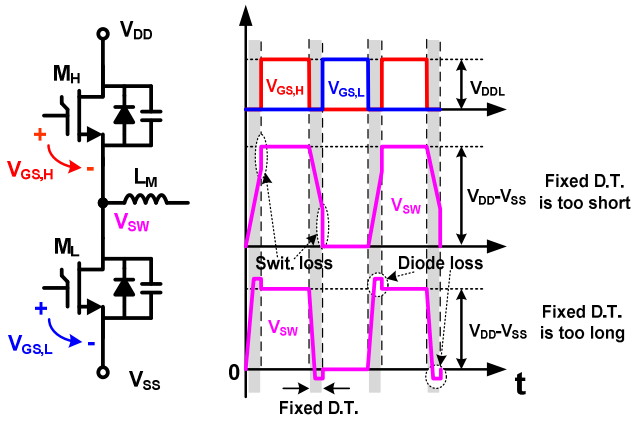

Fig. 2: Disadvantages of the fixed dead-time scheme.

Controlling the dead-time for turning-on the power switch is important for the ZVS operation, but challenging to realize. As shown in Fig. 2, if the dead-time is fixed and shorter than the actual required value for full ZVS operation, the switching loss would reduce the power efficiency. On the other hand, if the dead-time is too long, the switch node voltage would be higher (or lower) than its desired value, resulting in the extra body-diode conduction loss in the converter. In addition, the desired dead-time for ZVS operation will be changed when either the supply voltage or the number of output LED varies. The capability of generating dynamic dead-time is thus essential. Previous manual tuning of the dead-time [4], [5] would be impractical for the LED drivers that handle wide ranges of the input and output variations. Dynamic dead-time with automatic ZVS detection was reported via using an extra off-chip auxiliary winding with an estimated resonant period [6] – [8]. However, the auxiliary winding complicates the magnetic design and the resonant period is only an empirical value that varies with voltage in practical environment, resulting in inaccurate dead-time control for power switches. This ZVS detection would also need at least 10s-of-ns delay and thus 100s-of-ns dead-time that is too long for proper operation of the LED drivers in the MHz range.

III. Synchronous Gate Driver with High-Speed Embedded ZVS Detection

Fig. 3 shows the schematic of the proposed gate driver for a pair of synchronous power switches. The gate driver consists of a pulse-based level shifter to upshift low-voltage duty-ratio information to the high-voltage domain for controlling the turn-off of the high-side power switch M_H; high- and low-side ZVS detectors to generate dynamic dead-time for enabling ZVS operation during the turn-on of M_H and M_L, respectively, under different input/output conditions; and voltage buffers to provide sufficient transient currents for driving input capacitance of power switches. The level shifter adopts the principle of the previous dynamic level shifter [9] to significantly reduce its average current consumption via decreasing the turn-on time of the level shifting stage using a short-pulse generator.

Both embedded high- and low-side ZVS detectors rely on a diode for detecting the voltage difference between the drain and source terminals of the power switch. Since both structures are similar, without the loss of generality, only the high-side ZVS detector will be discussed here. As shown in Fig. 3, the high-side ZVS detector consists of a self-biased current source, a diode-connected pMOS, a diode D_H, and a falling-edge detector. Specifically, the diode D_H is realized by the body diode of an always-off transistor in this design for the ease of chip-level integration, although an off-chip Schottky diode can also be used for a smaller turn-on voltage. The transistor-level implementation of the current source is given in Fig. 4(a). If the drain-to-source voltage $V_{DS,MH}$ (= $V_{DD} - V_{SW}$) of M_H is larger than the value of (5 V – $V_{SG,MPH}$ – V_D) that is chosen as 2.5 V in this design and V_D is the turn-on voltage of D_H, D_H is turned off. On the other hand, if $V_{DS,MH}$ equals or is smaller than 2.5 V, diode D_H is turned on to result in a diode current i_{DH} and the instant voltage drop of V_H. This voltage drop is then detected by the falling-edge detector to

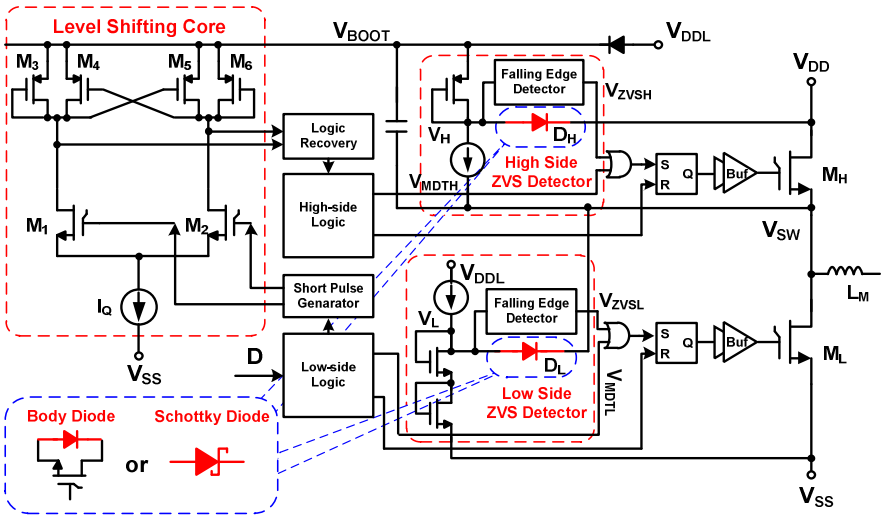

Fig. 3: Schematic of the proposed gate driver for synchronous power switches.

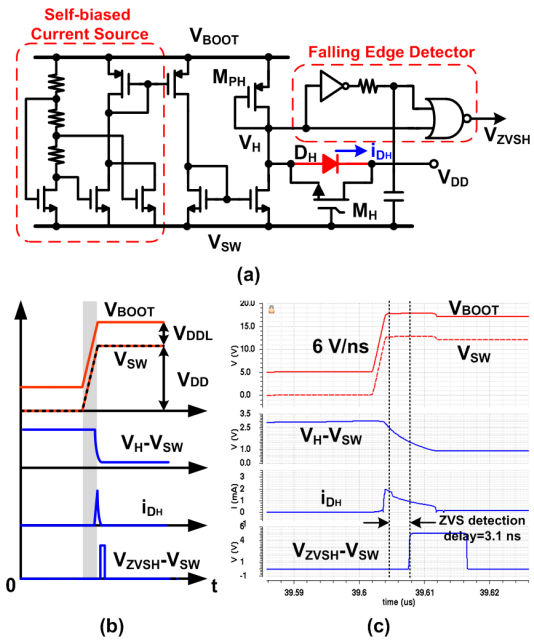

Fig. 4: (a) Schematic of the proposed HS ZVS detector, (b) its operation principle, and (c) simulated waveforms.

provide a pulse at V_{ZVSH} as shown in Fig. 4(b) for triggering the turn-on process of power switch M_H. Note that setting 2.5 V as the logic threshold is because the propagation delay from V_{ZVSH} to assert the gate voltage of M_H approximately equals the time for $V_{DS,MH}$ decreasing from 2.5 V to 0 in circuit simulations, and the logic threshold can be adjusted by varying the value of $V_{SG,MPH}$ using different bias currents.

Since each power switch has its own dedicated ZVS detector, the ZVS detection can be performed directly in the same common-mode voltage domain of the power switch without having extra delays in the voltage divider and level shifter. The ZVS detection delay can thus be minimized to only a few nanoseconds that reduce the required dead-time and enable the LED driver operating in the MHz range. Fig. 4(c) provides the simulation results of the high-side ZVS detector for turning on power switch M_H (in Fig. 3) when V_{SW} increases from 0 to 12 V with the slew rate of 6 V/ns. The worst-case ZVS detection delay is 3.2 ns (shown in Table I) under different process corner simulations and the static current consumption of the ZVS detector is only 20 µA.

TABLE I: ZVS DETECTION DELAY UNDER DIFFERENT CORNER MODELS

T= -40℃

Slope of V_{SW} (V/ns)	**50**			**5**		
Corner*	**TM**	**WP**	**WS**	**TM**	**WP**	**WS**
Delay @ HS(ns)	1.8	1.4	1.2	1.0	0.8	0.6
Delay @LS(ns)	0.9	0.6	1.7	0.4	0.3	0.7

T= 27℃

Slope of V_{SW} (V/ns)	**50**			**5**		
Corner*	**TM**	**WP**	**WS**	**TM**	**WP**	**WS**
Delay @ HS(ns)	1.4	1.6	1.2	1.8	1.0	1.4
Delay @LS(ns)	1.5	0.8	2.0	0.8	0.6	1.2

T= 120℃

Slope of V_{SW} (V/ns)	**50**			**5**		
Corner*	**TM**	**WP**	**WS**	**TM**	**WP**	**WS**
Delay @ HS(ns)	3.2	2.0	2.4	2.8	2.0	1.6
Delay @LS(ns)	2.2	1.6	2.6	1.3	0.9	1.9

*TM=Typical Mean; WP=Worst-case Power; WS=Worst-case Speed.

IV. PERFORMANCE VERIFICATION

To validate the ZVS synchronous buck–boost LED driver, the proposed gate driver was implemented in 0.5-µm 120-V CMOS technology and 4 power switches were realized by 100-V eGaNs FETs (EPC8010). In this design, the LED driver supports the input voltage from 5 to 60 V (nominal 12 V) and provides an average output current of 350 mA to a single string series-connected LEDs (Cree XLamp XB-D white LEDs) with the number from 1 to 20. To model the environment of hardware prototype testing, four pairs of stray inductors (0.2 nH each) are included at the drain and source terminals of each eGaN FET power switch in the circuit simulations.

Figs. 5 – 7 show the gate drive signals, switch node voltages (V_{SW1}, V_{SW2}) and output current of the proposed LED driver with the nominal 12-V input when driving 1, 4 and 20 LED(s). These figures illustrate both high-side and low-side ZVS operations are achieved at switch nodes S_{W1} and S_{W2}. For example, in Fig. 5, the low-side power switches (M_{L1} and M_{L2}) are turned on with the increase in $V_{GS,L1}$ and $V_{GS,L2}$ after voltages V_{SW1} and V_{SW2} decrease to 0, respectively. Figs 5 to 7 also justify that dynamic dead-times for high- and low-side power switches are generated by the proposed synchronous gate drivers under different numbers of output LEDs, and the dead-time is always smaller than 12.0 ns. Fig. 8 shows that the peak power efficiency of the proposed LED driver is about 94.2% at 2.5-MHz frequency under different input voltages of 12 V and 24 V and various numbers of output LEDs from 1 to 20. Table II provides the performance comparisons of the proposed LED driver with state-of-the-art counterparts [3] and [10] having similar input voltage ranges. This work has much smaller magnetic volume than [3] due to the use of non-isolated synchronous converter topology and high-frequency ZVS operation enabled by the proposed gate driver with embedded ZVS detection. Thanks to high-frequency operation, the proposed LED driver uses a much smaller output capacitor than [10], which would result in better dimming performance.

V. CONCLUSIONS

A non-isolated ZVS synchronous buck-boost LED driver with dynamic dead-time controlled gate drive is proposed and verified in this paper. The proposed gate driver enables the LED driver to operate at 2.5MHz frequency with the peak efficiency of 94.2% under 12-V input voltage condition. With ZVS operation of non-isolated buck-boost topology, the proposed LED driver has the smallest magnetic volume over its counterparts. The proposed LED driver is able to support a wide input voltage range of 5 to 60 V and output LED number of 1 to 20, which is suitable for automotive lighting applications.

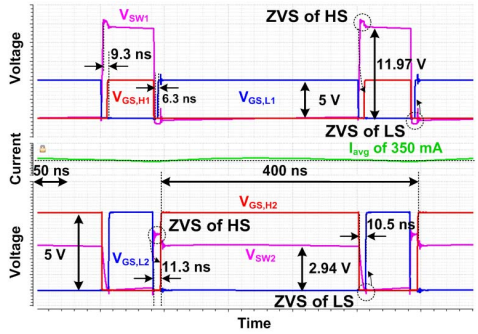

Fig. 5: Key waveforms of the proposed LED driver at V_{IN}=12V when driving 1 LED.

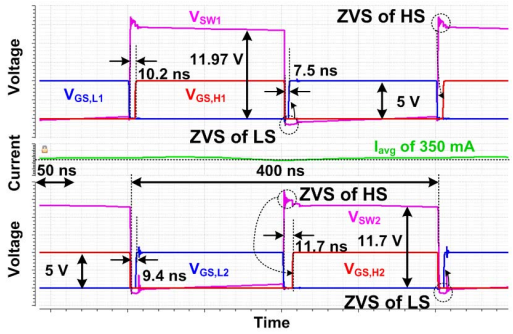

Fig. 6: Key waveforms of the proposed LED driver at V_{IN}=12V when driving 4 LEDs.

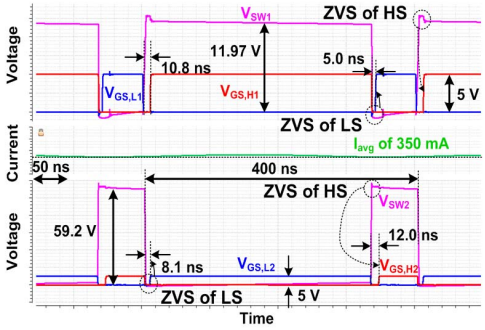

Fig. 7: Key waveforms of the proposed LED driver at V_{IN}=12V when driving 20 LEDs.

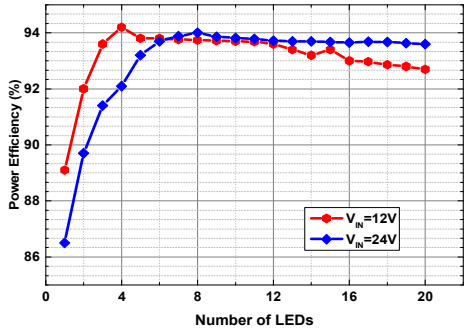

Fig. 8: Power efficiency of the LED driver under different values of V_{IN} and number of LEDs.

TABLE II: PERFORMANCE COMPARISONS OF DIFFERENT STATE-OF-THE-ART LED DRIVERS

	APEC 2017 [3]		LT 3791 [10]	**This work**
Converter Topology	Ćuk		Buck–Boost	**Buck–Boost**
Power Transistors	MOSFET	eGaN FET	MOSFET	**eGaN FET**
Gate Drivers	UCC27511-A	LM5114	On-Chip	**On-Chip Proposed ZVS Gate Driver**
Switching Frequency	1.8 – 2.4 MHz		0.3 MHz	**2.5 MHz**
Input Voltage	5–45 V (nominal: 12 V)		4.7–58 V (nominal: 24 V)	**5–60 V (nominal: 12 V)**
Output Voltage	3 – 50 V		0 – 52 V	**3 – 60 V**
Average LED Current	500 mA		2000 mA	**350 mA**
Inductor	0.68 µH		10 µH	**1 µH (L_M) and 0.5 µH×2 (L_{AUX1} and L_{AUX2})**
Magnetic Volume	2237 cm^3*		1585 cm^3*	**1208 cm^3**
Energy-Transfer Capacitors	4.5 µF×2		N. A.	**0.5 µF×2 (C_{AUX1} and C_{AUX2})**
Output Capacitor(s)	125 nF		4.7µF×4	**220 nF**
Max. Output Power	30 W		50 W	**20 W**
Peak Efficiency	92.9%	93.5%	98%	**94.2%**

* Extracted from magnetic core data in the literature and datasheet.

REFERENCES

[1] D. Park, Z. Liu, and H. Lee, "A 40 V 10 W 93%-efficiency current accuracy-enhanced dimmable LED driver with adaptive timing difference compensation for solid-state lighting applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1846–1860, Aug. 2014.

[2] Texas Instruments, "Load dump and cranking protection for automotive backlight LED power supply," Mar. 2015.

[3] A. Sepahvand, M. Doshi, V. Yousefzadeh, J. Patterson, K. Afridi, and D. Maksimovic, "High-frequency ZVS Ćuk converter for automotive LED driver applications using planar integrated magnetics," *in Proc. IEEE Applied Power Electronics Conference and Exposition*, Mar. 2017, pp. 2467 – 2474.

[4] J. Xue and H. Lee, "A 2-MHz 60-W zero-voltage-switching synchronous noninverting buck–boost converter with reduced component values," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 7, pp. 716–720, Jul. 2015.

[5] I. H. Oh, "A soft-switching synchronous buck converter for zero voltage switching (ZVS) in light and full load conditions," *in Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2008, pp. 1460–1464.

[6] P. Preller, "Voltage apparatus having a switching element receiving driving pulses having a duration and a starting time that are depended upon a load," U.S. Patent 6 229 716, May 8, 2001.

[7] C. Fu-Zen and D. Maksimovic, "Digital control for improved efficiency and reduced harmonic distortion over wide load range in boost PFC rectifiers," *IEEE Transactions on Power Electronics*, vol. 25, no. 10, pp. 2683 – 2692, Oct. 2010.

[8] Texas Instruments, "UCC28060 datasheet: Natural interleaving dual-phase transition-mode PFC controller," Nov. 2008.

[9] Z. Liu and H. Lee, "A 25W 97%-efficiency 3.5MHz integrated dimmable LED driver with lossless synchronous current control and floating nMOS sensing scheme," *in Proc. IEEE Applied Power Electronics Conference and Exposition*, Mar. 2014, pp. 1378 – 1383.

[10] Linear Technology, "LT 3791 Datasheet: 60 V 4-switch synchronous buck-boost LED driver controller," 2012, Available online: http://cds.linear.com/docs/en/datasheet/3791fc.pdf.