State of Health (SOH) Estimation of Multiple Switching Devices Using a Single Intelligent Gate Driver Module

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***Abstract*: This paper presents a new platform for intelligent gate-driver architecture that enables real-time health monitoring of power devices while performing features offered by a commercially available driver. The novelty of this new technique is the application of spread spectrum time domain reflectometry (SSTDR) embedded pulse width modulated (PWM) sequence across the gate and the source of a power MOSFET. A degraded MOSFET experiences an increase in both ON-state channel resistance and equivalent series resistance of gate-source capacitance, and the SSTDR sequence can characterize the level of aging in a live circuit based on these impedance variations. To validate our proposed method, the SSTDR incident signal was applied across the high side MOSFET of a synchronous buck converter, and corresponding reflections were recorded and analyzed. Extensive variation in impedances throughout the circuit using PWM switching scheme makes the degradation detection more challenging. However, a new algorithm has been introduced in this paper to solve the problem mentioned above. Included experimental results demonstrate that the developed method can perform online degradation monitoring of multiple devices from a single measurement point, which will eliminate the need of a separate state of health (SOH) monitoring module for detecting degradation in each device. Although the initial test results are obtained for power MOSFETs, the proposed technique is equally applicable to other power devices such as IGBTs and silicon carbide (SiC) MOSFETs.**

Keywords— ***Condition monitoring; degradation; power MOSFET; power cycling; SSTDR; intelligent gate driver; reliability.***

I. Introduction

Reliability and performance of power converters greatly depend on power semiconductor devices such as MOSFETs and IGBTs along with capacitors and gate drivers. Reliability of these critical components degrades with time due to mechanical and thermo-electrical stresses, therefore downgrading the performance of the overall power conversion systems [1]-[3]. It is a well-known fact that a shift in gate-source threshold voltage, gate leakage current and switching turn ON and turn OFF times are predominantly caused by chip related failures, which indicate the gate structure degradation [3],[4]. In contrast, increased ON-state channel resistance ($R_{DS(ON)}$), collector-emitter voltage in saturation ($V_{CE(SAT)}$), and thermal resistance are identified as the precursors of the package related degradation such as wire-bond lift offs, solder fatigues and so on [1], [3],[4]-[7].

In recent literatures, measuring the failure precursors of power devices [8]-[11] or analyzing the model of the degradation process or combining the both [12]-[16] are explored to monitor the condition of the power converters continuously. However, measuring the precursors requires the use of additional probes, complex hardware as well as digital controllers, which may not be cost-effective. In addition, measurable electrical quantities such as changes in $R_{DS(ON)}$ and $V_{CE(SAT)}$ are negligible compared to off-stage resistance and voltage, and they often need isolated sensors, and this can result in low-resolution measurement. Furthermore, direct measurements are extremely difficult in a live power converter when the switches are pulsed by PWM signals. In contrast, model and system identification based techniques require huge computational task along with accurate training data and circuit model. They also need to be tuned under different operating conditions; otherwise, it may result in false detection. Moreover, none of the above techniques is capable of detecting degradation levels in multiple devices from a single measurement.

To overcome these limitations, SSTDR based condition-monitoring methods of power devices have been proposed in [17],[18]. SSTDR's performance does not depend on the circuit's operating condition, and this unique feature makes SSTDR an excellent candidate for condition monitoring process [19],[20]. That being said, previous SSTDR based condition-monitoring methods required SSTDR test signals to be applied across the drain-source terminals of a power MOSFET or collector-emitter terminals of an IGBT, which could be unsuitable for high voltage circuits. To eliminate this shortcoming, a novel in-situ condition monitoring technique applying sine modulated pseudo noise sequence (SMPNS) embedded PWM signal across the gate-source terminal of a MOSFET in a single switch dc-dc converter has been proposed in [21]. SMPNS is the incident signal of spread spectrum time domain reflectometry (SSTDR), and it reflects from any impedance mismatches found in its propagation path [19], [20]. Moreover, having a voltage level of minimum 22 mV and center frequency of up to 48 MHz, SMPNS acts as a low-voltage high-frequency noise on top of the 15V (or 18V for SiC MOSFETs) PWM sequence, and thus, it does not impact the normal

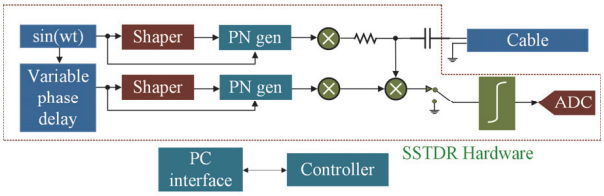


Fig. 1. Block diagram of the SSTDR fault diagnosis mechanism [20].

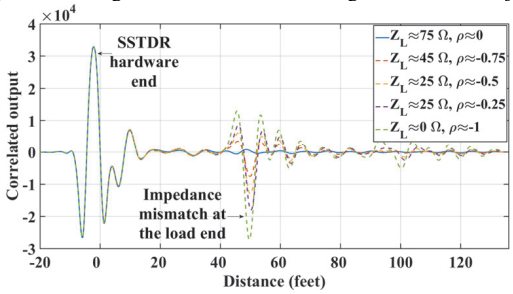


Fig. 2. Variation in correlated amplitude for the different values of reflection coefficients ($\rho \leq 0$) and load impedances ($Z_L \leq Z_0$) (for 50 feet long, 75 Ω co-axial cable) [21].

switching operation of the circuit [21]. Although this novel technique provides a new platform for the intelligent gate-drive architecture, this method [21] was able to detect degradation level only in a single switch from a single measurement unit.

In this paper, the SMPNS embedded PWM sequence was applied across the gate-source terminal of the high side MOSFET in a synchronous buck converter, and it was apparent that this arrangement could measure the degradation in both MOSFETs, one at a time, from a single measurement point. This will suffice the need for additional SOH module for detecting degradation in each device, and thus make it cost effective. Last but not the least, embedding SMPNS with PWM sequence provides the concept of integrating the state of health (SOH) feature in a single gate driver package that will lead to built-in-self-test (BIST) functionality in a power converter circuit.

II. Fundamentals of SSTDR Technology

SSTDR is a reflectometry based technique, which has been successfully used for fault detection in transmission lines [19],[20], and photovoltaic (PV) arrays [22]. In SSTDR, a high-frequency sine modulated pseudo noise sequence (SMPNS) (V_0^+, I_0^+) is continuously sent through the wire, and the delayed copies of the incident signal and the reflected signals (V_0^-, I_0^-) from any impedance mismatches are correlated. A block diagram of the SSTDR fault diagnosis mechanism is shown in Fig. 1. A lobe or peak is generated at a time delay in the auto - correlation plot that corresponds to the distance from the source terminal, when the incident signal experiences any impedance mismatches against the characteristic impedance in its propagation path. Since the incident signal and noise signal are asynchronous, the cross-correlation of them is nearly close to zero. SSTDR's immunity to noise and low-voltage characteristics make it an ideal method to monitor the impedance variation in various current paths in a live circuit. Reflection coefficient, ρ as defined in equation (1), is an important parameter in reflectometry sensor technologies. Z_L and Z_0 are the two variables in this function: Z_0 is the

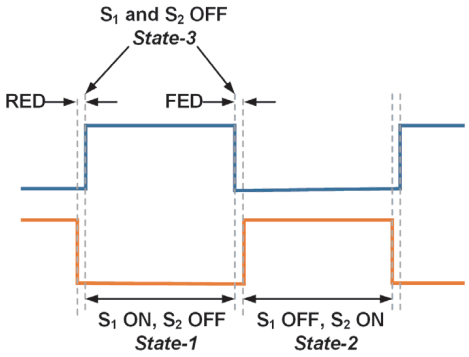


Fig. 3. Active high complementary (AHC) PWM switching scheme showing three different switching states (not drawn to scale). Here, RED= rising edge delay, FED= falling edge delay.

characteristic impedance of the transmission path and Z_L represents the impedance at the terminal. From this equation, if the terminal/load impedance is higher than the impedance of the transmission path/characteristic impedance, the reflection coefficient, ρ will be positive. In the same way, if the terminal impedance is lower than that of the transmission path, ρ is negative [19],[20].

$$\rho = \frac{V_0^-}{V_0^+} = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad (1)$$

In Fig. 2, different correlation plots have been generated for different values of reflection coefficient ($\rho \leq 0$) applying 48 MHz SSTDR signal through 50 feet long RG-6/U co-axial cable having 75 Ω (Z_0) characteristic impedance [21]. The first peak is due to the impedance mismatch between the SSTDR hardware and the co-axial cable, and the second peak is due to the impedance mismatch at the interface of the co-axial cable and the terminal load. According to (1) and Fig. 2, if $\rho \leq 0$, it is evident that any rise in load impedance (Z_L) will result in a decrease in magnitudes of the auto-correlated peak values (less negative). Since the equivalent series resistance of the gate-source capacitance (ESR_{GS}) and ON-state channel resistance ($R_{DS(ON)}$) is significantly smaller than that of the SSTDR test cable and the lumped network of the power converter, the auto-correlated peak amplitude will be negative, and the increased $R_{DS(ON)}$ and ESR_{GS} of an aged MOSFET will cause a reduction in the auto-correlated magnitudes.

III. Equivalent Circuits of The Synchronous Buck Converter and Corresponding SSTDR Signal Paths

SSTDR signal was continuously sent through the test points (TP1 and TP2, shown in Fig. 5), which were connected across the gate-source terminals of the high-side MOSFET (S_1) in a synchronous buck converter. Three operating states of the converter were considered provided that the switches were pulsed with active high complementary (AHC) PWM sequence (Fig. 3). The states are (i) S_1 is ON, S_2 is OFF (state-1), (ii) S_1 is OFF, S_2 is ON (state-2) and (iii) S_1 and S_2 both are OFF (dead time/ state-3). For simplicity, we ignored the turn OFF and turn ON switching transients of the MOSFET. A high-frequency model of a power MOSFET is shown in Fig. 4 highlighting the parasitic inductances and capacitances [23], [24]. SSTDR signal will propagate through all possible *ESR* paths of the parasitic capacitances (C_{GS}, C_{GD} and C_{DS}) along with the $R_{DS(ON)}$ of the

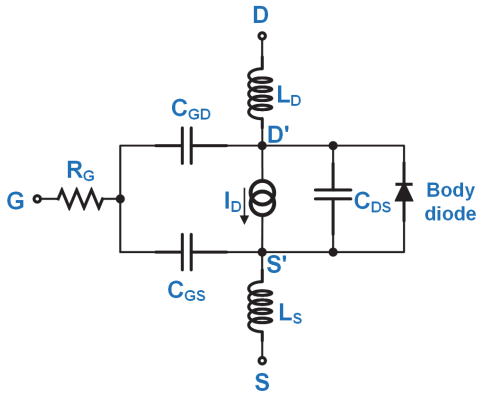


Fig. 4. High frequency equivalent circuit of a power MOSFET showing parasitic inductances and capacitances [23]- [24].

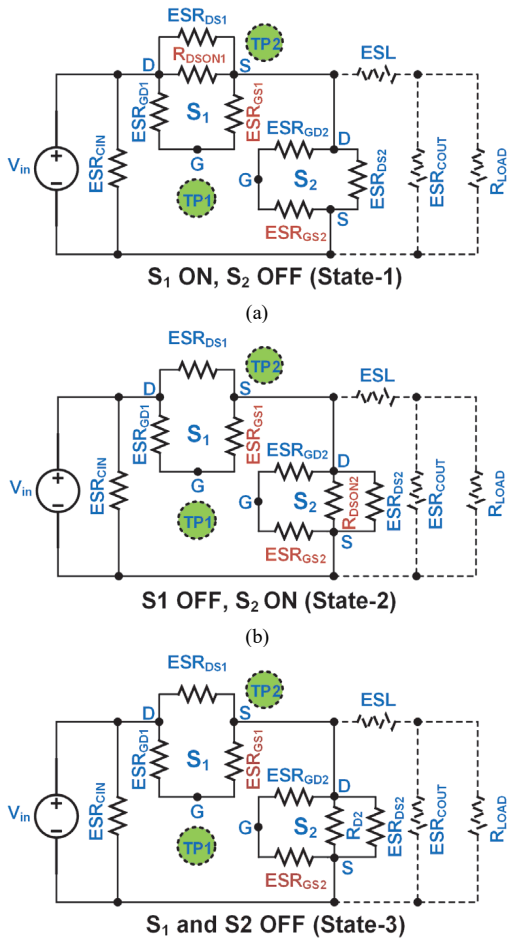


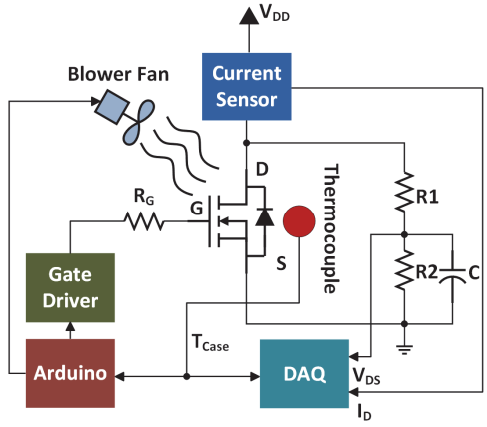
Fig. 5. Synchronous buck converter's equivalent impedance paths for SSTDR signals showing ESRs of parasitic capacitances and $R_{DS(ON)}$ of power MOSFET for a) state-1, b) state-2 and c) state-3. R_{D2}= forward diode resistance of Schottky diode.

MOSFETs. In addition, the parasitic inductances of the MOSFETs can be ignored as they have little or no impact on the SSTDR, and they do not change with the aging of the switching devices [1],[3]. However, the ESR of the gate to source capacitance (C_{GS}) and ON-state channel resistance, $R_{DS(ON)}$ significantly increase with the continuous aging of the MOSFET, and these rates are higher compared to the other parasitics in the MOSFET [1],[3]. Therefore, any variation in these components (marked with red, shown in Fig. 5) will have an influence on the equivalent impedance paths of each of the states as well as the auto-correlated amplitudes of the SSTDR signal. For instance, increased $R_{DS(ON)}$ of aged S_1 and increased $R_{DS(ON)}$ of aged S_2 will affect state-1 and state-2, respectively. It is obvious that the high-frequency SSTDR signal would not significantly propagate through the output capacitances and the load of the converter because the inductor would act as a low pass filter.

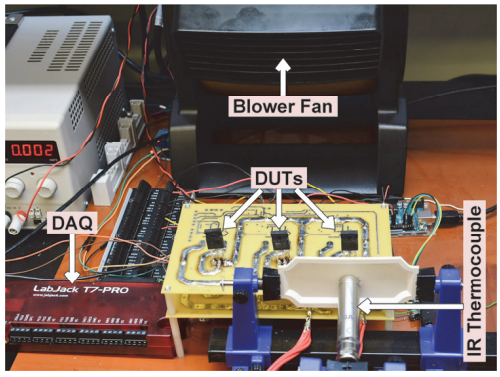
IV. EXPERIMENTAL SET-UP

A. Accelerated Aging Station

To perform the accelerated aging, active power cycling was conducted to apply electro-thermal stresses to a 600V-50A N-Channel MOSFET with a temperature gradient of 115° C. During the test, LabJack T-7 Pro data acquisition system (DAQ) was used to measure and record V_{DS}, I_D and case temperature (T_{Case}). The case temperature was measured using an IR thermocouple from OMEGA. Fig. 6 (a) and Fig. 6 (b)



(a)



(b)

Fig. 6. Experimental set-up for aging process, (a) Schematic (b) Photograph.

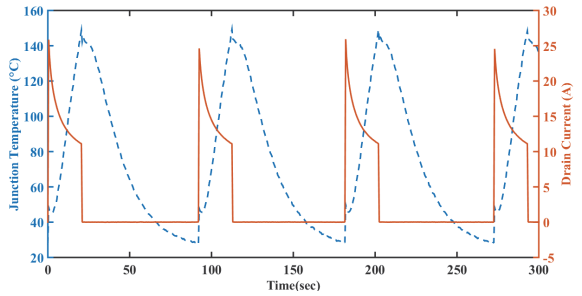


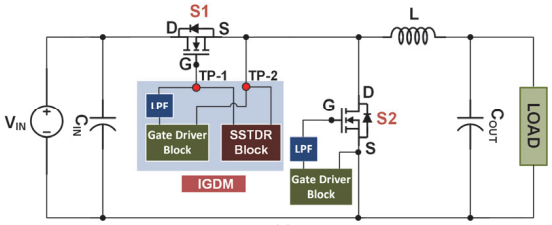
Fig. 7. Junction temperature and drain current swing of DUT during the power cycling test in the aging station.

show the schematic diagram and the photograph of the power MOSFET aging station respectively.

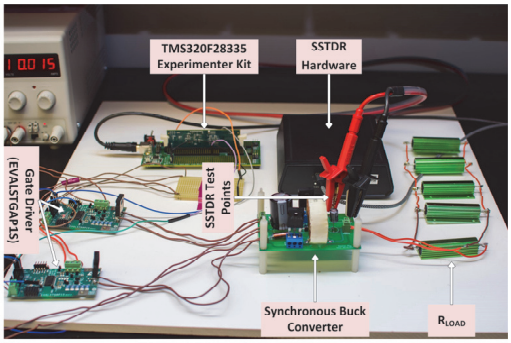
The aging process was continued for 8500 cycles, and it was found that the $R_{DS(ON)}$ increased from 49.5 mΩ to 75.77 mΩ. Both readings were taken at the junction temperature of 25° C. The increase in $R_{DS(ON)}$ is a clear indication of the aging of the MOSFET. A cooling fan was activated to reduce the temperature faster while the DUT was turned OFF. The swings in junction temperature and drain current of the device under test (DUT) during the power cycling test are shown in Fig. 7.

B. Degradation monitoring of Power MOSFETs in Synchronous Buck Converter

Fig. 8 shows the schematic diagram and the photograph of the test setup to perform the online degradation monitoring method. SSTDR hardware probes were connected across the gate-source of the high side MOSFET (S_1) inside the live synchronous buck converter. This hardware allows scanning the DUT connected to the hardware with frequencies up to 48 MHz. The experiment was performed for two operating conditions of the converter, e.g. 10 kHz and 20 kHz with 50% duty cycle. To



(a)



(b)

Fig. 8. Experimental set-up for condition monitoring, (a) Schematic (b) Photograph. Here, IGDM= Intelligent gate driver module.

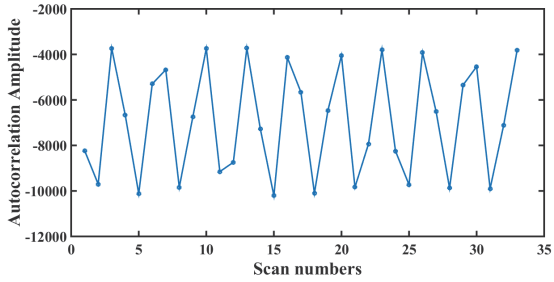


Fig. 9. A plot showing the pattern of negative peak amplitudes versus number of scans for baseline. Here, SSTDR frequency was 48 MHz, and operating frequency of the converter was 10 kHz with 50% duty ratio.

minimize shoot through, the active-high complementary (AHC) PWM sequences with a dead time of 0.1 μ second were generated by the TMS320F28335 experimenter kit from TI. Three groups of tests were conducted to verify the proposed SSTDR algorithm. The first group was considered as a baseline when all MOSFETs were new. Then we sequentially inserted the aged MOSFET at the two different positions of the converter; high side and low side (one MOSFET at a time) and considered them as group 1 and group 2, respectively. To make sure the reflected signal would not significantly propagate through the gate driver, a low pass filter (LPF) was inserted between the gate driver circuit and each of the MOSFET (as shown in Fig. 7 (a)).

V. EXPERIMENTAL RESULTS

SSTDR incident signals of two frequencies (10 and 20 kHz) were applied across the gate-source of the high side MOSFET (S_1), and ten (10) readings were obtained in each group. A 20 feet long two-conductor cable having VOP of 0.673 times the speed of light was used to connect the SSTDR hardware with the DUT to avoid the 'blind spot' error for SSTDR frequency up to 24 MHz. This error occurred when the connecting wire is small enough to make the reflected signal overlap with the incident signal (due to small time delay) [19]. More than 1100 sets/scans of auto-correlated amplitudes were generated for each reading, and only the negative peak values at the time shift corresponding to the distance from the SSTDR hardware to the high side MOSFET (S_1) were collected.

Interestingly, within each group, the autocorrelation peaks in each set had a certain level of deviation in a quasi-periodic manner because a continuous stream of SSTDR signals traveled through different equivalent impedance paths due to three different switching states. Fig. 9 shows the negative peak amplitudes for a few number of scans for baseline while SSTDR frequency was 48 MHz, and operating frequency of the converter was 10 kHz with 50% duty ratio. Here, the extreme values of high and low amplitudes roughly correspond the state-1 and state-2, respectively, since the higher amplitudes correspond to lower resistance and vice versa provided that $\rho \leq 0$. A periodic pattern in SSTDR peak amplitudes was expected due to the periodicity of these three different operating states. Unfortunately, SSTDR signal takes a certain amount of time to travel the distance through the wire and thus adds up a delay in each scan. Moreover, there are several sources of error in SSTDR hardware such as measurement errors, connection

errors, signal processing errors and so on. All these errors are responsible for the quasi-periodic pattern in the peak values. According to [21], a long PCB trace inside the gate driver circuit layout or increasing the frequency of the SMPNS can solve the 'blind spot' error, and synchronizing it with the PWM signal confidently differentiate the SSTDR data according to their respective switching states. However, these advantages can only be achieved if the SSTDR block is embedded in the gate driver circuit.

At this point, we are working on this embedded solution, and an intermediate algorithm was adopted to solve the problem depicted in the previous paragraph. The entire set of peak values for each reading was divided into 100 bins based on their amplitudes of descending order, and the frequency/ histogram of each reading of the corresponding bins was averaged for each group and plotted in Fig. 10 and Fig. 11 for PWM frequency of 10 and 20 kHz, respectively. To avoid confusion, we named this frequency distribution of the peak values as amplitude distribution. The left side and right side of the histograms

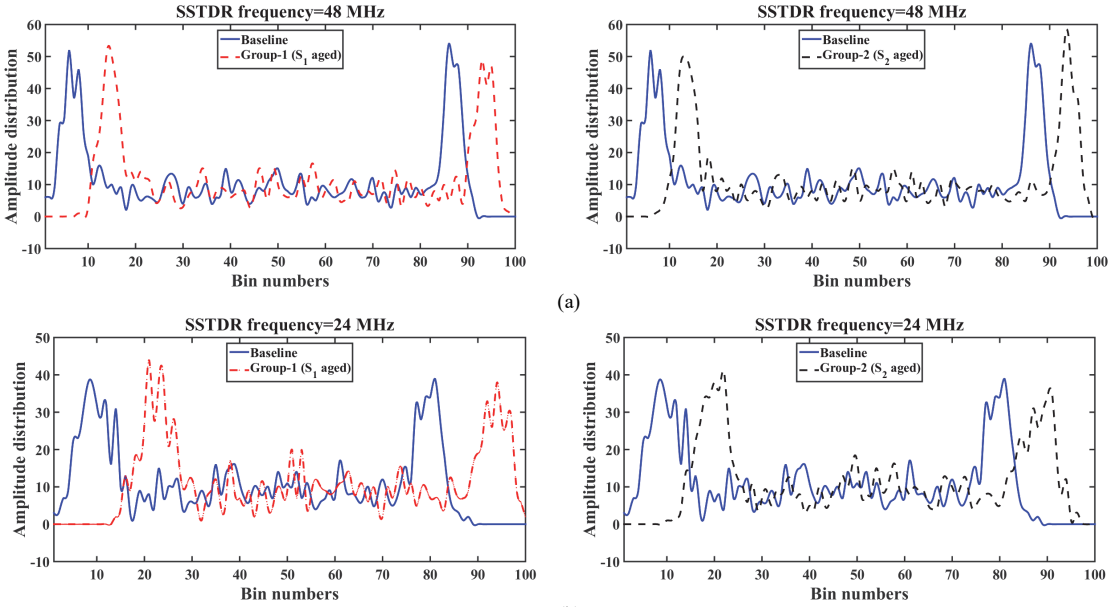


Fig. 10. Comparison of amplitude distributions for PWM frequency=10 kHz with 50% duty cycle; (a) SSTDR frequency=48 MHz, and (b) SSTDR frequency=24 MHz.

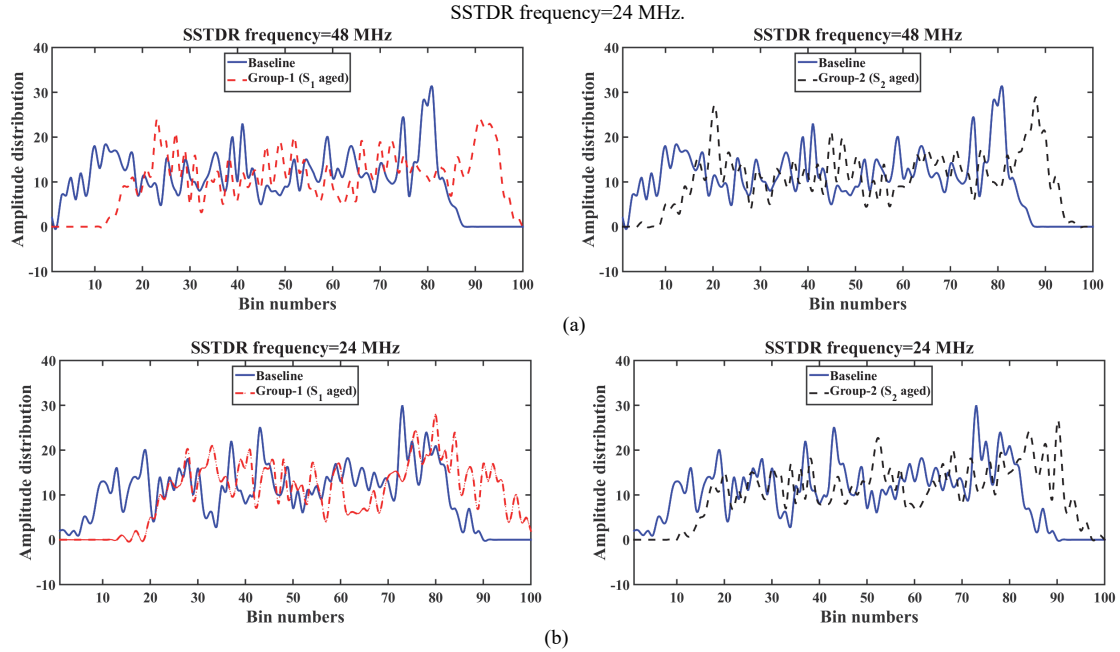


Fig. 11. Comparison of amplitude distributions for PWM frequency=20 kHz with 50% duty cycle; (a) SSTDR frequency=48 MHz, and (b) SSTDR frequency=24 MHz.

represent the auto-correlation amplitudes counts for state-1 and state-2, respectively, since they are arranged in descending order and OFF state resistance of the MOSFET is much higher than its ON-state resistance. For both switching frequencies of the converter, there was a rightward shift from the baseline for each group in the bin plots. This indicates that the correlation data for both the states have higher counts for the aged MOSFET compared to the baseline. This clearly indicates that the combined effect of *ESR* at the gate oxide interface and $R_{DS(ON)}$ has increased in an aged MOSFET.

Interestingly, the frequency counts for state-1 and state-2 for any group is lower for higher PWM frequency, and this is due to the fact that higher PWM frequency leads to less time in state-1 and state-2 provided that the dead time (state-3) remain the same. Moreover, a small variation exists in the amount of shift from baseline for group-1 and group-2 since the distances of the two MOSFETs from the SSTDR test points are different.

VI. CONCLUSIONS AND FUTURE WORKS

A novel in-situ condition monitoring technique applying sine modulated pseudo noise sequence (SMPNS) embedded PWM signals across the gate-source terminal of a MOSFET in a synchronous buck converter has been proposed in this paper. It was found that by analyzing the amplitude distribution of SSTDR peak values and their locations, it is possible to identify the individual degradation in both MOSFETs from a single measurement. Thus, a considerable amount of system-level savings can be achieved by eliminating the need for separate condition monitoring unit for high-side and low-side power switches. The authors are presently working on an embedded solution which will accommodate the SSTDR based SOH estimation unit inside a gate driver module. The fabrication details and experimental results will be summarized in future publications.

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