Harmonic Current Analysis of the Active Front End System in the Presence of Grid Voltage Disturbance

Bo Wen[1], and Paolo Mattavelli[2]
[1]The University of Manchester, UK
[2]University of Padova, Italy
bo.wen@manchester.ac.uk

***Abstract*— Prediction and control of harmonics injected into the grid from power electronics converters are very important for the power system. This paper analyzes the harmonic currents of an active front-end (AFE) system using its input admittance in the synchronous rotating frame in the presence of voltage harmonics at the point of common coupling (PCC). A voltage harmonic at the PCC of the AFE system with angular frequency of ω may induce current harmonics with angular frequency at not only ω, but also $2\omega_0$-ω. The line angular frequency is ω_0. To reduce the induced current harmonics, a grid sensitivity function defined by the grid and AFE impedances should be designed with low magnitude. The proposed analysis and method are validated using simulation and experiments.**

***Index Terms*— Active front-end, harmonics, impedance**

I. INTRODUCTION

Due to the progress of power semiconductor technologies and the need of the abilities of regeneration and flexible control, active front-end (AFE) rectifier system with higher switching frequencies [1], as shown in Fig. 1, is been used more and more in motor drive systems. A major concern about the AFE converter is its harmonic performance. This is because the prediction and regulation of harmonics injected into the grid from power electronics converter is a challenge facing power system. To limit the potential negative impact that an interconnected power electronics converter could have on the power quality (PQ) of the grid, IEEE Standard 519 [2] specifies maximum limits for the total demand distortion and for the harmonic amplitudes of the injected currents by the converter. Therefore, *L* and *LCL* filters are designed [3] for an AFE to meet the harmonic limits presented in the standards [2]. Harmonic current analysis of an AFE is usually based on the phase-leg voltages (v_{a1}, v_{b1}, v_{c1} in Fig. 1) harmonics, the filter impedance and an ideal grid condition [3]. From a power system point of view, current harmonics with different orders of an AFE converter are due to switching action and they are 'cross-coupled' because of pulse width modulation effect [4][5]. 'Harmonic admittance matrix' or 'frequency coupling matrix' is used to find the steady-state relation between the voltage and current harmonics of an AC-DC or DC-AC converter [5][6]. Other than switching harmonics, harmonic couplings are found due to controllers of the converter, such as current control loop, voltage control loop and phase-locked loop (PLL) [7][8][9]. Actually, along with the ever increasing switching frequency due to the application of advanced power devices, harmonics induced by the interaction between controllers of a converter, grid impedance, and grid disturbance [10] are getting worse, they could be inter-harmonics that cannot be analyzed using 'Harmonic admittance matrix' [5][6].

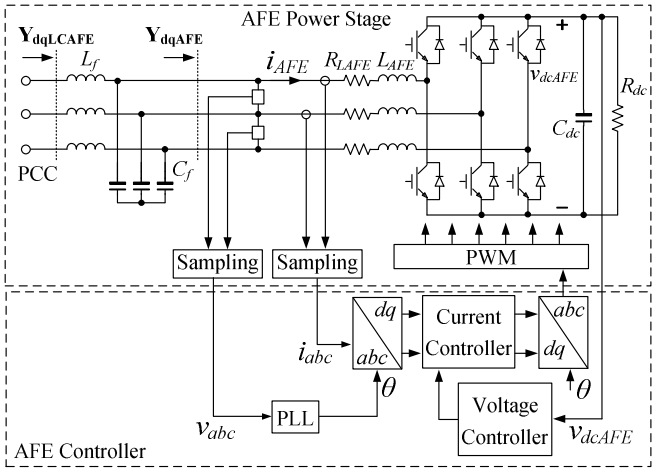


Fig. 1. An AFE system with an *LC* filter.

This paper analyzes the harmonic currents of an AFE system using the input admittance of the AFE in the synchronous rotating (*direct-quadrature*, *dq*) frame in the presence of voltage disturbances. This paper shows that the AFE is a system that similar to a salient pole machine. A disturbance with angular frequency ω at its terminal voltage induces currents not only at ω but also ($2\omega_0$-ω) with ω_0 the line angular frequency [11]. This interesting phenomenon is discussed in other papers using sequence domain impedances with different definitions [7]–[9][12], however, this paper shows that this phenomenon is actually a result of *dq* admittance asymmetrical [12][13]. Induced current harmonics can be calculated using the magnitude and frequency of the voltage disturbance and the *dq* input admittance of the AFE. To reduce the induced current harmonics, a grid sensitivity function based on the grid and AFE impedances is proposed.

By reducing the magnitude of the sensitivity function, the harmonic currents can be suppressed. An experimental system with a voltage source inverter (VSI) emulating the grid feeds to an AFE is used to validate the proposed method.

The paper is organized as follows: In section II, the *dq* impedance model of the AFE converter is discussed to unveil the root of coupled harmonic. Section III defines the grid sensitivity function for harmonic current calculation and suppression. Experimental results that validate the proposed concepts are shown in section IV. Section V is the conclusions.

II. Root of the Coupled Harmonic — a Perspective of *DQ* Impedance

In the *dq* frame, the current response to a voltage harmonic is calculated using the relationship as it is illustrated in Fig. 2. In a three-phase balanced power system, voltage harmonic with an angular frequency of ω is a rotating vector in the stationary ($\alpha\beta$) frame, as shown in (a), and its trajectory is a circle. After being transferred to the *dq* frame rotating at ω_0, ω_0 is the fundamental angular frequency, the voltage harmonic is still a rotating vector with angular frequency ω-ω_0. Its trajectory is still a circle, which means the *q*-axis voltage signal has the same magnitude and exact $\pi/2$ phase leg comparing to the *d*-axis voltage signal, as shown in Fig. 2. In *dq* frame, the admittance of the three-phase AFE converter is a multi-input and multi-output (MIMO) transfer function matrix. If the admittance matrix of the AFE system has a property that $Y_{dd}=Y_{qq}$ and $Y_{dq}=-Y_{qd}$, the corresponding current vector also has a circular trajectory with an angular frequency of ω-ω_0 as shown in Fig. 2 (a). If the admittance matrix is treated as a complex filter, in the communication theory, such property is named as a *balanced* structure [14]. In order to avoid confusion, such property is defined as a *symmetrical* admittance in this paper. If the admittance matrix is *dq* asymmetrical, $Y_{dd}\neq Y_{qq}$ or $Y_{dq}\neq -Y_{qd}$, the resultant current vector will have an elliptical trajectory that can be synthesized using two circles, see Fig. 2 (b). The current vector can be then broken down into two vectors with opposite rotating angular frequency, one is ω-ω_0 another is $-(\omega-\omega_0)$. When transferred back to the $\alpha\beta$ frame, they become harmonics with angular frequency ω and $2\omega_0-\omega$.

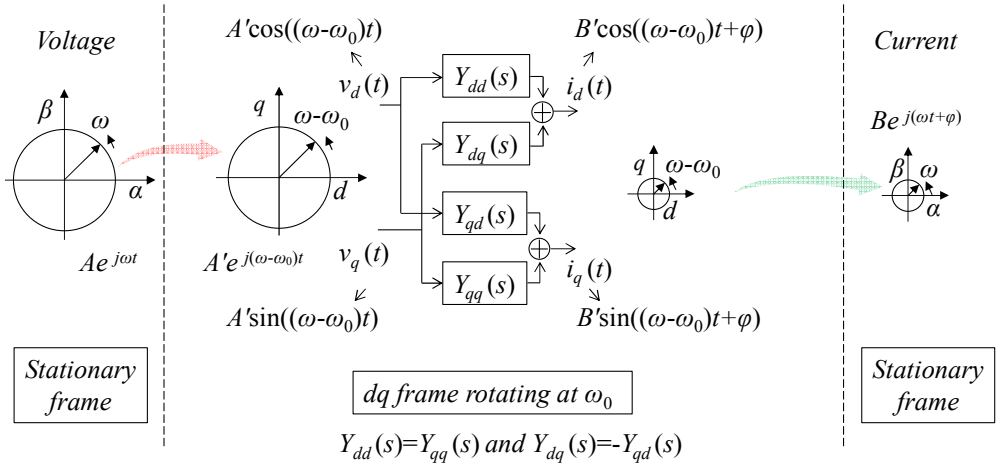


Fig. 2. The current response of *dq* admittances to a voltage harmonic: (a) symmetrical *dq* admittances; (b) asymmetrical *dq* admittances.

The input admittance matrix of an AFE converter in the *dq* frame is denoted as $\mathbf{Y_{dqAFE}}$. Modeling of the $\mathbf{Y_{dqAFE}}$ is well discussed in [15]–[17]. Here, the results in [15] are used for analysis:

$$\mathbf{Y}_{\mathbf{dqAFE}}=\begin{pmatrix}\mathbf{I}+\mathbf{G}_{\mathbf{id}}\left(\mathbf{I}+\mathbf{G}_{\mathbf{del}}\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{cv}}\mathbf{K}\mathbf{G}_{\mathbf{vd}}\right)^{-1}\mathbf{G}_{\mathbf{del}}\cdot\\ \left(-\mathbf{G}_{\mathbf{dei}}+\mathbf{G}_{\mathbf{ci}}\right)\mathbf{K}\end{pmatrix}^{-1}\cdot\left[\mathbf{Z}_{\mathbf{in}}^{-1}+\mathbf{G}_{\mathbf{id}}\left(\mathbf{I}+\mathbf{G}_{\mathbf{del}}\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{cv}}\mathbf{K}\mathbf{G}_{\mathbf{vd}}\right)^{-1}\mathbf{G}_{\mathbf{del}}\cdot\left[\left(\mathbf{G}_{\mathbf{dei}}-\mathbf{G}_{\mathbf{ci}}\right)\mathbf{G}_{\mathbf{PLL}}^{\mathbf{i}}\mathbf{K}-\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{cv}}\mathbf{K}\mathbf{G}_{\mathbf{ve}}+\mathbf{G}_{\mathbf{PLL}}^{\mathbf{d}}\mathbf{K}\right]\right] \quad (1)$$

In (1), the converter dynamics are modeled by MIMO transfer function matrices. Specifically, $\mathbf{G_{vd}}$ corresponds to the transfer function from duty cycle to output DC voltage; $\mathbf{G_{ve}}$ is the transfer function of input AC voltage to output DC voltage; $\mathbf{G_{id}}$ is the transfer function from duty cycle to the boost inductor current; $\mathbf{Z_{in}}$ is the open-loop input impedance. To capture the PLL dynamics two additional transfer functions are introduced in the model, $\mathbf{G^d_{PLL}}$ and $\mathbf{G^i_{PLL}}$ [16][17]. The feedback controller transfer function $\mathbf{G_{ci}}$ and $\mathbf{G_{cv}}$, the decoupling transfer function $\mathbf{G_{dei}}$, the signal conditioning filter K, and the delay transfer function $\mathbf{G_{del}}$ – capturing the time delay T_{del} introduced by sampling and pulse width modulation.

Most of the matrices in (1) are asymmetrical, take $\mathbf{Z_{in}}$ as an example:

$$\mathbf{Z}_{\mathbf{in}}=\begin{bmatrix}Z_{indd} & Z_{indq}\\ Z_{inqd} & Z_{inqq}\end{bmatrix}=\begin{bmatrix}Z_{dc}\left(D^s_{dAFE}\right)^2+Z_{LAFE} & Z_{dc}D^s_{dAFE}D^s_{qAFE}-\omega_0 L_{AFE}\\ Z_{dc}D^s_{dAFE}D^s_{qAFE}+\omega_0 L_{AFE} & Z_{dc}\left(D^s_{qAFE}\right)^2+Z_{LAFE}\end{bmatrix} \quad (2)$$

$$Z_{dc}=\frac{R_{dc}}{R_{dc}C_{dc}s+1} \quad (3)$$

$$Z_{LAFE}=L_{AFE}s+R_{LAFE} \quad (4)$$

Eq. (2) is the expression for $\mathbf{Z_{in}}$. It is the function of the converter duty cycles, D^s_{dAFE} and D^s_{qAFE}. Usually, D^s_{dAFE} is much bigger than D^s_{qAFE} for unity power factor condition. Then $\mathbf{Z_{in}}$ is asymmetrical at low frequency. When the frequency is increased high enough, the influence of D^s_{dAFE} and D^s_{qAFE} can be ignored, $\mathbf{Z_{in}}$ becomes symmetrical, see Fig. 3. Parameters of the AFE system is listed in Table I of the Appendix.

In fact, matrices $\mathbf{G_{vd}}$, $\mathbf{G_{ve}}$, $\mathbf{G_{id}}$, $\mathbf{G^d_{PLL}}$, $\mathbf{G^i_{PLL}}$, and $\mathbf{G_{cv}}$ are all asymmetrical. Together with the input *LC* filter, the closed-loop AFE admittance $\mathbf{Y_{dqLCAFE}}$ is asymmetrical, as shown in Fig. 4. Actually, if the parameters of the current controllers are designed with high enough value, $\mathbf{Y_{dqLCAFE}}$ could be symmetrical since $\mathbf{G_{ci}}$ is symmetrical. However, due to the DC voltage controller and the PLL, in the low-frequency range that is below the bandwidth of the DC voltage controller and the bandwidth of the PLL, $\mathbf{Y_{dqLCAFE}}$ is always asymmetrical. Eq. (5) shows the expression of $\mathbf{G_{ci}}$. Eq. (6)–(9) show the expression of $\mathbf{G^d_{PLL}}$ and $\mathbf{G^i_{PLL}}$. Eq. (10) shows the expression of $\mathbf{G_{cv}}$.

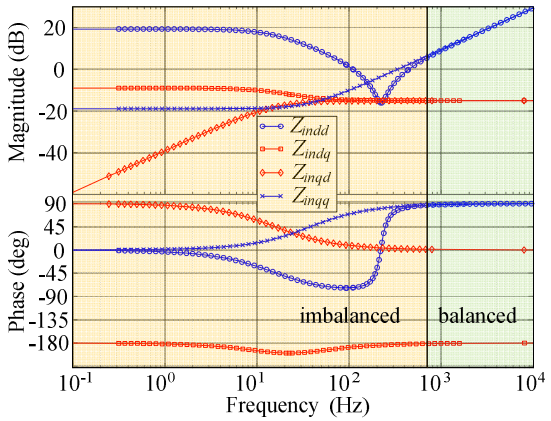


Fig. 3. The Bode plot of matrix $\mathbf{Z_{in}}$.

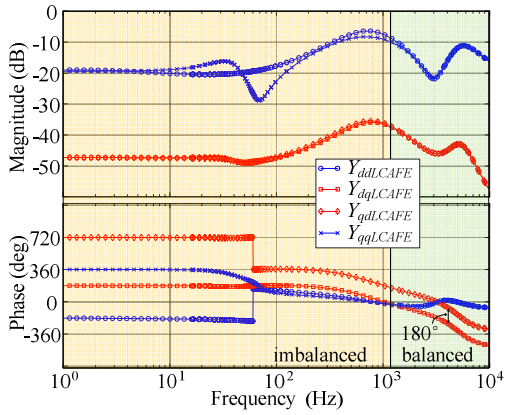


Fig. 4. The Bode plot of matrix $\mathbf{Y_{dqLCAFE}}$.

$$\mathbf{G}_{\mathbf{ci}}=\begin{bmatrix}k_{piAFE}+\dfrac{k_{iiAFE}}{s} & 0\\ 0 & k_{piAFE}+\dfrac{k_{iiAFE}}{s}\end{bmatrix} \quad (5)$$

$$\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}=\begin{bmatrix}0 & -D^s_{qAFE}G_{PLL}\\ 0 & D^s_{dAFE}G_{PLL}\end{bmatrix} \quad (6)$$

$$\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}=\begin{bmatrix}0 & -I^s_q G_{PLL}\\ 0 & I^s_d G_{PLL}\end{bmatrix} \quad (7)$$

$$G_{PLL}=\frac{tf_{PLL}}{s+V^s_d tf_{PLL}} \quad (8)$$

$$tf_{PLL}=k_{pllAFE}+k_{ipllAFE}/s \quad (9)$$

$$\mathbf{G}_{\mathbf{cv}}=\begin{bmatrix}k_{pvAFE}+\dfrac{k_{ivAFE}}{s} & 0\\ 0 & 0\end{bmatrix} \quad (10)$$

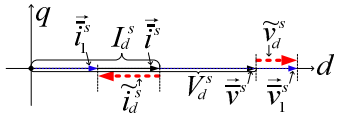


Fig. 5. Vector diagram illustration of Z_{dd}.

Fig. 5 shows the vector diagram of the AFE system. $\vec{\tilde{v}}^s$ is the PCC (point of common coupling) voltage vector that is aligned with *d* axis. $\vec{\tilde{i}}^s$ is the current vector of that AFE, it is synchronized with $\vec{\tilde{v}}^s$. When a voltage disturbance happens in *d* axis, the voltage vector $\vec{\tilde{v}}^s$ becomes $\vec{\tilde{v}}_1^s$. Because of the DC voltage control, the output and input power should keep constant, then the magnitude of the current vector will be decreased and it becomes $\vec{\tilde{i}}_1^s$, from a small-signal point of view, the Z_{dd} is a negative incremental resistor as shown in Eq. (13).

$$\left(\vec{\tilde{v}}^s+\Delta\vec{\tilde{v}}^s\right)\cdot\left(\vec{\tilde{i}}^s+\Delta\vec{\tilde{i}}^s\right)=\left(V_d^s+\tilde{v}_d^s\right)\cdot\left(I_d^s+\tilde{i}_d^s\right)=V_d^s\cdot I_d^s \tag{11}$$

$$V_d^s\cdot I_d^s=\left(V_d^s+\tilde{v}_d^s\right)\cdot\left(I_d^s+\tilde{i}_d^s\right)\approx V_d^s\cdot I_d^s+V_d^s\tilde{i}_d^s+\tilde{v}_d^s I_d^s \tag{12}$$

$$Z_{dd}\big|_{j\omega=0}=\frac{\tilde{v}_d^s}{\tilde{i}_d^s}=-\frac{V_d^s}{I_d^s} \tag{13}$$

Actually, Z_{dd} of the AFE system can be approximated as a negative resistor within the control bandwidth of the DC voltage.

For Z_{qq}, it behaves as a positive incremental resistor as shown in Fig. 6:

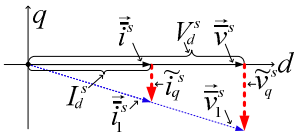


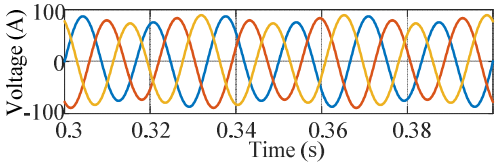
Fig. 6. Vector diagram illustration of Z_{qq}.

Z_{qq} can be calculated as:

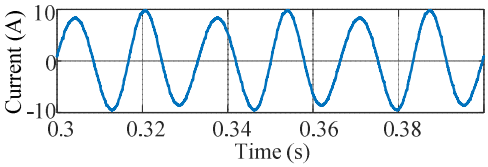
$$Z_{qq}\big|_{j\omega=0}=\frac{\tilde{v}_q^s}{\tilde{i}_q^s}=\frac{V_d^s}{I_d^s} \tag{14}$$

Actually, Z_{qq} of the AFE system can be approximated as a positive incremental resistor within the bandwidth of its PLL.

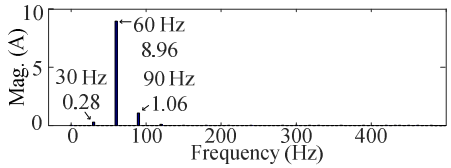
From the aforementioned analysis, within the control bandwidth of the DC voltage and the PLL, $\mathbf{Y_{dqLCAFE}}$ is always asymmetrical.



(a)

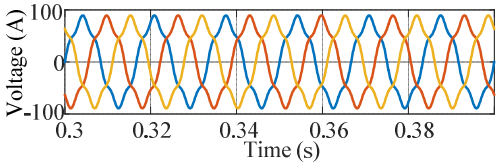


(b)

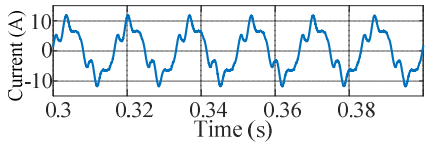


(c)

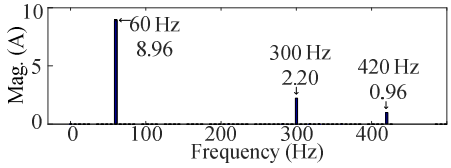
Fig. 7. Case 1, (a) v_{PCC} with 30 Hz harmonic, (b) i_{ga}, (c) spectrum of i_{ga}.



(a)

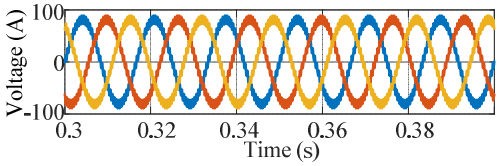


(b)

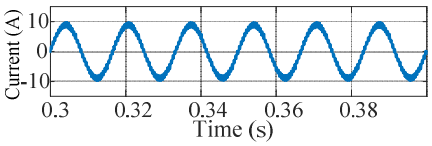


(c)

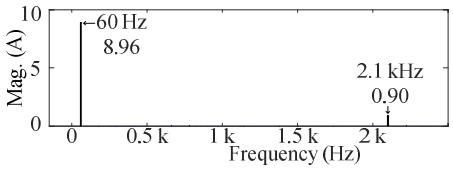
Fig. 8. Case 2, (a) v_{PCC} with 300 Hz harmonic, (b) i_{ga}, (c) spectrum of i_{ga}.



(a)



(b)



(c)

Fig. 9. Case 3, (a) v_{PCC} with 2.1 kHz harmonic, (b) i_{ga}, (c) spectrum of i_{ga}.

Switching model of the system shown in Fig. 1 was constructed in the Matlab/Simulink environment to verify the aforementioned analysis. Parameters of the simulation can be

found in the Appendix. The simulation results are shown in Fig. 7, Fig. 8, and Fig. 9. In Fig. 7 (a), a symmetrical voltage harmonic with a frequency of 30 Hz (voltage harmonic with an angular frequency of ω in Fig. 2) was added to the PCC voltage v_{PCC}, see Fig. 1. The phase a PCC current i_{ga}, see Fig. 1, has not only a 30 Hz harmonic (current harmonic with an angular frequency of ω in Fig. 2) but also a 90 Hz harmonic (current harmonic with an angular frequency of $2\omega_0$-ω in Fig. 2), see Fig. 7 (b) and (c). Fig. 8 (a), (b), and (c) give the results of having 300 Hz harmonic voltage and Fig. 9 (a), (b), and (c) show the results of adding 2.1 kHz voltage harmonic. They verify the aforementioned analysis.

III. The Grid Sensitivity Function

The grid voltage has background harmonics, especially when the grid impedance is significant. To reduce the induced current harmonics from an AFE, one can design the input admittance of the AFE to be symmetrical. However, as mentioned above, due to the DC voltage control and the PLL, below a certain frequency (bandwidth of the DC voltage controller and the PLL), the impedance matrix of the AFE will always be asymmetrical. For some applications, fast DC voltage controller and PLL are desired. It is neither possible nor useful to design a symmetrical impedance for the AFE in the low frequency.

Another way to reduce the current harmonics of the AFE system is to reduce the sensitivity of the AFE to the disturbance from the grid. The grid sensitivity function, $\mathbf{G_{se}}$, of the system can be defined as:

$$\vec{i}_L = \mathbf{G_{se}} \cdot \vec{v}_s = \left(\mathbf{Z_s} + \mathbf{Z_L}\right)^{-1} \cdot \vec{v}_s \qquad (15)$$

$\mathbf{Z_s}$ is the output impedance of the source (grid), $\mathbf{Z_L}$ is the input impedance of the load, both are in the *dq* frame, see Fig. 10. Actually, reducing the magnitude of $\mathbf{G_{se}}$ is to reduce the series resonance between the grid and the load in the *dq* frame.

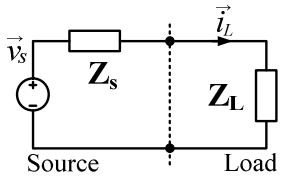


Fig. 10. Impedance representation of a source feeding to a load.

The sensitivity function is the admittance seen by the voltage source $\vec{v}_s$ and thus it shows the amplification of current harmonics in presence of voltage harmonics.

To validate this method, an experimental system consists of a VSI and an AFE shown in Fig. 11. The VSI is consisted of a two-level voltage source inverter and an *LC* filter, the parameters of the VSI and filter are listed in the Appendix. In this system, the voltage disturbance is generated by the dead time (T_{dt} = 2 μs) of the VSI and AFE. The dead time generates 5th, 7th, 11th, and 13th … harmonics to the system. When the DC voltage feedback control is designed too fast, $\mathbf{G_{se}}$ of the system has a peak nearly 10 dB at 360 Hz in the *dq* frame, see the solid red curve in Fig. 12. This peak amplifies the current harmonics at the 5th and 7th in the *abc* frame caused by the dead time voltage disturbances, the time domain experimental results are shown in Fig. 13.

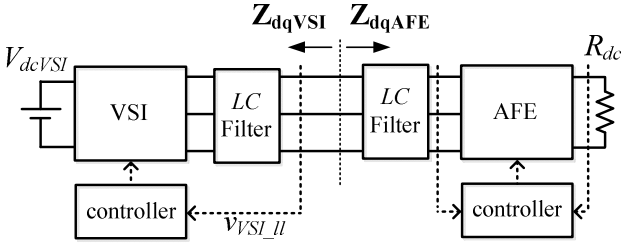


Fig. 11. Experimental system of a VSI feeding the AFE.

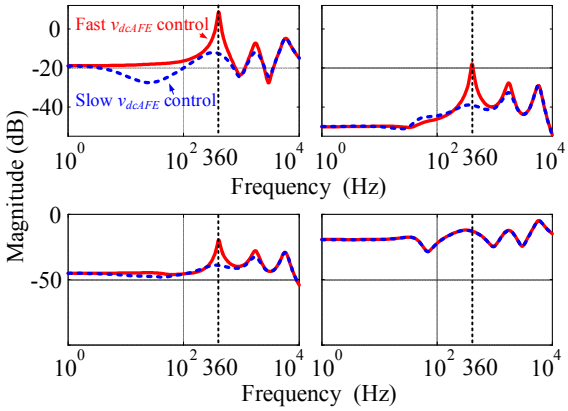


Fig. 12. $\mathbf{G_{se}}$ of the experimental system.

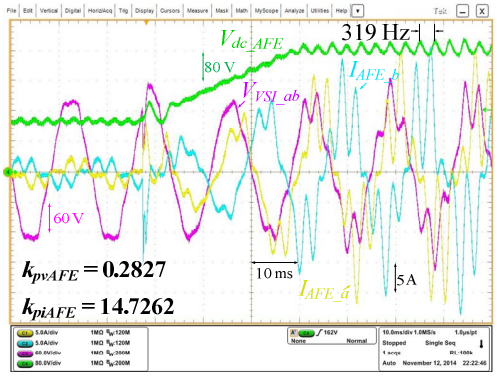


Fig. 13. Test results with fast DC voltage control of the AFE.

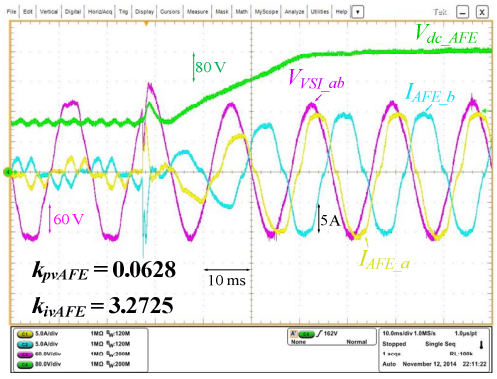


Fig. 14. Test results with slow DC voltage control of the AFE.

The grid sensitivity function $\mathbf{G_{se}}$ can be reduced by designing a slow DC voltage controller for the AFE (with smaller values of k_{pvAFE} = 0.0628 and k_{ivAFE} = 3.2725), as shown by the dashed blue curve in Fig. 12, then the current harmonics of the system can be reduced significantly as shown in Fig. 14.

IV. CONCLUSIONS

Harmonic currents performance of an AFE system is analyzed in this paper using the input admittance of the AFE in the *dq* frame. The results show that the AFE system is a *dq* asymmetrical system at a low frequency similar to a salient pole machine. When a disturbance with angular frequency ω is applied to its terminal voltage, its currents have not only a harmonic at ω but also $(2\omega_0-\omega)$ with ω_0 the line angular frequency. The induced current harmonics can be reduced by shaping the magnitude of the grid sensitivity function defined by the grid and AFE impedances in the *dq* frame significantly lower than 0 dB. The proposed analysis and method are validated using simulation and experiments. They are very useful for integrating AFE systems to a more power electronics power system where the grid impedance and voltage disturbances are high due to switching actions.

APPENDIX

TABLE I. PARAMETERS OF THE AFE AND VSI SYSTEM

Symbol	Description	Value
V_{ll}	Grid line-line peak voltage	$57.5\sqrt{6}$ V
f_{line}	Grid (line) voltage frequency	60 Hz
ω	Grid voltage angular frequency	$2\pi f_{line}$
L_{VSI}	Filter inductance of the VSI	0.97 mH
R_{LVSI}	Equivalent series resistance of L_{VSI}	80 mΩ
C_{VSI}	Filter capacitance of the VSI	30 μF
R_{CVSI}	Series damping resistance of C_{VSI}	200 mΩ
V_{dcVSI}	Inverter DC voltage	270 V
f_{sw}	Switching frequency of VSI and AFE	20 kHz
$V_{drefVSI}$	*d* channel voltage reference of VSI	99.6 V
$V_{qrefVSI}$	*q* channel voltage reference of VSI	0 V
k_{iiVSI}	Integrator gain of current controller	0
k_{pvVSI}	Proportional gain of voltage controller	0.029
k_{ivVSI}	Integral gain of voltage controller	78.5398
L_{AFE}	Inductance of AFE	0.47 mH
C_{dc}	DC link capacitor of AFE	100 μF
V_{ll}	Grid line-line peak voltage	$57.5\sqrt{6}$ V
R_{dc}	Load resistor of AFE	96 Ω
V_{dcAFE}	DC voltage of AFE	320 V
V^s_d	*d* channel voltage of the AC input	99.6 V
k_{piAFE}	Proportional gain of AFE current controller	0.0098
k_{iiAFE}	Integrator gain of AFE current controller	19.635
k_{pvAFE}	Proportional gain of AFE voltage controller	0.1414
k_{ivAFE}	Integrator gain of AFE voltage controller	7.3631
$k_{ppllAFE}$	Proportional gain of AFE PLL	2.019
$k_{ipllAFE}$	Integral gain AFE of PLL	634.2
L_f	Inductance of AFE input filter	120 μH
C_f	Capacitance of AFE input filter	10 μF
R_{Cf}	Series damping resistance of C_f	1 Ω
T_{dt}	Dead time of AFE and VSI	2 μs

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