An Adaptive Framework for Mitigating Current Harmonics Caused by Distributed Energy Resources

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***Abstract*—When connected to distribution networks with distorted grid voltages, inverters can easily produce high levels of current harmonics. When these networks have high interface impedances, the control schemes designed to mitigate these harmonics can easily become destabilized. This paper demonstrates a multirate controller that can adapatively generate harmonic currents as needed at frequencies up to nearly half the sample rate. The controller is shown to be stable even with purely inductive grid impedances as high as 10% per unit. Both simulation and experimental results are presented.**

***Index Terms*—Power converter, power system harmonics**

I. Introduction

The dynamics of traditional power systems are concentrated well below the fundamental system frequency. Since there are no appreciable dynamics at higher frequencies, harmonic signals and their impact on power quality can be treated using steady-state techniques [1], [2]. As more power-electronic devices integrate into the distribution network, however, this decoupling disappears [3]. By their very nature, power electronics require wide control bandwidths, meaning that small stability margins may exist either above or below the fundamental system frequency. This can be problematic when devices are connected to non-ideal distribution networks possessing harmonic distortion and non-zero interface impedance. Sustained oscillations above the fundamental can easily occur if the grid impedance possesses the characteristics needed to destabilize a converter at a certain frequency.

Although designers can limit bandwidths to prevent undesirable interactions, the potential impact of grid distortion makes it necessary to achieve high performance at relatively high frequencies. Recent studies have shown, for instance, that many commercially available distributed energy resources (DERs) that meet appropriate regulations when connected to a harmonic-free grid often violate current harmonic limits if the grid voltage has as little as $3\,\%$ harmonic distortion [4]. For context, IEEE Standard 519 now allows total voltage harmonic distortion as high as $8\,\%$ [5]. Additional studies indicate that high levels of DER penetration can lead to significant spectral content at frequencies above the 20th harmonic [6]. These findings suggest that DERs must be able to operate stably at multiple harmonics regardless of the grid conditions. The challenge is that distribution networks are dynamic, time-varying environments, making it difficult for either utilities or power-electronics engineers to predict the conditions to which DERs will be subjected when field-deployed. Robust and adaptive control is thus essential if both power quality and stability are to be ensured.

To mitigate unwanted harmonic content, DERs must have sufficient loop gain at the appropriate frequencies. Typically, this includes the fundamental and certain odd multiples. Several schemes have been designed to achieve this requirement, and these schemes typically utilize either multiple resonant control (MRSC) [7]–[12] or repetitive control (RC) [13]–[30]. These methods are commonly integrated with some means to reduce the impact of the resonance caused by the LCL filter at the grid interface. Example approaches include capacitor voltage or current feedback and notch filtering [31]. Such controllers are relatively easy to stabilize when connected to a stiff grid possessing minimal inductance. If the grid has a non-negligible impedance, however, such schemes can cause low-frequency harmonics or even instability.

This paper proposes an alternate scheme utilizing a multirate controller. A low-bandwidth outer-loop digital control system generates a set of amplitude commands used to synthesize a reference for an analog peak current controller. This inner system acts to control the current in the inverter-side inductor. The Discrete Fourier Transform (DFT) determines the harmonic content in the grid-side current and its outputs are compared to the reference amplitudes once each line cycle. Simulation results demonstrate that this controller is stable at frequencies reaching nearly half the sample rate even when the grid impedance is purely inductive at $10\,\%$ per unit.

This paper demonstrates the effectiveness of the proposed control system. Section II first describes the basic concept and its implementation. Section III then utilizes simulation studies to demonstrate its effectiveness in comparison to a multiple resonant controller. Section IV provides experimental results using a new AC-stacked architecture. The paper concludes with a discussion on future work.

II. Controller Implementation

Fig. 1 shows the basic connections for the proposed controller. Note that we measure both the inductor current $i_L(t)$ and the grid current $i_G(t)$. The inductor current is passed to an analog peak current controller that determines the appropriate switching signals. A microcontroller uses measurements of the

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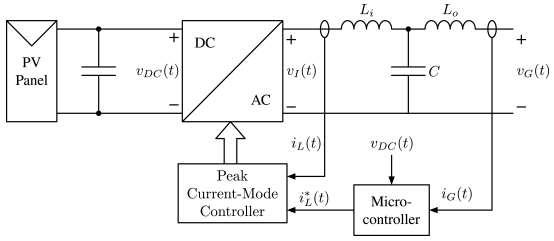


Fig. 1. Connection diagram showing the basic elements of the proposed mixed-signal control scheme.

grid current to determine the reference waveform $i_L^*(t)$. This multirate, mixed-signal control system implements a version of dq-frame control [32]–[34]. Assuming a harmonic-free grid voltage of the form $V_G \sin(\omega_1 t)$, then the dq controller acts to generate a current reference of the form

$$i_G(t) = I_1 \sin(\omega_1 t + \theta_1), \tag{1}$$

where the phase offset θ_1 represents the potential desire to source or sink reactive power. This waveform is generated using the d and q-axis references

$$I_{d,1}^* = I_1 \cos(\theta_1), \tag{2}$$

and

$$I_{q,1}^* = I_1 \sin(\theta_1). \tag{3}$$

These slowly-varying signals exist in a frame rotating synchronously with the grid voltage. They are mapped to stationary-frame currents using the transformation

$$\begin{bmatrix} I_{d,1}^* \\ I_{q,1}^* \end{bmatrix} = \begin{bmatrix} \cos(\phi) & \sin(\phi) \\ -\sin(\phi) & \cos(\phi) \end{bmatrix} \begin{bmatrix} i_{\alpha,1}^*(t) \\ i_{\beta,1}^*(t) \end{bmatrix} \tag{4}$$

where $\phi = \omega_1 t - \frac{\pi}{2}$. The stationary-frame reference currents are thus

$$i_{\alpha,1}^*(t) = I_1 \sin(\omega_1 t + \theta_1) \tag{5}$$

and

$$i_{\beta,1}^*(t) = -I_1 \cos(\omega_1 t + \theta_1). \tag{6}$$

In traditional dq-based control, these signals are references for the modulator generating the switching waveforms. The control system operates by continuously transforming the measured grid current into the rotating dq-frame. The measured dq currents are then compared to $I_{d,1}^*$ and $I_{q,1}^*$. Appropriate compensators minimize the error between the commanded and actual dq-frame currents.

Harmonics make it difficult to implement the traditional dq approach in single-phase applications [35]. When significant harmonics are present, the dq quantities develop time-varying sinusoidal signals in addition to their nominal DC values. Additional filtering is then needed to extract the necessary information. Each harmonic of interest requires a separate dq-transformation and additional filtering [35]. At the fundamental and each harmonic, one also also needs to synthesize a set of signals locked in phase and in quadrature with the corresponding grid current at that frequency. This is potentially difficult to implement.

Fig. 2 shows the alternative dq-type scheme proposed in this paper. This method utilizes the DFT to determine the appropriate d and q-axis quantities. The final output of this controller is the grid current $i_G(t)$, which is now assumed to have harmonics. In this case, we assume the grid current to have a constant amplitude and phase over a single line cycle although both can vary from one cycle to the next. If so, we can denote the grid current over the mth cycle as

$$i_G(t) = \sum_{k=1}^{\infty} I_k[m] \sin(k\omega_1 t + \theta_k[m]). \tag{7}$$

This signal is filtered and sampled to yield $i_G[n]$. Assuming the sampling rate is an integer multiple N of the fundamental frequency f_1, then $i_G[n]$ can be expressed as

$$\begin{aligned} i_G[n] &= i_G(t)\Big|_{t=n/(Nf_1)} \\ &= \sum_{k=1}^{\frac{N}{2}} I_k[m] \sin(2\pi kn/N + \theta_k[m]) \\ &= \sum_{k=1}^{\frac{N}{2}} \big[I_k[m] \cos(\theta_k[m]) \sin(2\pi kn/N) \\ &\qquad + I_k[m] \sin(\theta_k[m]) \cos(2\pi kn/N) \big]. \end{aligned} \tag{8}$$

For $k = 1$, we note that the two corresponding amplitudes in Eq. 8 are the same as the desired amplitudes presented in Eqs. 2 and 3. In general, the amplitudes at the kth harmonic correspond to the dq currents in a frame rotating at $k\omega_1$. Thus, we can rewrite Eq. 8 as

$$\begin{aligned} i_G[n] = \sum_{k=1}^{\frac{N}{2}} \big[& I_{d,k}[m] \sin(2\pi kn/N) \\ & + I_{q,k}[m] \cos(2\pi kn/N) \big]. \end{aligned} \tag{9}$$

In a typical dq-approach, one would use $i_G[n]$ to compute $i_{\alpha,k}(t)$ and $i_{\beta,k}(t)$. These would then need to be transformed into the dq frame. Instead of performing that transformation directly, however, we compute the DFT of $i_G[n]$ over a single period. We express the resulting DFT samples over the mth period as $X_k[m]$. If N is even and a separate control system acts to remove any DC content from the current, then the inverse DFT of $i_G[n]$ is

$$\begin{aligned} i_G[n] = \frac{2}{N} \sum_{k=1}^{\frac{N}{2}-1} \big[& \mathrm{Re}\{X_k[m]\} \cos(2\pi kn/N) \\ & - \mathrm{Im}\{X_k[m]\} \sin(2\pi kn/N) \big]. \end{aligned} \tag{10}$$

Comparing (9) and (10) shows that for $1 \le k < \frac{N}{2}$

$$I_{d,k}[m] = -\frac{2}{N} \mathrm{Im}\{X_k[m]\} \tag{11}$$

$$I_{q,k}[m] = \frac{2}{N} \mathrm{Re}\{X_k[m]\}. \tag{12}$$

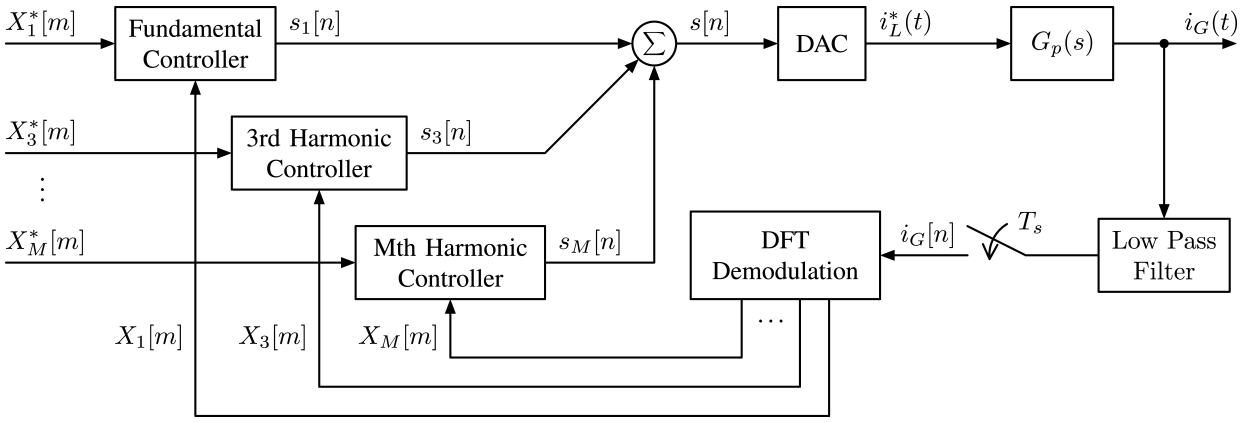


Fig. 2. High-level block diagram of the proposed control system.

Eqs. 11 and 12 demonstrate that the DFT coefficients are simply the d and q-axis currents at the kth harmonic. This simplification, which requires the sampling window to be well aligned with the fundamental period, allows the dq components to be easily computed in the discrete-time domain. Successful implementation, however, requires two key elements. First, there must be a robust mechanism for keeping the sampling window synchronized to the line current. Second, the harmonic content must be remain relatively constant over a single period of the fundamental.

Fig. 2 shows that we compute the complex amplitudes $X_k[m]$ at the fundamental and $M-1$ harmonics. Each of these complex signals is calculated once per line cycle and fed to the corresponding harmonic controller where it is compared to a complex reference $X_k^*[m]$. The output of the kth harmonic controller is a single digital signal $s_k[n]$ containing samples of the desired reference current at the frequency $k\omega_1$. These M signals are summed within the microcontroller and passed to a digital-to-analog converter (DAC) that synthesizes the complete reference $i_L^*(t)$. This signal is fed to the subsystem $G_p(s)$, which we define as the plant. Fig. 3 shows that this subsystem consists of a mixed-signal circuit comparing i_L^* and i_L. The inverter output voltage $v_I(t)$ drives the output filter. The grid current is the final output which is fed back to the outer digital loop operating at line frequency.

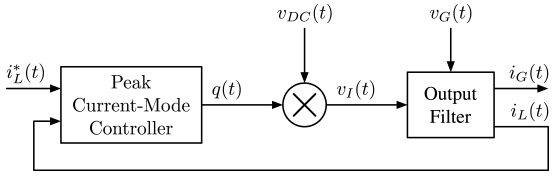


Fig. 3. Model of the plant, $G_p(s)$.

Fig. 4 shows a more complete version of the controller implemented at each harmonic frequency. Each controller has two signal paths, one for the real part of X_k, which corresponds to the q-axis component of $i_{G,k}$, and one for the imaginary part, which corresponds to the d-axis component of $i_{G,k}$. Each signal path has its own digital PI compensator designed to force zero steady-state error to a constant reference. The compensator outputs are upsampled to a much higher rate and then scaled by the appropriate carrier waveform. The final output $s_k[n]$ is combined with the corresponding signals from the other harmonic controllers to create the complete digital reference $s[n]$.

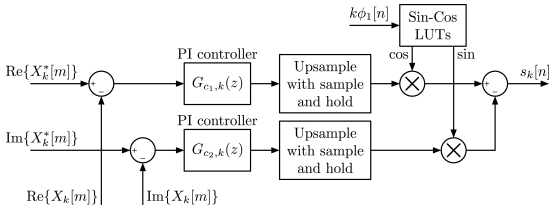


Fig. 4. Controller implemented at the kth harmonic.

III. Stability Analysis and Comparison to Multiple Resonant Control

This section investigates the stability of the proposed controller and compares it to that of the more standard multiple resonant controller. We first propose a simple analytical model and use it to predict the results from a simulated converter under both stiff and weak grid conditions. We then compare the performance to a converter using multiple resonant controllers.

A. Simplified Model and Stability Analysis

Fig. 5 shows a simplified model for the control system described in the previous section. This model shows only the behavior at a single harmonic frequency. This model begins by recognizing that the outer digital loop in Fig. 2 provides only a very low frequency set of amplitude commands to the peak-mode current controller that sets the actual inverter currents. At the kth harmonic, therefore, we can represent the inverter and analog controller simply as a set of constant gains derived directly from the value of $G_p(s)$ for $s = \jmath k\omega_1$. Since we are generating both d and q-axis currents, this plant is really a two-input, two-output transfer function matrix, $G_{p,k}(z)$. We evaluate this in the z-domain since the outer

loop is implemented digitally. The transfer function matrix evaluated at the kth harmonic is simply

$$G_{p,k}(z) = \begin{bmatrix} \mathrm{Re}\{G_p(jk\omega_1)\} & -\mathrm{Im}\{G_p(jk\omega_1)\} \\ \mathrm{Im}\{G_p(jk\omega_1)\} & \mathrm{Re}\{G_p(jk\omega_1)\} \end{bmatrix}. \quad (13)$$

In our design, the proportional and integral gains are identical for any given harmonic. The PI compensators are thus

$$G_{c_1,k}(z) = G_{c_2,k}(z) = G_{c,k}(z) = K_{P,k} + \frac{K_{I,k}}{f_1}\frac{z}{z-1}. \quad (14)$$

Note that the unit-delay elements in Fig. 5 represent the computation time required to sample $i_G(t)$ and compute $X_k[m]$. The complete loop gain matrix is ultimately

$$L_k(z) = z^{-1}G_{c,k}(z)G_{p,k}(z). \quad (15)$$

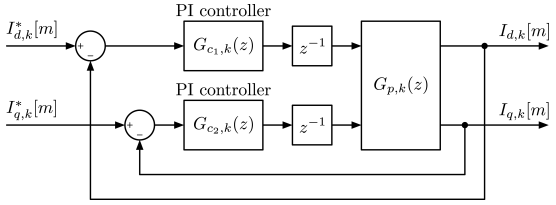


Fig. 5. Simplified discrete-time model of system.

To investigate the validity of the simplified model, we simulated the converter with the parameter values identified in Table I. Simulink was chosen as the modeling tool. To compare the simulated results to the predictions from the simplified model, we must have a a set of values to populate the transfer function matrix presented in Eq. 13. Since it is very tedious to derive a closed-form model for a peak-mode current controller [36], we developed an empirical model for $G_p(s)$ by simply perturbing the system around a particular operating point. Specifically, we perturbed the steady-state current given in Eq. 7 at each harmonic from the fundamental out to half the sampling frequency. Fig. 6 shows the resulting transfer function assuming a typical level of grid distortion. Note that we determined the transfer function for several different grid impedance values. The bounding cases are a stiff grid with $L_g = 0$, and an extremely weak grid having a pure inductance at $10\,\%$ per unit. Since the system was designed to be provide $4.8\,\mathrm{kW}$ into a $240\,\mathrm{V}$ single-phase network, the chosen weak grid condition corresponds to $L_g = 3.2\,\mathrm{mH}$. Typically, $10\,\%$ per unit is considered a worst case condition for grid impedance [31], [37]. When evaluating performance, we chose appropriate values from $G_p(s)$.

We conducted several tests to compare the simulated performance to that predicted by the mathematical model presented in Fig. 5. Fig. 7 shows the modeled and simulated response to a combined step in the amplitude and phase at the fundamental. Note that the current amplitude was increased by $0.5\,\mathrm{A_{rms}}$ and the phase was increased by $5°$. Similarly, Fig. 8 shows the modeled and simulated responses to a step in the d and q-axis coefficients at the 17th harmonic in response to a command to mitigate any current distortion at that frequency. Note the close agreement in all four results. In the case of the 17th harmonic, there is a slight amount of oscillation in the simulation results. This oscillation is very small, and it was determined to be caused by a numeric issue in the simulation resulting from a discrete-time simulation of the typically continuous-time peak-mode current controller. Note that the results shown in Figs. 7 and 8 were obtained assuming $500\,\mu\mathrm{H}$ of grid-side inductance.

TABLE I
SIMULATION PARAMETERS

Symbol	Parameter	Value
f_{sw}	switching frequency	$30\,\mathrm{kHz}$
V_{DC}	DC bus voltage	$32\,\mathrm{V}$
L_i	inverter-side inductance	$330\,\mu\mathrm{H}$
r_i	inverter-side inductor parasitic resistance	$10\,\mathrm{m\Omega}$
C	LCL-filter capacitance	$10\,\mu\mathrm{F}$
r_c	LCL-filter capacitor parasitic resistance	$10\,\mathrm{m\Omega}$
L_o	grid-side inductance	$330\,\mu\mathrm{H}$
r_o	grid-side inductor parasitic resistance	$0\,\Omega$
$L_{g,st}$	grid inductance for the stiff grid	$0\,\mathrm{H}$
$L_{g,wk}$	grid inductance for the weak grid	$3.2\,\mathrm{mH}$

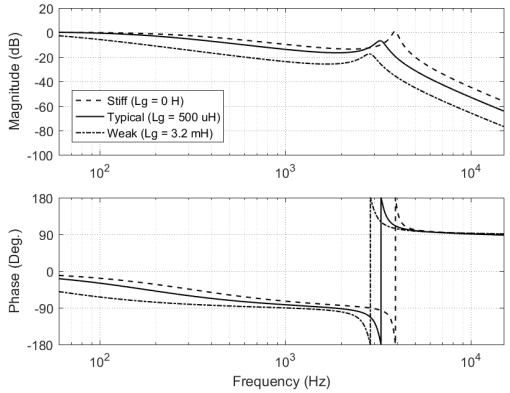
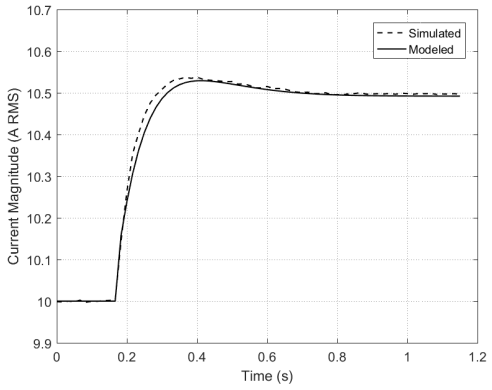


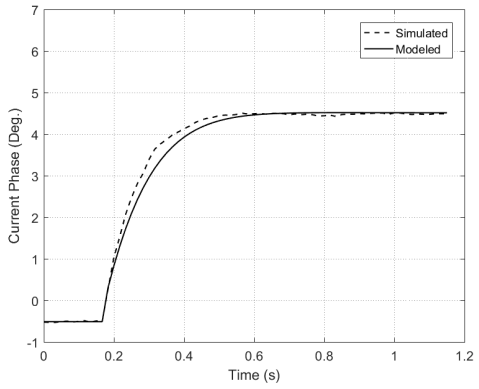
Fig. 6. $G_p(s)$ for several grid-side impedance values with a distorted grid voltage.

The analytical model presented in Fig. 5 allows us to investigate the stability of the proposed controller in the face of variations in the grid impedance. In general, the closed-loop transfer matrix for the simplified discrete-time model has two pairs of complex-conjugate poles in the z-plane. To evaluate stability, we examined the range of controller gains K_P and K_I that would keep these poles within the unit-circle at any given harmonic under the weak grid condition. Fig. 9 shows the range of controller gains for which the controller is stable at each of several different harmonics. In general, this control system should be stable up to nearly half the sample rate since there is minimal negative phase shaft in the loop gain. We note that the system is clearly stable out to the 41st harmonic, although the range of controller gains is somewhat limited.

In a robust system we would obviously prefer to keep



(a)



(b)

Fig. 7. Response to a change at the fundamental (a) $0.5\,\mathrm{A_{rms}}$ step change (b) $5°$ step change.

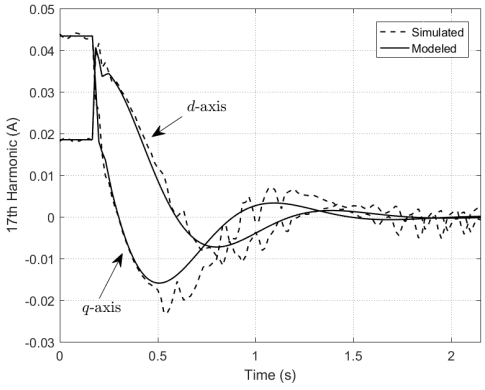


Fig. 8. Simulated and modeled dq-frame currents at the 17th harmonic. following a command to reduce the currents to zero.

the poles well inside the unit circle. To understand how this desire for robustness impacts our ability to reject higher-order harmonics, we attempted to impose a minimum $30°$ phase-margin requirement. To do so, we assumed that the pole pair closest to the unit circle would dominate the response and we transformed it into the continuous-time domain using the transformation $z = \exp(s/f_1)$. Using this approach,

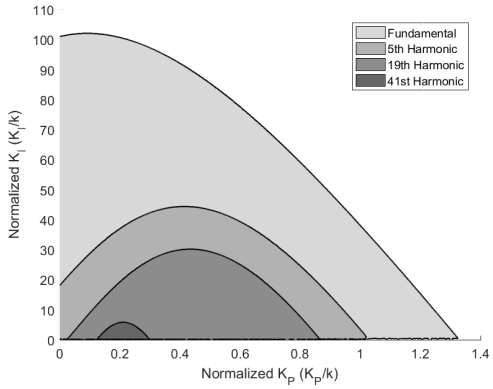


Fig. 9. Stability regions for the fundamental, 5th, 19th, and 41st harmonics of the weak grid condition. Note that K_P and K_I gain coefficients are normalized by the harmonic order, k.

an equivalent discrete-time damping ratio was determined. We then related this damping ratio to a phase margin using appropriate approximations [36]. Fig. 10 shows the controller gains corresponding to an approximate $30°$ phase margin at several different harmonic numbers. We note that the regions are slightly smaller than the corresponding stability regions, but robustness is clearly achieved.

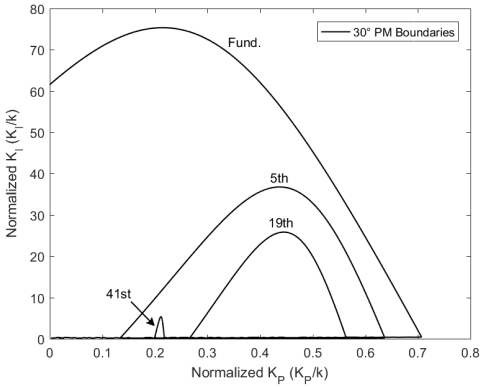


Fig. 10. $30°$ phase margin boundaries for the fundamental, 5th, 19th, and 41st harmonics of the weak grid condition. Note that K_P and K_I gain coefficients are normalized by the harmonic order, k.

B. Comparison to a Multiple Resonant Controller

To demonstrate the capabilities of the proposed controller, we compared its performance to that achieved using a multiple resonant controller of the form

$$G_c = K_P + \sum_{k=1,3,5,\ldots} K \frac{2k\zeta\omega_1 s}{s^2 + 2k\zeta\omega_1 s + (k\omega_1)^2}. \qquad (16)$$

This compensator is essentially a damped proportional-plus-resonant (PR) controller. Despite the number of publications available on these systems, the literature still includes relatively limited guidance on the the selection of suitable

design parameters. Using guidelines published in [38], we first selected a K_P value assuming no resonant controllers would be used. This sets the dynamics of the underlying system. Noting that the resonant terms only provide additional negative phase shift at crossover, we selected K_P to achieve an initial phase margin of $60°$ when connected to the stiff grid. Each resonant stage was then designed to achieve a particular metric for steady-state error. As in [38], we set the bandwidth at each harmonic to be $\pm k\,\mathrm{Hz}$, and we selected K and ζ so that the steady-state phase error at the pass band edges at the fundamental would be approximately $2.56°$. This value ensures that a power factor of at least 0.999 is achievable within the entire $\pm 1\,\mathrm{Hz}$ band around the fundamental. Selection of the error criteria at the harmonics is slightly less clear, as most authors seem to focus solely on meeting requirements imposed by regulatory bodies rather than attempting to drive the harmonics to some true minimum. In any event, this phase error achieved using this method does not increase significantly at the higher harmonics and the harmonic levels are below IEEE 1547 requirements.

Fig. 11 shows the loop gain using the proposed multiple resonant controller. The stiff grid again has $L_g = 0$. With this controller, however, a purely reactive weak grid with $10\,\%$ impedance has an unacceptably low crossover and will have difficulty compensating any harmonics. We instead considered a weak grid having a $40\,\%$ X/R ratio at $10\,\%$ per unit magnitude, which is actually much closer to what is typically considered in the literature [31]. As shown, the system has a crossover near the 12th harmonic when connected to the weak grid. When attempting to cancel out to the 11th harmonic, the phase margin is reduced to approximately 30°. Additional compensators would only further reduce the phase margin of the underlying system and might potentially cause the system to be unstable near the higher harmonics.

Note that both compensators considered here, i.e. the multiple resonant version and our proposed system, were both designed assuming the same inverter hardware. Our design was able to provide a comparable phase margin at a harmonic frequency in excess of the 40th and it was able to do so assuming a far weaker grid scenario. Had we considered a grid with some resistance, our system could easily compensate more harmonics.

IV. Experimental Results

The proposed control scheme has been extensively tested in the laboratory using the stacked AC architecture described in [39], [40]. Each inverter in this architecture switches at $500\,\mathrm{kHz}$. Operation at this frequency enables significant miniaturization of the passive components in the LCL-filter, and the fact that each converter only produces approximately $15\,\mathrm{V_{rms}}$ allows the use of low-voltage MOSFET switches to maintain conversion efficiency [40]. The approach is different than a cascaded H-Bridge topology, as control is fully decentralized [40]. A grid-interface termination box provides protection features and the grid-side inductor. The only required communications is a low-bandwidth $60\,\mathrm{Hz}$ pulse transmitted over the power line to synchronize the operation of each inverter [40]. A $120\,\mathrm{V_{rms}}$ unit consisting of eight inverters was successfully field-deployed for several months [41]. For the purposes of this paper, testing was performed using the simple three-inverter topology shown in Fig. 12. The grid is provided by connecting the network to a distorted grid through a variable transformer. Table II summarizes the relevant parameter values for this experimental setup, and Fig. 13 shows the arrangement in the laboratory.

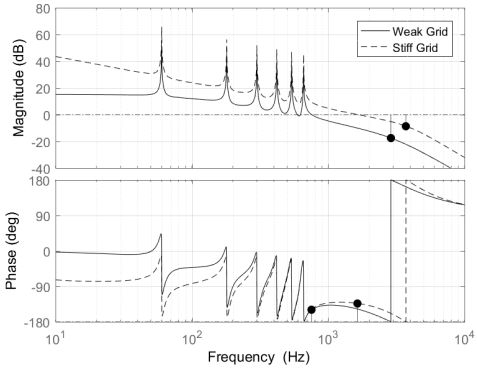


Fig. 11. Bode plot for designed PR+HC current control. Minimum gain and phase margins for the weak grid condition: gain margin = 17.63 dB at 2.88 kHz and phase margin = 30.15° at 755.57 Hz. Minimum gain and phase margins for the stiff grid condition: gain margin = 8.69 dB at 3.72 kHz and phase margin = 46.73° at 1.64 kHz.

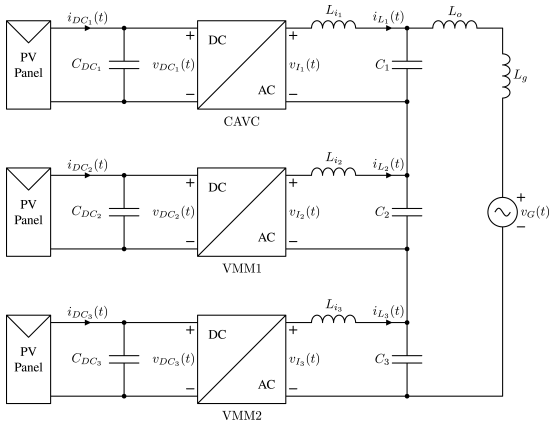


Fig. 12. The low-voltage, AC-stacked topology. This implementation only has 3 inverters, but the approach is scalable according to the network voltage.

Fig. 14 shows the open-circuit grid voltage in the laboratory. Note that the overall voltage THD is $8.063\,\%$, which is slightly above the recommended maximum, but clearly possible in practice [5]. Fig. 15 shows the measured grid current before and after the converter began to cancel distortion at harmonic numbers $3, 5, 7, 9, 11, 13,$ and 15. The THD of the current waveform reduces from $18.522\,\%$ to $1.282\,\%$.

One of the primary attractions of this approach is its ability to adapt to changing grid conditions. Recall that we initially only compensated for odd harmonics out to the 15th. Since we

TABLE II
EXPERIMENTAL SETUP PARAMETERS

Symbol	Parameter	Value
f_{sw}	switching frequency	500 kHz
V_{DC}	DC bus voltage	32 V
L_i	inverter-side inductance	10.5 µH
C	LCL-filter capacitance	6 µF
L_o	grid-side inductance	50 µH

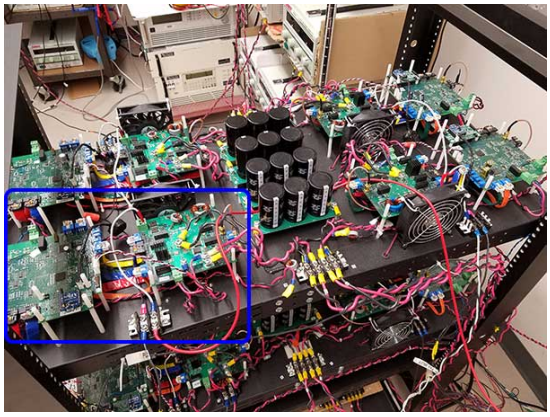


Fig. 13. Laboratory arrangement for the AC-stacked architecture. The two PCBs that comprise one prototype inverter are highlighted.

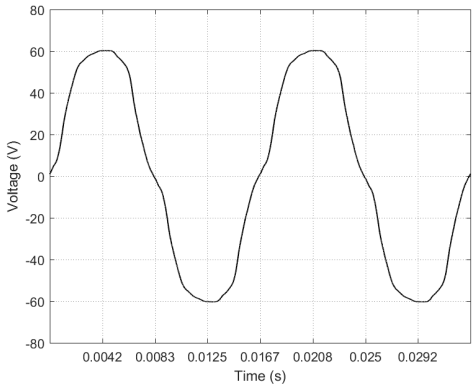


Fig. 14. Measured grid voltage in the lab. Note that the amplitude is only about 45 V_{AC} because only three inverters are used. The voltage here is measured on the output side of a variac.

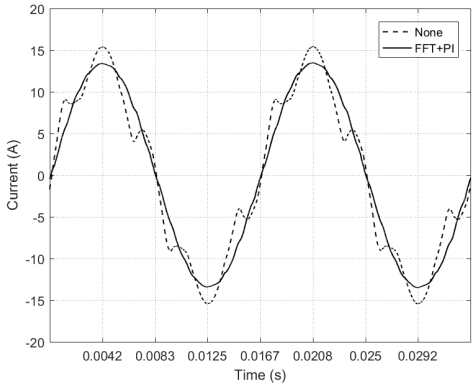


Fig. 15. Measured grid current with and without harmonic compensation.

are continuously computing the DFT of the current, however, we can easily detect when a given harmonic becomes large enough that it requires compensation. After running for some time generating the compensated current shown in Fig. 15, the system detected the presence of appreciable harmonic content at the 17th and 19th harmonics. The impact on the THD is shown in Fig. 16. Clearly, the spectral content is further reduced at these higher order harmonics.

V. CONCLUSION

The controller presented in this paper can adaptively mitigate a significant number of harmonic currents. Section III demonstrated that the proposed scheme can mitigate many more harmonics than a similar multiple resonant controller without compromising stability even in cases where the grid is extremely weak and purely reactive. Furthermore, the stability analysis was performed using only a simulated converter operating at 30 kHz. When combined with the 500 kHz AC-stacked architecture, this control scheme can theoretically compensate for harmonics well beyond the 50th which is the highest considered in IEEE Standard 1547 [42].

Although the proposed scheme is promising and has been demonstrated in the field, there are some potential limitations. First, we have assumed the grid current amplitude and phase to be constant at each harmonic over a single period of the fundamental. Although we have found no issues with this in the field, it merits closer investigation. Second, we need to further study the impact of a varying line frequency on the ability of the DFT to appropriately calculate the harmonic amplitudes. If the sampling clock is not perfectly aligned with the period of the current, this can potentially cause problems although no significant issues have been discovered during field tests. Future publications will address these issues.

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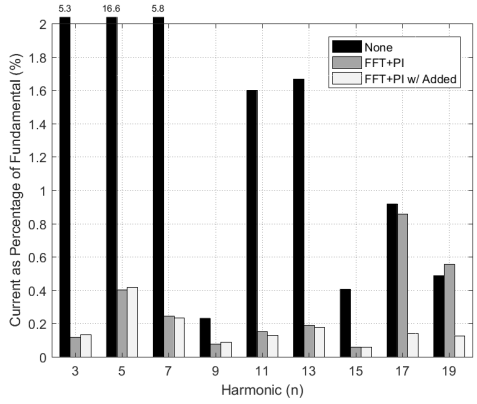

Fig. 16. Current harmonic amplitudes in each of three conditions: (1) Without compensation, (2) using the proposed FFT-based compensator out to only the 15th, and (3) using the the proposed FFT-based compensator out to the 19th.

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