Design and Performance Improvement for Single-Voltage-Loop Controlled Voltage-Source-Converters with a Low *LC*-Resonant-Frequency

Xiaoqiang Li[1], Pengfeng Lin[2], and Yi Tang[1]
[1]School of Electrical and Electronic Engineering
[2]Interdisciplinary Graduate School
Nanyang Technological University
Singapore
lixiaoqiang@ntu.edu.sg, LINP0010@e.ntu.edu.sg,
yitang@ntu.edu.sg

Kai Wang
School of Electrical and Power Engineering
China University of Mining and Technology
Xuzhou, China
career_wkai@163.com

***Abstract*—In order to improve the disturbance rejection capability of capacitor voltage and also effectively attenuate the switching voltage harmonics, a large filter capacitance in *LC*-filters is preferred in practical applications, thus generally leading to a low *LC*-resonant-frequency. For conventional proportional-resonant (PR) voltage controllers, the single-voltage-loop control could only be stable with a high *LC*-resonant-frequency, e.g., greater than 1/3 of system sampling frequency. In this paper, a design method of single-voltage-loop control is presented for voltage-source converters (VSCs) with a low *LC*-resonant-frequency. Instead of using a positive proportional gain in the PR voltage controller, it is found that a negative proportional gain can achieve a different stability design region, i.e., less than 1/3 of system sampling frequency, thus low *LC*-resonant-frequency VSCs can be stable. Furthermore, in order to avoid the poor dynamic performance caused by the negative proportional gain, a closed-loop zeros configuration based control method is proposed. With this control, the dynamic performance can be designed independently without affecting system stability. Finally, experimental results are provided to verify the effectiveness of the proposed method.**

***Keywords*—Closed-loop zeros; dynamic performance; low *LC*-resonant-frequency; single-voltage-loop; stability design region; voltage-source-converters (VSCs)**

I. Introduction

Voltage-controlled voltage-source converters (VSCs) have been widely used in many power conversion applications, such as 50/60-Hz uninterruptible power supplies (UPS) [1], [2], 400 Hz ground power units (GPU) for airplanes [3], and dynamic voltage restorers (DVRs) [4]. An *LC*-type output filter is normally demanded in these applications to suppress converter switching ripples and provide high-quality output voltage. However, the *LC*-filter resonance may cause system instability.

To ensure system stability, one commonly used method is the double-loop control scheme, which consists of an outer capacitor voltage loop and an inner inductor- or capacitor-current loop [2], [4]-[7]. Another recently attractive solution to the stability issue is the single-loop control, where only a capacitor voltage loop is implemented [3], [8]. Consequently, the control structure and parameters design can be greatly simplified, and current sensors for the internal current loop can be saved. In [7] and [8], it was revealed that resonant frequency ω_r of *LC*-filter should be designed to be greater than 1/3 of system sampling frequency, i.e., $\omega_r>\omega_s/3$, when a proportional-resonant (PR) or proportional-integral (PI) controller is used for the output voltage control. However, in practical applications, in order to improve disturbance rejection capability of the capacitor voltage and also attenuate switching voltage harmonics effectively, a large filter capacitance is commonly adopted, thus generally leading to a low *LC*-resonant-frequency. This design constraint is therefore difficult to be satisfied. In [8], only a resonant (R) controller was adopted to regulate the output voltage, and it was shown that the stability design region of *LC*-filter can be extended to $\omega_s/6$, i.e, $\omega_r>\omega_s/6$. Nevertheless, this method is still restricted for a lower *LC*-resonant-frequency, and the system cannot be stabilized when $\omega_r<\omega_s/6$. Moreover, the system dynamic is also limited as only a resonant controller is involved in the voltage control.

In this paper, a design method of single-loop voltage control is proposed for low *LC*-resonant-frequency VSCs. In this method, by using a negative proportional gain in the PR voltage controller, it is found that the stability design region of *LC*-filter becomes $\omega_r<\omega_s/3$. The detailed design guidance with specified stability margin requirements is also presented. In addition, a closed-loop zeros configuration based control method is proposed, which can improve system dynamic performance without affecting system stability.

II. Proposed Design Method for Low *LC*-Resonant-Frequency VSCs

Fig. 1 shows a single-phase *LC*-filtered voltage-controlled VSC, and Fig. 2 shows the voltage control diagram in the continuous *s*-domain, where $G_c(s)$ is the PR voltage controller, $G_d(s)$ is the equivalent 1.5 sampling periods of control delay [8], [9], and $G_{vc}(s)$ is the transfer function from converter-side voltage $v_i(s)$ to capacitor voltage $v_c(s)$.

From Fig. 2, the open-loop transfer function $T_o(s)$ can be derived as

$$T_o(s) = G_c(s)G_d(s)G_{vc}(s)\,. \tag{1}$$

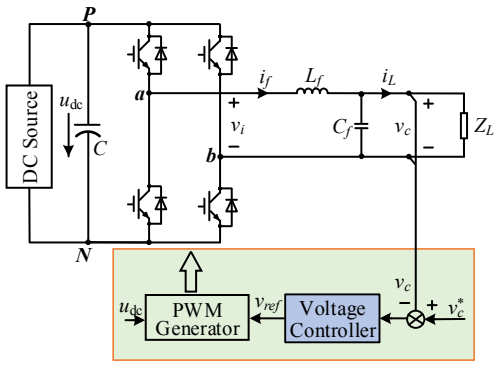


Fig. 1. A single-phase *LC*-filtered voltage-controlled VSC with single-voltage-loop control.

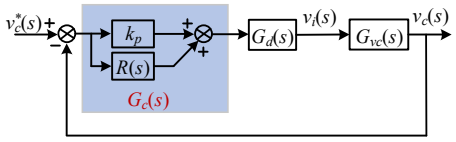


Fig. 2. Voltage control diagram in the continuous *s*-domain.

Since *LC*-resonant-frequency ω_r is normally far greater than fundamental frequency ω_1, the PR voltage controller can be seen as a proportional (P) controller in the high-frequency range for stability analysis.

A. P Controller with A Negative Proportional Gain k_p

Generally, proportional gain k_p of the PR voltage controller should be positive. Under this scenario, resonant frequency ω_r should be greater than $\omega_s/3$ to ensure system stability [7], [8]. In contrast, a negative proportional gain k_p is employed in this research, then the phase and magnitude of $T_o(s)$ can be derived as

$$\begin{cases} \angle T_o(j\omega) = \begin{cases} -\pi - 1.5\omega T_s, & \omega < \omega_r \\ -2\pi - 1.5\omega T_s, & \omega > \omega_r \end{cases} \\ \left| T_o(j\omega) \right| = \left| \dfrac{k_p \omega_r^2}{\omega_r^2 - \omega^2} \right| \end{cases}, \qquad (2)$$

where T_s is the sampling period.

According to the Nyquist stability criterion, the encirclements N of (-1, j0) by the Nyquist curve of $T_o(s)$ should be zero to ensure system stability due to no unstable open-loop poles. To achieve this, the phase of $T_o(s)$ at resonant frequency ω_r should be greater than -3π, then it can be derived as

$$-2\pi - 1.5\omega_r T_s > -3\pi \Rightarrow \omega_r < \omega_s / 3 . \qquad (3)$$

Fig. 3 shows the Bode plots of $T_o(s)$ with a negative proportional gain k_p. As seen, there are two critical phase crossings (-180° and -540°), located at ω=0 and $\omega_s/3$ respectively when $\omega_r < \omega_s/3$ while located at ω=0 and ω_r respectively when $\omega_r > \omega_s/3$. Obviously, when $\omega_r > \omega_s/3$, the system cannot be stable since the -540° phase crossing at resonant frequency ω_r causes $N \neq 0$. Therefore, when with a

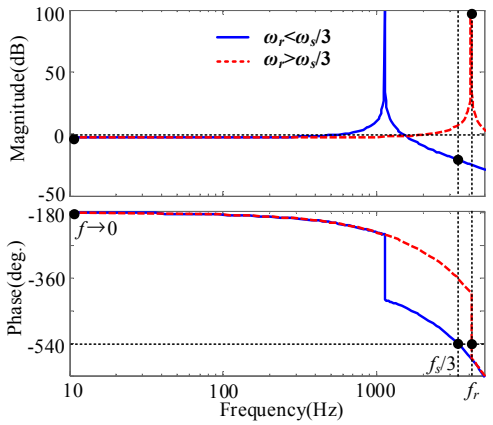


Fig. 3. Bode plots of open-loop transfer function $T_o(s)$ with a negative proportional gain k_p.

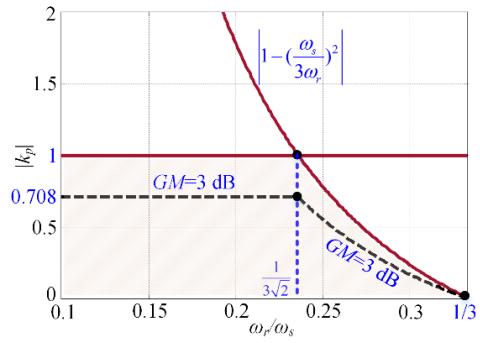


Fig. 4. Stability range of $|k_p|$ varying with resonant frequency ω_r.

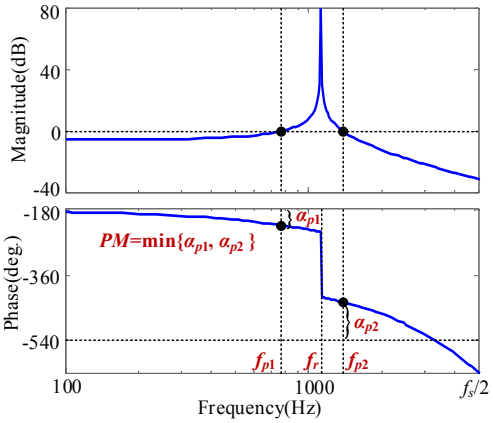


Fig. 5. Bode plots of open-loop transfer function $T_o(s)$ for PM design.

negative proportional gain k_p, the stability design region of *LC*-resonant-frequency is $\omega_r < \omega_s/3$. Following this design, the system with a low *LC*-resonant-frequency thus could be stable.

In order to ensure system stability when $\omega_r < \omega_s/3$, the magnitude of $T_o(s)$ should be less than 1 at both ω=0 and $\omega_s/3$. In other words, the gain margin (GM) should be greater than 0 dB. From (2) and Fig. 3, it can be obtained as

$$\text{GM} = \min\{-20\log_{10}|T_o(j0)|, -20\log_{10}|T_o(j2\pi f_s/3)|\} > 0\text{dB} \quad (4)$$
$$\Rightarrow |k_p| < \min\left\{1, \ |1-(\frac{\omega_s}{3\omega_r})^2|\right\}$$

The shaded area in Fig. 4 represents the stability range of $|k_p|$ varying with resonant frequency ω_r. As seen, $|k_p|$ should be less than 1 when $\omega_r < \omega_s/3\sqrt{2}$ while less than $|1-(\omega_s/3\omega_r)^2|$ when $\omega_s/3\sqrt{2} < \omega_r < \omega_s/3$. Furthermore, sufficient GM should be reserved and generally GM ≥3 dB. The dashed line in Fig. 4 represents the boundary of $|k_p|$ with GM ≥3 dB, and $|k_p|$ should be designed below this boundary.

In addition, sufficient phase margin (PM) should also be reserved for system stability and generally PM ≥30°. From Fig. 5, PM is equal to $\min\{\alpha_{p1}, \alpha_{p2}\}$. According to (2), $\alpha_{p1}=1.5\omega_{p1}T_s$ and $\alpha_{p2}=\pi-1.5\omega_{p2}T_s$. With $20\log_{10}|T_o(j\omega_{p1,2})|=0$ dB, $\omega_{p1} = \omega_r\sqrt{1-|k_p|}$ and $\omega_{p2}=\omega_r\sqrt{1+|k_p|}$. Then, it can be derived as

$$\text{PM} = \min\{\alpha_{p1}, \alpha_{p2}\} \geq 30^\circ$$
$$\Rightarrow |k_p| \leq \min\{1-\frac{\omega_s^2}{324\omega_r^2}, \frac{25\omega_s^2}{324\omega_r^2}-1\}. \quad (5)$$

The shaded area in Fig. 6 represents the stability design of $|k_p|$ varying with resonant frequency ω_r with PM ≥30° and GM ≥3 dB.

B. Closed-loop Zeros Configuration Based Control Method

From Fig. 2, the closed-loop transfer function $G_{cl1}(s)$ with a fundamental PR voltage controller can be derived as (6), where ω_1 is the fundamental frequency. From $G_{cl1}(z)$, it can be seen voltage controller $G_c(z)$ introduces two closed-loop zeros, given as (7).

$$G_{cl1}(s) = \frac{T_o(s)}{1+T_o(s)} = \frac{[k_p s^2 + k_i s + k_p\omega_1^2]G_d(s)G_{vc}(s)}{s^2+\omega_1^2+[k_p s^2+k_i s+k_p\omega_1^2]G_d(s)G_{vc}(s)}. \quad (6)$$

$$z_{1,2} = \frac{-k_i \pm \sqrt{k_i^2-4k_p^2\omega_1^2}}{2k_p}. \quad (7)$$

According to (7), if k_p>0, both z_1 and z_2 are located at the left-half-plane (LHP) of s-plane, while if k_p<0, these two zeros are located at the right-half-plane (RHP), indicating a non-minimum phase system. The RHP zeros will cause system undershoot and slow dynamic response [10]. In order to eliminate the RHP zeros caused by the negative proportional gain k_p, a closed-loop zeros configuration based voltage control is proposed, shown in Fig. 7, where a feedforward control of capacitor voltage is introduced with proportional coefficient $(1-m)k_p$ while the proportional gain of the PR controller is changed as mk_p.

From Fig. 7, the closed-loop transfer function $G_{cl2}(s)$ can be derived as (8). Comparing (8) with (6), it can be seen that the proposed control only changes the closed-loop zeros introduced by the PR voltage controller. Therefore, the proposed control would not affect system stability design. The new closed-loop zeros are given as (9).

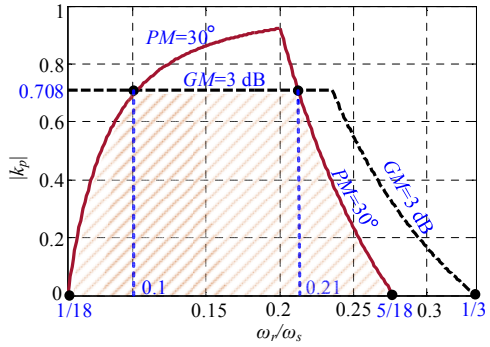


Fig. 6. Stability design of $|k_p|$ varying with resonant frequency ω_r with GM≥3 dB and PM ≥30°.

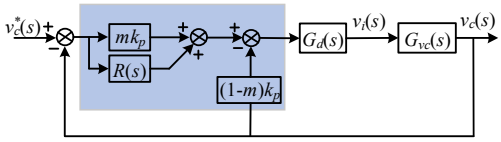


Fig. 7. Proposed voltage control method based on closed-loop zeros configuration.

$$G_{cl2}(s) = \frac{[mk_p+R(s)]G_d(s)G_{vc}(s)}{1+T_o(s)} = \frac{[mk_p s^2+k_i s+mk_p\omega_1^2]G_d(s)G_{vc}(s)}{s^2+\omega_1^2+[k_p s^2+k_i s+k_p\omega_1^2]G_d(s)G_{vc}(s)}. \quad (8)$$

$$z_{1,2} = \frac{-k_i \pm \sqrt{k_i^2-4m^2k_p^2\omega_1^2}}{2mk_p}. \quad (9)$$

In (9), if m is also less than 0, mk_p is greater than 0 and closed-loop zeros $z_{1,2}$ thus can be shifted from the RHP to the LHP of s-plane. Consequently, the adverse effects brought by the negative proportional gain k_p can be removed. As well known, the LHP zeros can make the dynamic response faster, but also can increase the overshoot, and these effects become prominent as the zeros move close to the imaginary axis. From (9), the position of the zeros can be adjusted by changing m, thus the system dynamic can be designed by tuning m independently.

III. Experimental Results

Under the conditions of L_f=1 mH, C_f=20 μF, f_{sw}=f_s=10 kHz and f_1=50 Hz, where f_{sw} is the switching frequency, ω_r/ω_s is equal to 0.113, then $|k_p|$ should be less than 0.708 according to Fig. 6. With this constraint, k_p is designed as -0.6 and k_i is designed as 300 with the requirement of steady-state error.

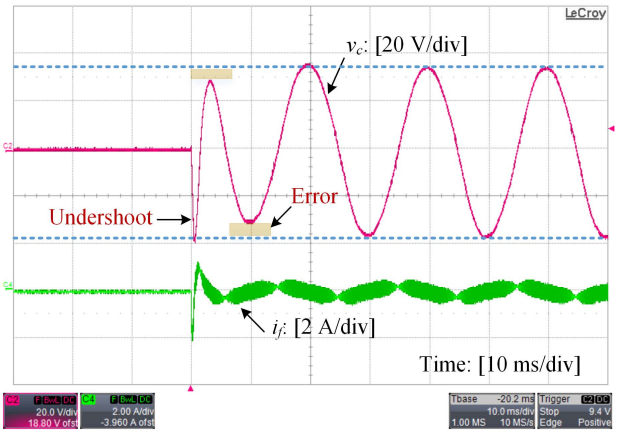


Fig. 8. Step response with the conventional control method.

Under the above design parameters, Fig. 8 shows the step response of the capacitor voltage with the conventional voltage control method shown in Fig. 2, where the system operates at the no-load condition to avoid physical resistive damping from the loads, and a cosine reference voltage $A_m\cos(\omega_1 t)$ is performed. By using a negative proportional gain k_p, it can be seen that the system works stably even if resonant frequency ω_r is less than $\omega_s/3$. As also seen, due to the presence of the RHP zeros caused by the negative k_p, the undershoot of the capacitor voltage appears during startup, and the system exhibits slow dynamic response, which indicates a poor dynamic performance.

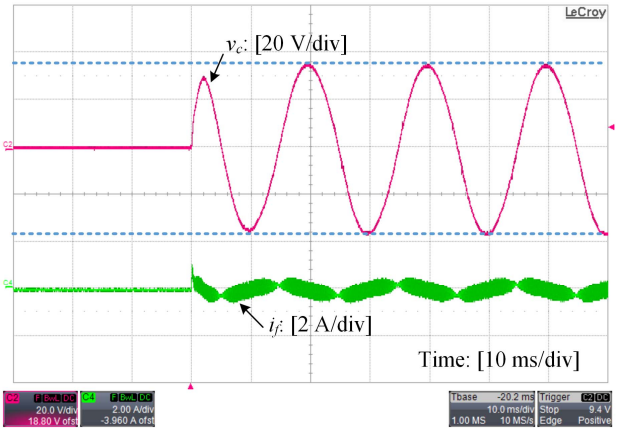
Fig. 9 further shows the step response of the capacitor voltage with the proposed voltage control method shown in Fig. 7, where m=-0.2, -0.5 and -0.7 respectively. As seen, the undershoot of the capacitor voltage disappears for all three cases, because the RHP zeros are shifted to the LHP of s-plane by the proposed control method. As also seen, with the increase of $|m|$, the response speed is improved but the overshoot increases, indicating that the system dynamic can be adjusted by m. Furthermore, it can also be seen that the system is always stable, because the proposed control method does not affect the stability design of voltage controller.

IV. Conclusion

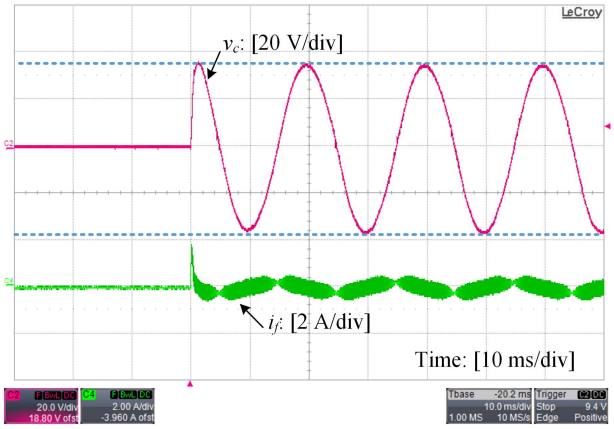
This paper proposes a design method of single-voltage-loop for low LC-resonant-frequency VSCs. By using a negative proportional gain in the PR voltage controller, it is found that the stability design region of LC-filters is $\omega_r<\omega_s/3$, thus low LC-resonant-frequency VSCs can be stable. Furthermore, in order to improve system dynamic performance, a closed-loop zeros configuration based voltage control method is proposed. According to this control method, the dynamic performance can be designed independently without affecting system stability.

Acknowledgment

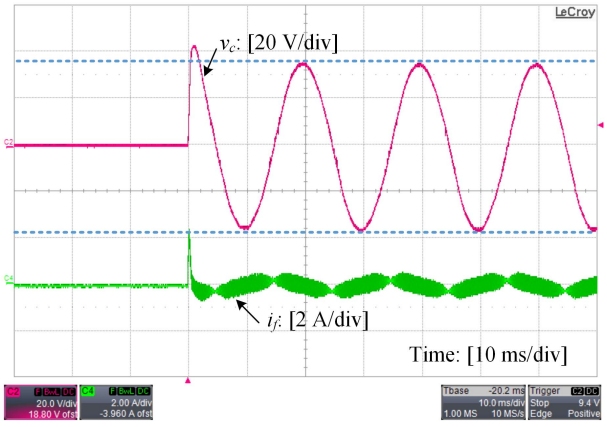
This research was supported by the National Research Foundation, Prime Minister's Office, Singapore under the Energy Programme and administrated by the Energy Market Authority (EP Award No. NRF2015EWT-EIRP002-007).



(a)



(b)



(c)

Fig. 9. Step response with the proposed control method. (a) m=-0.2. (b) m=-0.5. (c) m=-0.7.

References

[1] J. M. Guerrero, L. Hang, and J. Uceda, "Control of distributed uninterruptible power supply systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2845–2859, Aug. 2008.

[2] P. C. Loh, M. J. Newman, D. N. Zmood, and D. G. Holmes, "A comparative analysis of multi-loop voltage regulation strategies for single

and three-phase UPS systems," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1176–1185, Sep. 2003.

[3] Z. Li, Y. Li, P. Wang, H. Zhu, C. Liu, and F. Gao, "Single-loop digital control of high-power 400-Hz ground power unit for airplanes," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 532–543, Feb. 2010.

[4] Y. Li, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Investigation and improvement of transient response of DVR at medium voltage level," *IEEE Trans. Ind. Appl.*, vol. 43, no. 5, pp. 1309-1319, Sep./Oct. 2007.

[5] P. C. Loh, and D. G. Holmes, "Analysis of multiloop control strategies for *LC*/*CL*/*LCL*-filtered voltage-source and current-source inverters," *IEEE Trans. Ind. Appl.*, vol. 41, no. 2, pp. 644-654, Mar./Apr. 2005.

[6] J. He, and Y. Li, "Generalized closed-loop control schemes with embedded virtual impedances for voltage source converters with *LC* or *LCL* filters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1850–1861, Apr. 2012.

[7] Y. Geng, Y. Yun, R. Chen, K. Wang, H. Bai, and X. Wu, "Parameters design and optimization for *LC*-type off-grid inverters with inductor-current feedback active damping," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 703–715, Jan. 2018.

[8] X. Wang, P. C. Loh, and F. Blaabjerg, "Stability analysis and controller synthesis for single-loop voltage-controlled VSIs," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7394–7404, Sep. 2017.

[9] X. Li, X. Wu, Y. Geng, X. Yuan, C. Xia, and X. Zhang, "Wide damping region for *LCL*-type grid-connected inverter with an improved capacitor-current-feedback method," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5247-5259, Sep. 2015.

[10] Y. Zhang, J. Liu, Z. Dong, H. Wang, and Y. Liu, "Dynamic performance improvement of diode-capacitor-based high step-up DC-DC converter through right-half-plane zero elimination," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6532-6543, Aug. 2017.