Analysis of Gate Signal Interference in an Integrated SiC MOSFET Module

Zezheng Dong, Xinke Wu, Kuang Sheng
College of Electrical Engineering
Zhejiang University
Hangzhou, China
wuxinke@zju.edu.cn

***Abstract*—A silicon carbide MOSFET half-bridge module is fabricated with 1200V devices from wolfspeed. The gate drivers and the decoupling capacitors are integrated in this module. The layout of the direct bonded copper (DBC) board is designed to minimize stray inductance and module size. The gate signal interference occurring during the double pulse test (DPT) is analyzed in detail with an analytical model. Experiments are done to verify this analytical model, and impact of the gate signal interference is discussed to offer better guidance for the design of the integrated power module. Solutions are also provided to eliminate the gate signal interference.**

Keywords—silicon carbide MOSFET; integrated gate driver; gate signal interference

I. INTRODUCTION

Wide bandgap devices such as silicon carbide (SiC) MOSFETs are becoming more and more attractive in high voltage [1, 2] and high frequency applications [3, 4]. Due to superior material properties, the ideal specific conduction resistance ($R_{on,sp}$) of a SiC unipolar device can be much smaller than that of its silicon counterpart, so die size shrinks. Smaller die size leads to lower capacitance and higher switching speed [5]. Volume of power electronics systems can be reduced significantly by increasing the switching frequency [6].

Fast switching speed means higher *di/dt* and *dv/dt* in the circuit, which induces new problems for the application of SiC MOSFETs [7, 8]. Parasitic inductances existing in the power loop and gate driving loop are critical limitation for fast switching of SiC MOSFETs. Voltage overshoot and oscillation become more serious in the converters with high parasitic inductance. Conventional implementations of SiC based applications using discrete devices usually bear these problems. So integrated SiC modules with low parasitic inductance are needed in high frequency switching situation. As shown in Fig.1, a SiC power MOSFET half-bridge module is designed and fabricated with gate drivers and bypassing ceramic capacitors integrated on the direct bonded copper (DBC) board. This integration minimizes the power loop inductance and gate driving inductance from several tens of nanohenries to less than 10 nanohenries. At the same time, volume of the module shrinks when compared to discrete devices.

After fabrication, double pulse test is applied to the module. During the test, gate signal interference is observed, which is mentioned briefly in [4]. In this paper, an analytical model is established to analyze this phenomenon more precisely and discussions of the gate signal interference are done. Also, solutions to mitigate the interference are proposed. This paper offers a guidance for the design of integrated power module consisting of gate drivers.

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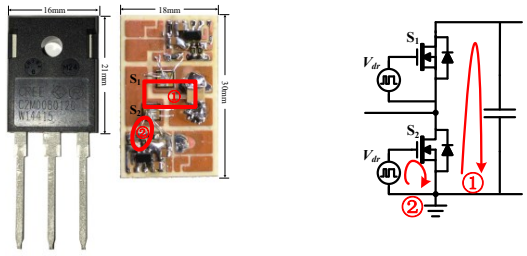
II. FABRICATION OF THE SIC MOSFET HALF BRIDGE MODULE

A. Design and Fabrication of the Integrated Power Module

As analyzed before, to fully utilize SiC MOSFETs' advantages, the impact of the circuit parasitic should be minimized. So a SiC MOSFET integrated power module (IPM) is carefully designed and fabricated, as shown in Fig. 1(a).

Two SiC MOSFETs from Wolfspeed are soldered onto a DBC board (30mm×18mm) of 0.38mm thick Al_2O_3 ceramic and 0.2mm thick copper. Specifications of the integrated power module (IPM) are listed in Table I. Two 1200V/15nF decoupling capacitors with 1206 package are placed as close as possible to the chips of the half bridge module, minimizing the power loop inductance to only 6.5nH. The module also has two



(a) (b)

Fig. 1. (a) Comparison of the SiC MOSFET with TO-247 package and the SiC MOSFET IPM (b) Power loop and gate driving loop illustration

TABLE I. SPECIFICATIONS OF THE IPM

Parameters	Value
Rated Voltage/Current	1200V/20A
SiC MOSFET	CPM2-1200-0080B
Bypassing Capacitors (on board)	1200V/15nF(×2)
Signal Isolation	Si8233
Gate Driver IC	UCC27531

gate driver IC UCC27531 [9] with small packaging of SOT-23 integrated on the DBC board. A turn on gate resistor R_{g_on} together with a turn off resistor R_{g_off} are also mounted on the module for adjustment of the switching speed. Though with the external resistance, parasitic inductance of the driving loop is reduced to less than 9nH. Si8233 is selected for the signal isolation of the IPM. Two auxiliary power supplies QA01C from MORNSUN provide +20V/-4V for the gate driver ICs.

B. *Gate Signal Interference of the Integrated Module*

Double pulse test (DPT) is conducted on the module. Fig.2 (a) shows the equivalent circuit of the test set-up, and Fig.2 (b) gives the prototype of the test circuit. But when the test voltage and voltage switching speed rises, interference occurs on the gate-source voltage v_{gs} and drain-source voltage v_{ds}, as shown in Fig.2 (c). This interference reduces the reliability of the module and should be eliminated or mitigated. Due to the integration of gate drivers, the high dv/dt induced by the switching SiC MOSFETs interferes the input pin of the gate drivers through parasitic capacitance of DBC board.

III. Analysis of the Gate Signal Interference and Experiment Verification

A. *Analysis of the Gate Signal Interference*

Overview of the IPM and its corresponding circuit diagram are shown together in Fig. 3(a). The input pin structure inside the driver IC consists a capacitor C_{in} about 20pF and a pull-down resistor R_0 about 500kΩ. R_s represents the resistance that should be placed in series to the input pin of the driver IC according to the manufactory. The red capacitances in the circuit indicates the parasitic capacitances existing between the top and bottom pads of the DBC board. v_H is the voltage of the neutral point of the half bridge and v_n is the voltage change of bottom pad on DBC board. C_p is the parasitic capacitance beneath the pad of the input IC pin and v_{in} is the actual voltage applied on the input IC pin. V_{th_h} and V_{th_l} represent the high threshold voltage and high threshold voltage of the input IC pin.

Fig. 3(b) gives the waveforms timing sequence of the device under test (DUT). The interference is related to the driving loop of the DUT, which is picked out to in Fig. 4(a). The step-down pulse signal v_{pulse} comes to the input pin of the gate driver firstly. After a short time delay, the output of the driver steps down and turns off the SiC MOSFET. v_H rises, inducing a voltage change v_n on the bottom pad of the DBC board. Similarly v_n induces a voltage rises v_{in} on the input pin of the gate driver IC through C_p. R_0 shows high impedance in this transient process, so Fig.4 (a) is simplified as Fig.4 (b). Usually v_n is much larger than v_{in}, then v_n can be treated as a voltage source during this transient process, which draws a simple analytical model in Fig.4 (c). Equation (1) can be concluded here from this analytical model:

$$v_{in} = C_p \cdot \sigma \cdot R_s (1 - e^{-t/R_s C_{in}}) \tag{1}$$

Where σ represents dv_n/dt.

The maximum input interference voltage v_{in_max} can be derived as:

$$v_{in\_max} = C_p \cdot \sigma \cdot R_s (1 - e^{-v_{n\_max}/(\sigma R_s C_{in})}) \tag{2}$$

Where v_{n_max} is the maximum voltage rise of the bottom copper pad of DBC board. Once the v_{in_max} reaches the input

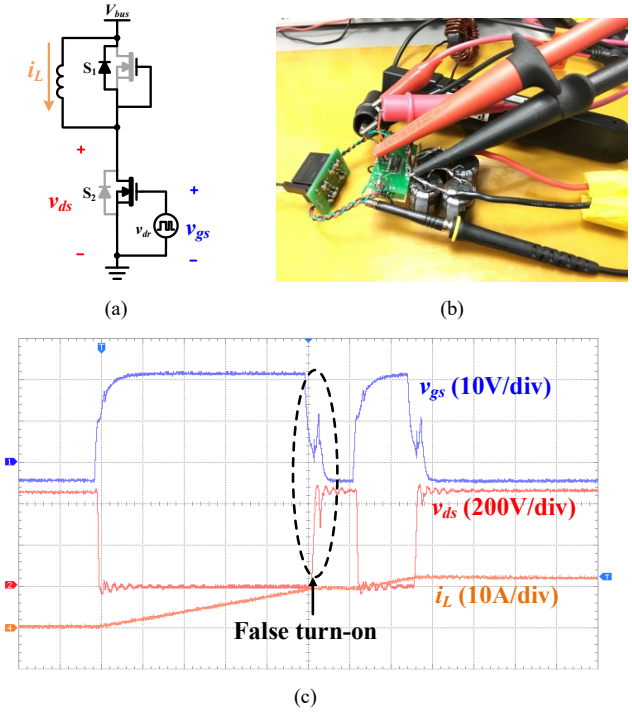


Fig. 2. Gate signal interference during double pulse test: (a) equivalent circuit (b) prototype of the test circuit (c) waveforms of the double pulse test.

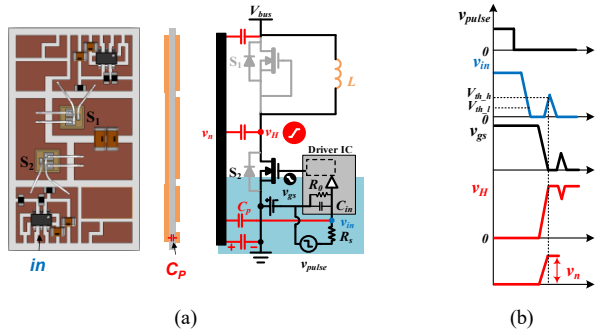


Fig. 3. (a) Overview of the IPM and corresponding circuit (b) Interference waveforms time sequence during turn off transient

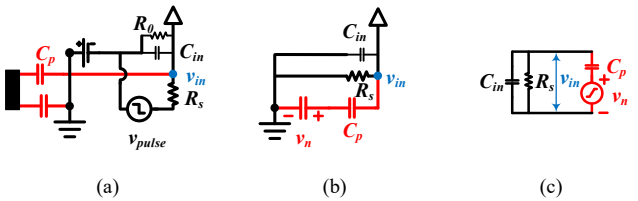


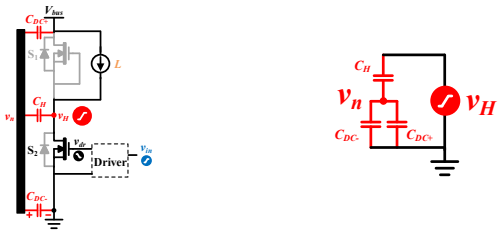
Fig. 4. Analytical model of the gate signal interference

high threshold voltage V_{th_h}, the driver's output will step up to turn on the SiC MOSFET falsely.

B. *Experiment Verification of the Analytical Model*

The bottom pad of DBC board is floating and it is difficult to measure the voltage change v_n because the parasitic capacitance is comparable to the probe. So it's reasonable to derive v_n through v_H and the parasitic capacitance, the equivalent circuit of which is illustrated in Fig. 5.

As shown in Fig.5 (a), the parasitic capacitance of the DBC board is mainly categorized into three part. C_H is the capacitance between the bottom copper layer and the neutral point pad on the top copper layer of DBC, and C_{DC+} is between the bottom copper layer and the positive point pad on the top copper layer. C_{DC-} is similar to C_{DC+}. Then v_n can be derived by dividing the voltage change of v_H during the interference



(a) (b)

Fig. 5. Equivalent circuit to derive v_n

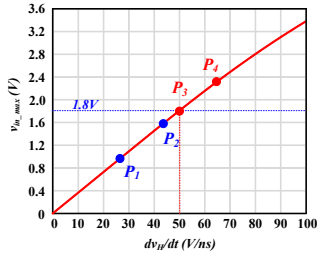
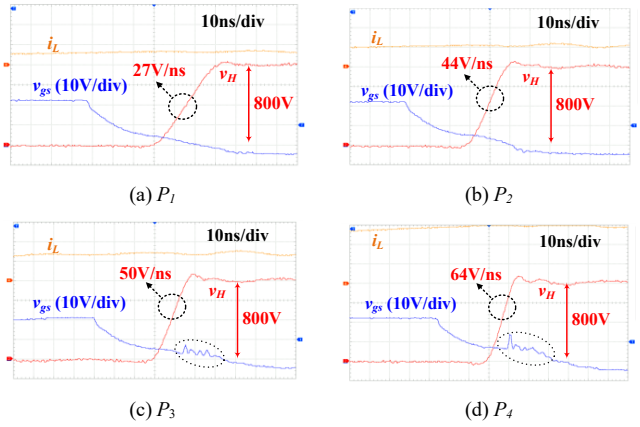


Fig. 6. The maximun input signal interference verses device switching speed under 800V bus voltage



(a) P_1 (b) P_2

(c) P_3 (d) P_4

Fig. 7. Verification waveforms under different switching speed

transition, namely (3).

$$v_n = C_H \cdot v_H / \left(C_{DC+} + C_{DC-} + C_H\right) = \lambda \cdot v_H \tag{3}$$

Substituting (3) into (2), (4) is derived

$$v_{in\_max} = C_p \cdot \lambda \cdot \sigma' \cdot R_s \left(1 - e^{-v_{H\_max}/(\sigma' R_s C_{in})}\right) \tag{4}$$

Here, σ' represents dv_H/dt, which can be directly observed on the oscilloscope.

Fig.6 plots v_{in_max} versus dv_H/dt under 800V bus voltage V_{bus}. Here. C_p is about 0.57pF and λ is about 0.425 according to simulation. R_s is chosen as 150Ω to meet the minimum requirement of the driver IC UCC27531 on the datasheet. It can be seen that the maximum gate signal interference voltage v_{in_max} on the input pin of the driver IC increases with the increasing switching speed of SiC MOSFET. When the rising speed of v_H reaches beyond about 50V/ns, the interference v_{in_max} on the input pin of the driver IC will reach the high threshold voltage V_{th_h}(which is 1.8V~2.2V here for UCC27531).

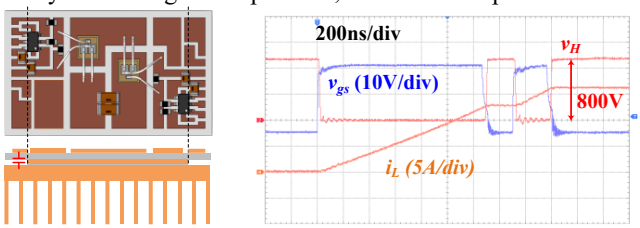
In order to verify this analytical model, DPT with different switching speed is done. Instead of capturing the voltage signal of the input pin of driver IC, the gate-to-source voltage v_{gs} of the DUT is observed because it is difficult to measure the voltage of v_{in} since the internal capacitance C_{in} is only 20pF, which is comparable to the measuring probe.

Four different switching speed is chosen, as marked P_1~P_4 in Fig.6. Fig. 7 shows the experiment waveforms of the four marked point. From Fig. 7(a) and (b), when the switching speed is lower than 50V/ns, no signal interference is observed. While from Fig. 7(c) and (d), when the switching speed is beyond 50V/ns, obvious interference occurs on the v_{gs} waveform (as shown in the dot line circle). And when the switching speed is higher (from 50V/ns to 64V/ns), the interference becomes more serious. This interference limits the improvement of the switching speed of SiC MOSFET, which cannot be ignored when the gate driver is integrated and the switching speed is extremely high.

C. *Solutions to mitigate the gate signal interference*

This gate signal interference occurs on the input pin of the driver IC. According to the analytical model in Fig. 4(c), the interference can be mitigated either by decreasing the impedance in the circuit loop or by minimizing the interference source.

By decreasing the impedance, an external capacitor can be



(a) (b)

Fig. 8. Gate signal interference mitigation by minimizing C_p

paralleled beside C_{in}. The resistance of R_s can also be minimized, but it should meet the requirement of the driver IC.

By minimizing the interference source, actually it is impossible to eliminate the voltage change v_n. But from Fig. 4(c), the parasitic capacitance C_p can reduced. The DBC has been carefully design to achieve only 0.57pF for C_p, and the pad under the input pin of driver IC cannot be further minimized since it will be impossible for soldering. Alternatively, the edge of the bottom pad can be adjust to eliminate the corresponding part beneath the input pin pad. Then when the DBC board is attached to the baseplate or heatsink, the parasitic capacitance can be greatly reduced. In Fig. 8(a), with 0.3mm (0.2mm for the bottom pad thickness and 0.1mm for the solder thickness) extra distance, C_p is reduced from 0.57pF to 0.15pF. Fig. 8(b) shows the DPT waveforms under 800V/13A. The switching speed is beyond 50V/ns, and no more gate interference is observed.

IV. CONCLUSIONS

In this paper, a SiC MOSFET power module with integrated gate drivers are designed, fabricated. The gate signal interference at the input pin of the gate drivers are analyzed in detail with a reasonable analytical model and discussions are done about the gate signal interference. Solutions are proposed according to the model to mitigate this interference, and experiment result shows evident improvement of the double pulse test. This paper offers a guidance for the design of integrated power module consisting of gate drivers.

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