A Single-Stage Bidirectional Dual-Active-Bridge AC-DC Converter Based on Enhancement Mode GaN Power Transistor

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***Abstract*—This paper presents a high step-down ratio single-stage AC-DC converter based on GaN HEMT and dual-active-bridge (DAB) topology. The dual-phase-shift (DPS) modulation and variable-frequency (VF) modulation control strategy are adopted to realize zero voltage switching (ZVS) over wide input voltage range and load conditions. Compared with conventional two-stage AC-DC converter, the elimination of DC link capacitor, protective relay and single power conversion stage enables a high efficiency and higher power density solution for energy storage applications. In addition, ZVS range of both buck and boost mode is fully analyzed in this paper. A 240 V_{rms} AC-48V DC, 80-250 kHz prototype was developed to verify the novel converter.**

***Keywords*—Dual-active-bridge (DAB); Zero-Voltage-Switching (ZVS); Power-Factor-Correction (PFC); Dual Phase Shift (DPS); Variable Frequency (VF)**

I. Introduction

Due to increasing penetration of residential solar energy systems, energy storage system (ESS) has been introduced to maximize the usage of renewable energy. The battery energy storage system (BESS) is widely used compare to the flywheel and compressed air because of its faster real and reactive power dispatch capability which can be used for various application such as voltage support and frequency response[1], as well as and peak shaving applications.

The conventional power converter used in BESS employs a two-stage structure, a PFC rectifier/inverter followed by an bidirectional isolated DC-DC converter[1]. For conventional two-stage AC-DC converter, large DC-link capacitor is inevitable to maintain a stable DC voltage[1][2]. The first stage is typically a hard switched CCM boost converter which limits the frequency range, therefore, achieving high power density and high efficiency is challenging. Single stage topology has been proposed [2] to address these challenges.

Reference[3][4][5][6] pointed out the well know DAB topology can be used as a single-stage AC-DC converter with full range ZVS operation and bidirectional power flow.

For a AC-half-bridge DC-full-bridge DAB topology, the leakage inductance could be disconnected from the input during the start up or fault protection, this eliminates potentially the need for additional protective relay. This paper proposes a half bridge based AC-DC topology as shown in Fig.1. Two GaN FETs are used to form a AC switch. A snubber C_{db} is introduced which can provide a current path for the current in the leakage inductance L_σ so no voltage overshoot present in the circuit. 650V GaN FET is used on the high voltage side and 80V eGaN FET are used in the low voltage side. The control objective is to have power factor correction (PFC) on the input side while maintain full ZVS operation for all GaN transistors. Section II introduces the dual-phase-shift control to realize zero-voltage-switching. Section III states variable frequency to realize power factor correction with zero-crossing improvement. In section IV, the simulation result verifies the control, and a hardware prototype is introduced to verify the converter. Section V concludes the paper with future work.

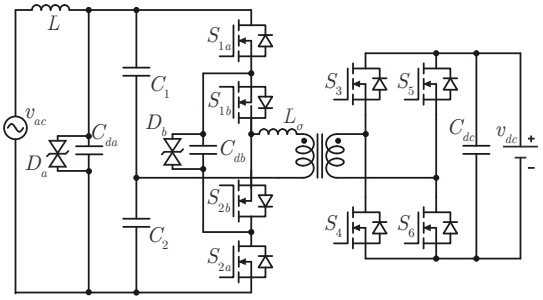


Fig. 1. Proposed DAB Topology

II. Dual-Phase-Shift Control Modulation

A dual active bridge control could utilize both single phase shift (SPS) and DPS to realize ZVS. Though both control modulations could realize ZVS, different control modulation would lead to different Root-Mean-Square (RMS) current, turn-off current and eventually, different loss.

Since SPS could be included in DPS, this section would only present DPS in buck (where $1/2|v_{ac}| > nv_{dc}$) and boost (where $1/2|v_{ac}| < nv_{dc}$) mode in AC-DC and DC-AC operation with its ZVS constrains.

A. Dual-Phase-Shift Modulation in AC-DC Operation and Its ZVS Constrains

The leakage inductance current of transformer in DPS modulation is stated in (1).

$$i_{L\sigma}(t)=\begin{cases}\frac{\frac{|v_{ac}|}{2}+nv_{dc}}{L_\sigma}(t-t_0)+i_{L\sigma}(t_0) & t_0<t<t_1\\ \frac{\frac{|v_{ac}|}{2}}{L_\sigma}(t-t_1)+i_{L\sigma}(t_0) & t_1<t<t_2\\ \frac{\frac{|v_{ac}|}{2}-nv_{dc}}{L_\sigma}(t-t_2)+i_{L\sigma}(t_0) & t_2<t<t_3\\ -\frac{\frac{|v_{ac}|}{2}-nv_{dc}}{L_\sigma}(t-t_3)+i_{L\sigma}(t_0) & t_3<t<t_4\\ -\frac{\frac{|v_{ac}|}{2}}{L_\sigma}(t-t_4)+i_{L\sigma}(t_0) & t_4<t<t_5\\ -\frac{\frac{|v_{ac}|}{2}+nv_{dc}}{L_\sigma}(t-t_5)+i_{L\sigma}(t_0) & t_5<t<t_6\end{cases} \tag{1}$$

Where

$$\begin{aligned}
i_{L\sigma}(t_0)&=-\frac{\frac{1}{4}|v_{ac}|+n(\theta_{5,6}-\theta_{3,4})v_{dc}}{2f_sL_\sigma}\\
i_{L\sigma}(t_1)&=\frac{(\theta_{5,6}-\frac{1}{4})|v_{ac}|+n(\theta_{5,6}+\theta_{3,4})v_{dc}}{2f_sL_\sigma}\\
i_{L\sigma}(t_2)&=\frac{(\frac{1}{4}-\theta_{3,4})|v_{ac}|+n(\theta_{5,6}+\theta_{3,4})v_{dc}}{2f_sL_\sigma}\\
i_{L\sigma}(t_3)&=\frac{\frac{1}{4}|v_{ac}|+n(\theta_{5,6}-\theta_{3,4})v_{dc}}{2f_sL_\sigma}\\
i_{L\sigma}(t_4)&=-\frac{(\theta_{5,6}-\frac{1}{4})|v_{ac}|+n(\theta_{5,6}+\theta_{3,4})v_{dc}}{2f_sL_\sigma}\\
i_{L\sigma}(t_5)&=-\frac{(\frac{1}{4}-\theta_{3,4})|v_{ac}|+n(\theta_{5,6}+\theta_{3,4})v_{dc}}{2f_sL_\sigma}
\end{aligned}$$

The voltage and current applied to the transformer and gate signal are drawn in Fig.2. In this DPS AC-DC control, $\theta_{3,4}$ is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of S_3 and S_4, and $\theta_{5,6}$ is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of S_5 and S_6. T_s is the time period of a single switching period.

The transferred instantaneous power in DPS modulation is given in (2).

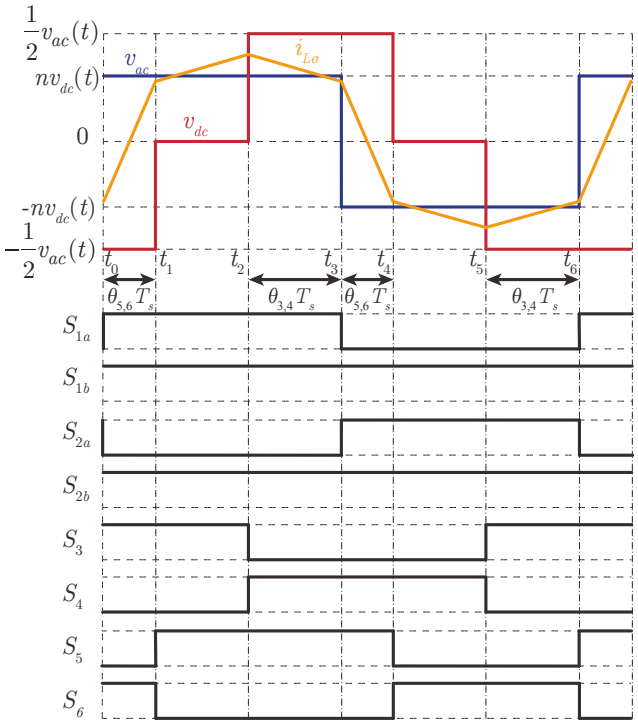
$$P(t)=\frac{n|v_{ac}(t)|v_{dc}(t)(-2\theta_{3,4}^2-2\theta_{5,6}^2+\theta_{3,4}+\theta_{5,6})}{4f_sL_\sigma} \tag{2}$$

1) Boost Mode in DPS AC-DC Operation: ZVS Analysis

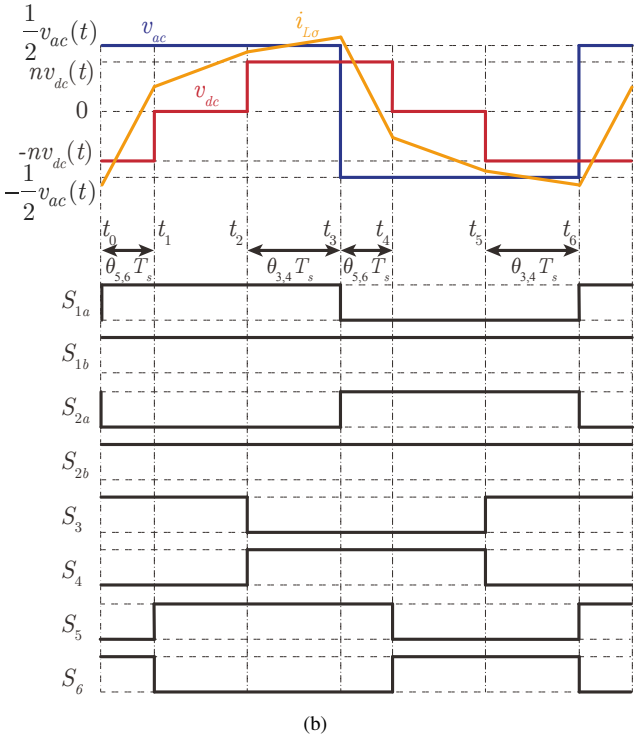
To simplify and maintain trapezoidal current shape, this paper set $i_{L_\sigma}(t_1)=i_{L_\sigma}(t_3)$, therefore the relationship of $\theta_{3,4}$ and $\theta_{5,6}$ could be derived in (3).

$$\theta_{3,4}=\frac{v_{ac}(1-2\theta_{5,6})}{4nv_{dc}} \tag{3}$$

To realize ZVS, the negative current should be large enough to discharge the Q_{oss} of transistor for both side, which would lead to (4).



(a)



(b)

Fig. 2. Dual-Phase-Shift Modulation AC-DC Operation Principle where $v_{ac}>0$ (a) In Boost Mode (b) In Buck Mode

$$\begin{aligned}
i_{L\sigma}(t_0)&\le -I_{s,ac}\\
i_{L\sigma}(t_3)&\ge I_{s,ac}\\
i_{L\sigma}(t_1)&\ge I_{s,dc}\\
i_{L\sigma}(t_2)&\ge I_{s,dc}
\end{aligned} \tag{4}$$

Where $I_{s,ac}$ indicates the minimum ZVS current for AC side transistors, and $I_{s,dc}$ indicates the minimum ZVS current for DC side transistors.

The constrain in (4) would lead to the range for $\theta_{5,6}$ in (5).

$$\theta_{5,6} \geq \theta_{5,6,min} = \frac{4f_s L_\sigma I_s}{|v_{ac}| + 2nv_{dc}} \tag{5}$$

I_s indicate the minimum communication current for transistors of both sides, which is $I_s = max(I_{s,ac}, I_{s,dc})$

2) Buck Mode in DPS AC-DC Operation: ZVS Analysis

In buck mode, $1/2|v_{ac}| > nv_{dc}$. The half-bridge full-bridge DAB circuit could not maintain trapezoidal current. Whereas ZVS could still be maintained. In buck mode, the ZVS condition could be included in (6).

$$\begin{aligned} i_{L\sigma}(t_0) &\leq -I_{s,ac} \\ i_{L\sigma}(t_1) &\geq I_{s,dc} \end{aligned} \tag{6}$$

B. Dual-Phase-Shift Modulation in DC-AC Operation and Its ZVS Constrains

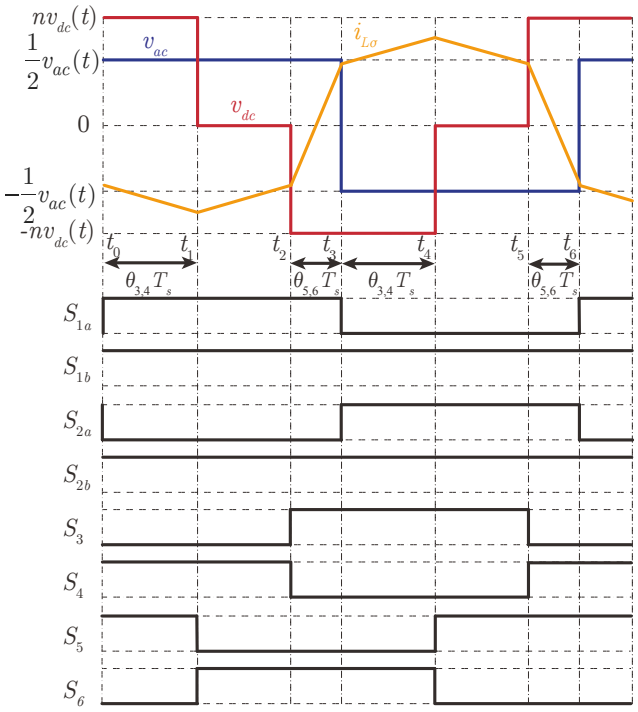
To achieve similar waveform as AC-DC operation, this section assumes (7), The leakage inductance current of transformer in DPS modulation is stated in (8).

$$\begin{aligned} \theta_{3,4,DC-AC} &= \theta_{5,6,AC-DC} \\ \theta_{5,6,DC-AC} &= \theta_{3,4,AC-DC} \end{aligned} \tag{7}$$

$$i_{L\sigma}(t) = \begin{cases} \frac{\frac{|v_{ac}|}{2} - nv_{dc}}{L_\sigma}(t-t_0) + i_{L\sigma}(t_0) & t_0 < t < t_1 \\ \frac{\frac{|v_{ac}|}{2}}{L_\sigma}(t-t_1) + i_{L\sigma}(t_0) & t_1 < t < t_2 \\ \frac{\frac{|v_{ac}|}{2} + nv_{dc}}{L_\sigma}(t-t_2) + i_{L\sigma}(t_0) & t_2 < t < t_3 \\ \frac{\frac{-|v_{ac}|}{2} + nv_{dc}}{L_\sigma}(t-t_3) + i_{L\sigma}(t_0) & t_3 < t < t_4 \\ -\frac{\frac{|v_{ac}|}{2}}{L_\sigma}(t-t_4) + i_{L\sigma}(t_0) & t_4 < t < t_5 \\ -\frac{\frac{|v_{ac}|}{2} + nv_{dc}}{L_\sigma}(t-t_5) + i_{L\sigma}(t_0) & t_5 < t < t_6 \end{cases} \tag{8}$$

Where

$$\begin{aligned} i_{L\sigma}(t_0) &= -\frac{\frac{1}{4}|v_{ac}| + n(\theta_{5,6} - \theta_{3,4})v_{dc}}{2f_s L_\sigma} \\ i_{L\sigma}(t_1) &= -\frac{(\frac{1}{4} - \theta_{3,4})|v_{ac}| + n(\theta_{5,6} + \theta_{3,4})v_{dc}}{2f_s L_\sigma} \\ i_{L\sigma}(t_2) &= -\frac{(\theta_{5,6} - \frac{1}{4})|v_{ac}| + n(\theta_{5,6} + \theta_{3,4})v_{dc}}{2f_s L_\sigma} \\ i_{L\sigma}(t_3) &= \frac{\frac{1}{4}|v_{ac}| + n(\theta_{5,6} - \theta_{3,4})v_{dc}}{2f_s L_\sigma} \\ i_{L\sigma}(t_4) &= \frac{(\frac{1}{4} - \theta_{3,4})|v_{ac}| + n(\theta_{5,6} + \theta_{3,4})v_{dc}}{2f_s L_\sigma} \\ i_{L\sigma}(t_5) &= \frac{(\theta_{5,6} - \frac{1}{4})|v_{ac}| + n(\theta_{5,6} + \theta_{3,4})v_{dc}}{2f_s L_\sigma} \end{aligned}$$



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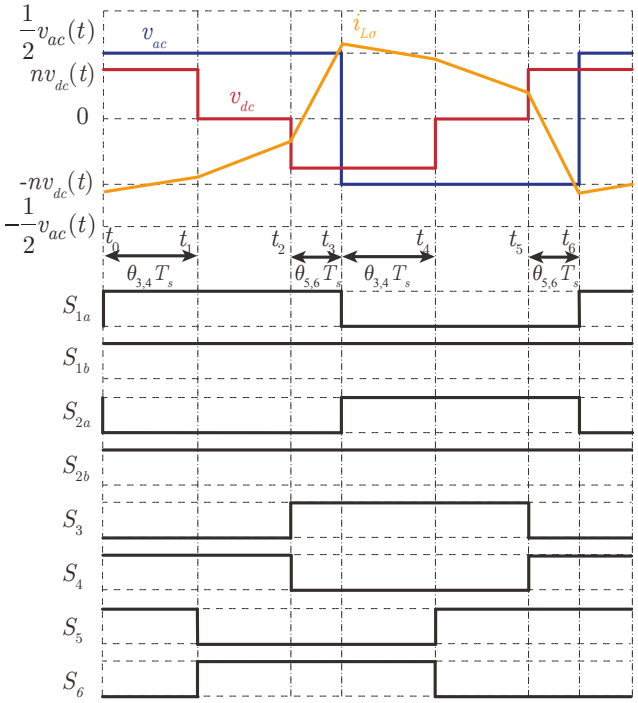
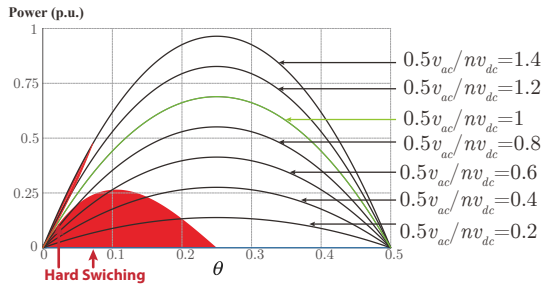


(b)

Fig. 3. Dual-Phase-Shift Modulation DC-AC Operation Principle where $v_{ac} > 0$ (a) In Boost Mode (b) In Buck Mode

The voltage and current applied to the transformer and gate signal are presented in Fig.3. In this DPS control, with the relationship of $\theta_{3,4}$ and $\theta_{5,6}$ in AC-DC and DC-AC mode included in (7), $\theta_{3,4}$ is the phase shift percentage (from 0 to



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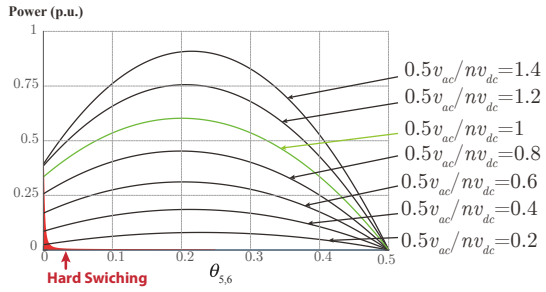


(b)

Fig. 4. Phase Shift Ratio $\theta_{3,4}$, $\theta_{5,6}$ and Switching Frequency f_s over Half Line Period for (a) Single Phase Shift; (b) Dual Phase Shift.

1) between the primary bridge and bridge leg of S_5 and S_6 in DC-AC mode, and $\theta_{5,6}$ is the phase shift percentage (from 0 to 1) between the primary bridge and bridge leg of S_3 and S_4 in DC-AC mode. T_s is still the time period of a single switching period.

The absolute transferred instantaneous power in DPS modulation still not change in DC-AC modulation besides the power transfer direction. $P_{DC-AC}(t) = -P_{AC-DC}(t)$, or as shown in (9).

$$P_{DC-AC}(t) = -\frac{n|v_{ac}(t)|v_{dc}(t)(-2\theta_{3,4}^2 - 2\theta_{5,6}^2 + \theta_{3,4} + \theta_{5,6})}{4f_s L_\sigma} \tag{9}$$

C. ZVS Range Comparison of SPS and DPS

[7] indicates the ZVS range of θ in single-phase-shift control and $\theta_{5,6}$ in dual-phase-shift control, which is independent from switching frequency f_s.

As a conventional control of DAB, SPS could be considered as a special circumstance of DPS where $\theta_{3,4}+\theta_{5,6} = 0.5$. Different from [7] which only analyzes boost mode, this paper analyses both boost and buck mode which is included in Fig.4. When phase shift ratio is larger than 0.25, there would be large circulating current, ideal choice of θ is smaller than 0.25[7]. From comparison of Fig.4, the red area indicates hard switching, and therefore, the ZVS range of dual-phase-shift is larger than single-phase-shift.

III. Variable Frequency Modulation

The transferred instantaneous power in DPS modulation is given in (2), and the instantaneous power required to achieve

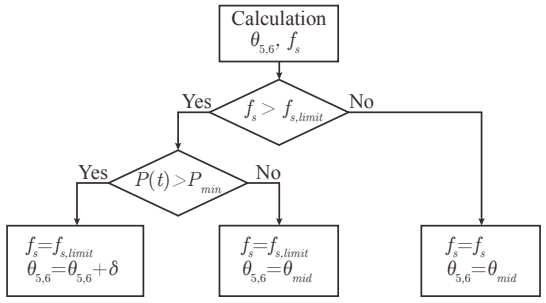


Fig. 5. Flow Chart of Proposed Control.

PFC is given in (10).

$$P_{PFC}(t) = V_{ac}I_{ac}sin^2(\omega t) - \frac{\omega(C_1+C_2)}{4}sin(\omega t)cos(\omega t) \tag{10}$$

To achieve PFC, simply make $P(t) = P_{PFC}(t)$, which could derive the value of switching frequency f_s in (11).

$$f_s = \frac{n|v_{ac}(t)|v_{dc}(t)(-2\theta_{3,4}^2 - 2\theta_{5,6}^2 + \theta_{3,4} + \theta_{5,6})}{4P_{PFC}(t)L_\sigma} \tag{11}$$

Reference [8] indicate a choice of $\theta_{5,6}$ could be set whereas achieves medium power between maximum and minimum instantaneous power given a certain frequency. The minimum power could be achieved by (4) and (6), and maximum could be achieved by setting the derivative with respect to $\theta_{5,6}$ to zero. The expression could be derived in (12).[8]

$$\theta_{5,6,mid} = \frac{\alpha|v_{ac}|^3 + (\alpha n v_{ac} + \beta)v_{ac}^2 + 4\alpha n^3 v_{dc}^3 + 4\beta n^2 v_{dc}^2}{4(v_{ac}^2 + 4n^2v_{dc}^2)(|v_{ac}| + 2nv_dc)} \tag{12}$$

Where

$$\alpha = 2 - \sqrt{2}$$
$$\beta = 8\sqrt{2}f_s L_\sigma I_s$$

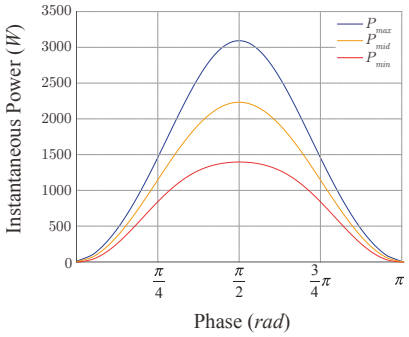
According to (11), it is obvious that for a relatively low P_{PFC}, f_s could be rather high. In practical, an upper limitation of f_s is reasonable since hardware could not stand an ultra-high switching frequency. Since the requirement of power factor is fulfilled by switching frequency, it could not be achieved whereas f_s is beyond frequency limitation in (11).

In zero-crossing period, in order to limit the sudden change of instantaneous power. This control method flow chart is shown in Fig.5, and the final result is shown in Fig.6.

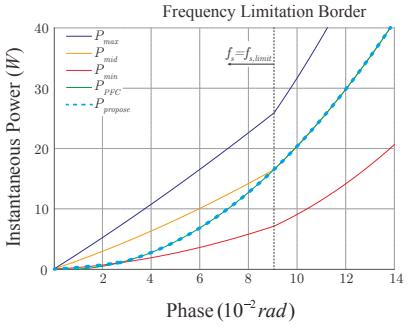
Fig.7 shows the frequency and phase shift change during half line period. Frequency upper limitation is set to be $250kHz$ in both theoretical analysis, simulation and hardware prototype. Phase shift ratio $\theta_{3,4}$ and $\theta_{5,6}$ is fulfilled by the requirement of (4) and (6) that guarantee ZVS during whole line period.

IV. Simulation Results and Experimental Verification

The proposed variable-frequency dual-phase-shift control method is simulated in Matlab/Simulink. With input voltage



(a)



(b)

Fig. 6. Instantaneous Power Transfer for $\theta_{5,6,min}$, $\theta_{5,6,mid}$ and $\theta_{5,6,max}$ (a) In Half Line Frequency; (b) In Zerp-Crossing Period.

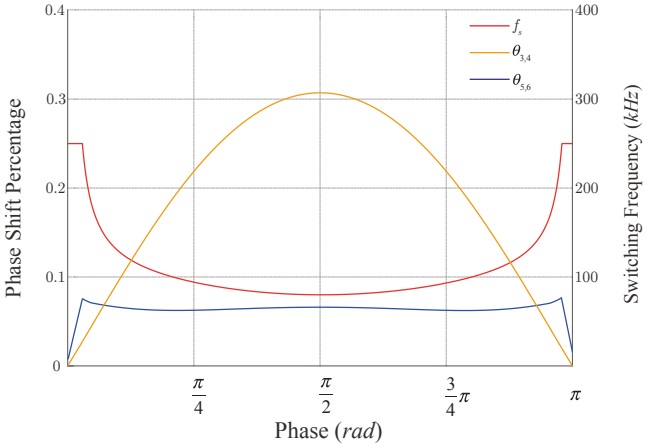
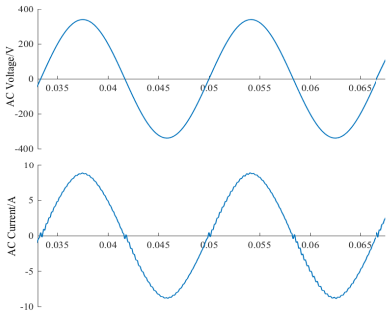


Fig. 7. Phase Shift Ratio $\theta_{3,4}$, $\theta_{5,6}$ and Switching Frequency f_s during Half Line Frequency.

of $240\,V_{rms}$ AC and output of $48V$ DC, Result is shown in Fig.8 for $1kW$ operation. Fig.8a shows its PFC performance with unity power factor, Fig.8b shows the transformer AC, DC side voltage and transformer current, with Fig.8c shows the zoomed-in waveform of Fig.8b to demonstrates the operation mode in section II. Fig.9 indicates ZVS operation of transistor S_{1a}, S_{2a}, S_3 and S_5, which indicates the ZVS operation of all transistors.

Hardware prototype is shown in Fig.10. The system parameter is shown in Table I. AC high voltage enhancement mode GaN GS66516T and DC low voltage eGaN EPC2029 are used



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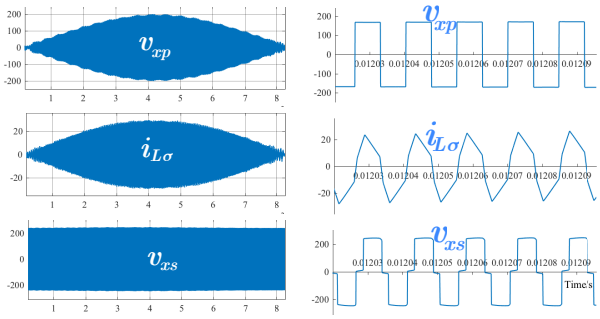
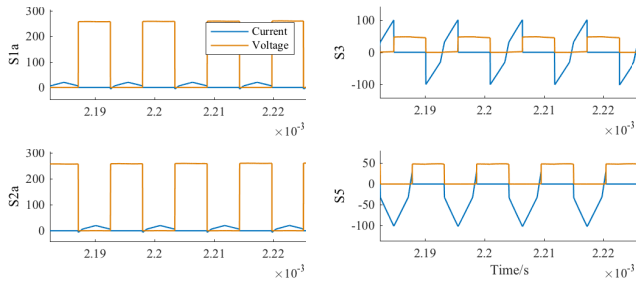


(b) (c)

Fig. 8. (a) AC Voltage and Current; (b) Transformer AC, DC Side Voltage v_{xp}, v_{xs} and Transformer Current $i_{L\sigma}$ over Half Line Period; (c) Zoomed-In Waveform of (b).



(a) (b)

Fig. 9. Voltage and Current of Switch for (a) S_{1a}, S_{2a}, and (b) S_3, S_5 indicating ZVS for All Transistors.

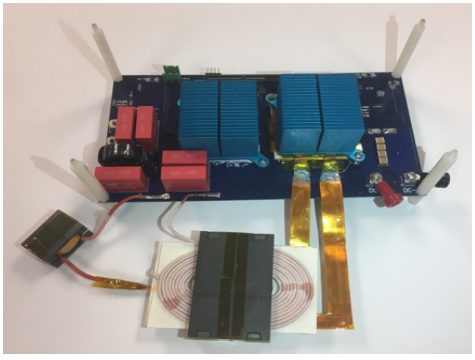
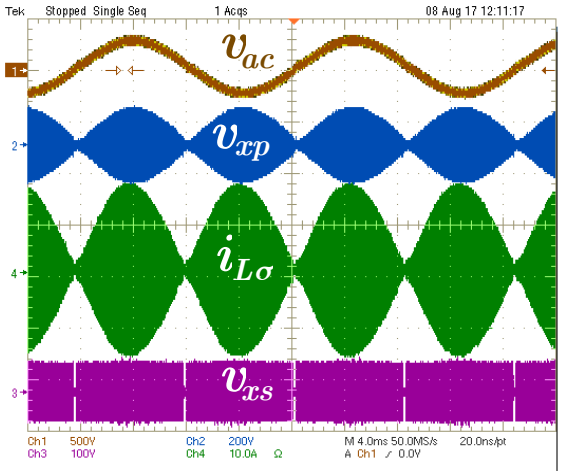


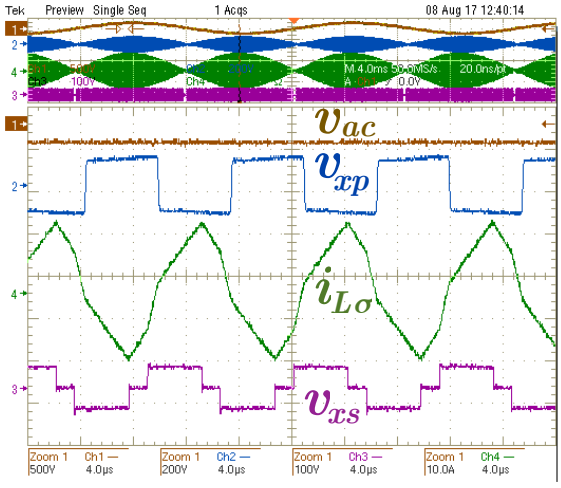
Fig. 10. Experimental Prototype.

TABLE I. SYSTEM PARAMETER OF OPERATION

Symbol	Description	Value
f_m	Grid Frequency	$60\,Hz$
f_s	Switching Frequency	$80 - 250kHz$
V_{ac}	AC Voltage	$240\,V_{rms}$
V_{dc}	DC Voltage	$48\,V$
C_1, C_2	AC Capacitor	$1.5\mu F$
C_{eq}	Switch Junction Capacitor	$130pF$
L_σ	Transformer Leakage Inductance	$10\mu H$
n	Transformer Turn Ratio	$5:1$
P	Rated Power Transfer	$1kW$



(a)



(b)

Fig. 11. (a) AC Voltage v_{ac}, Transformer Primary and Secondary Voltage v_{xp}, v_{xs} and Transformer Current $i_{L\sigma}$; (b) Zoom-In Waveform of (a).

in this converter. Fig.11a illustrates AC voltage, transformer AC and DC side voltage and transformer current. Fig.11b shows the zoomed-in waveform of Fig.11a. The voltage plateau of transformer AC and DC side voltage indicate ZVS. Fig.12 indicates the thermal performance without any fan and heat sink under half load.

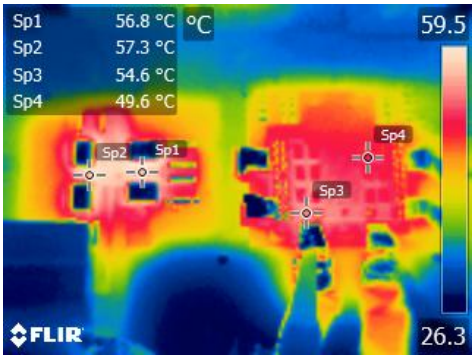


Fig. 12. Thermal Performance without Fan and Heat Sink.

V. CONCLUSION

This paper proposes a single-stage AC-DC converter based on a DAB topology. This paper fully analyses the ZVS range of dual-phase-shift control modulation in both buck and boost mode, with the comparison with single-phase-shift control. The dual-phase-shift variable-frequency control is analyzed and applied in the hardware of AC-DC converter with AC voltage of $240V_{rms}$ and DC voltage of $48V$. Theoretical analysis of control method, simulation and experimental verification is provide to verify the idea.

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