A 99.1% Efficient, 490 W/in^3 Power Density Power Factor Correction Front End Based on a 7-Level Flying Capacitor Multilevel Converter

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***Abstract*—This paper presents a power factor correction (PFC) front end based on a GaN-Based 7-level flying capacitor multilevel (FCML) boost converter. Compared to the conventional 2-level boost converter, the proposed 7-level FCML converter features the use of low-voltage-rated transistors, reduced voltage stress and high effective switching frequency on the filter inductor. These characteristics of the FCML converter lead to drastic reduction in the filter inductor size while maintaining high efficiency, and therefore significantly improve the power density of the PFC frond end compared to conventional solutions. On the other hand, the small inductance imposes challenges for the PFC control. The dynamics of the 7-level FCML converter has been analyzed and a feedforward control has been implemented to overcome these challenges. A hardware prototype is designed for universal AC input (90 VAC to 265 VAC), 400 V DC output at 1.5 kW power rating. The hardware prototype demonstrates improved efficiency and power density as well as power factor and THD performance compared to existing solutions. A peak efficiency of 99.07% and a power density of 490 W/in^3 has been experimentally verified.**

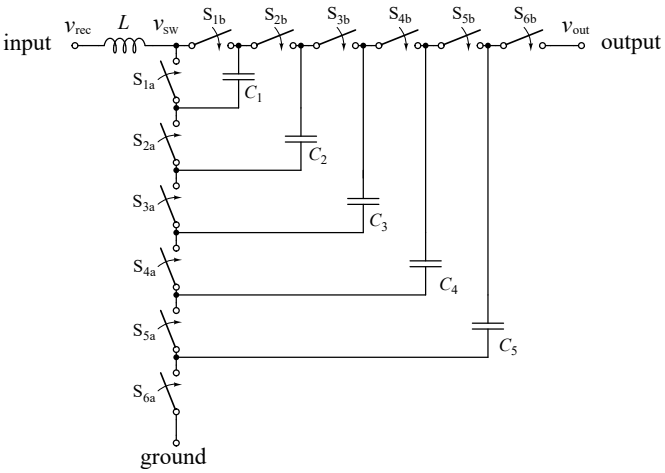

Fig. 1: Schematic drawing of a 7-level FCML boost converter.

I. Introduction

In many grid-connected single-phase AC to DC electrical systems, Power Factor Correction (PFC) is required to improve the power quality and conform to industrial standards (e.g., IEC 61000-3-2, Energy Star program, etc.). Moreover, many of these AC-DC systems are volumetrically constrained, so achieving high power density as well as high efficiency has become an important requirement.

In conventional boost converter based PFC front end designs, the size of the input inductor of the boost converter is limited by the large voltage swing amplitude and low switching frequency. Flying capacitor multilevel (FCML) converters have been conventionally used in high voltage and high power DC-AC applications [1]–[4]. It has been demonstrated recently that in several-hundred-volt, kilowatt-scale inverter applications, FCML converters also offer considerable efficiency and power density advantages compared to many conventional topologies [5]–[9]. The FCML converter in these applications features low voltage stress on transistors and high switching frequency, allowing the design to take full advantage of the recent development of high-speed GaN transistor technologies with voltage ratings around 100 V [10]. The work presented in this paper explores the use of flying capacitor multilevel (FCML) converters in PFC applications to further improve the power density and efficiency compared to state-of-the-art solutions. A 7-level FCML boost converter is developed as the PFC front end of a 1.5 kW, universal-input AC-DC rectifier system. The design allows for very high switching frequency, reduced filter inductor voltage stress and thus a significant reduction in the filter inductor size, while maintaining low switching loss and high overall efficiency. However, the input current is more sensitive to the disturbance from the input voltage because of the small inductor, imposing challenges for PFC control to achieve desired power quality. The dynamics of the 7-level FCML converter has been analyzed and a feedforward control has been implemented to overcome these challenges. The remainder of the paper is organized as follows: Section II introduces the operation of FCML converters and explains its advantages over conventional topologies in PFC applications; Section III discusses the PFC control challenges and solutions for the 7-level FCML converter; Section IV presents the implementation of the 1.5 kW hardware prototype; Section V demonstrates the performance of the hardware prototype through various experiments; finally, Section VI concludes the paper.

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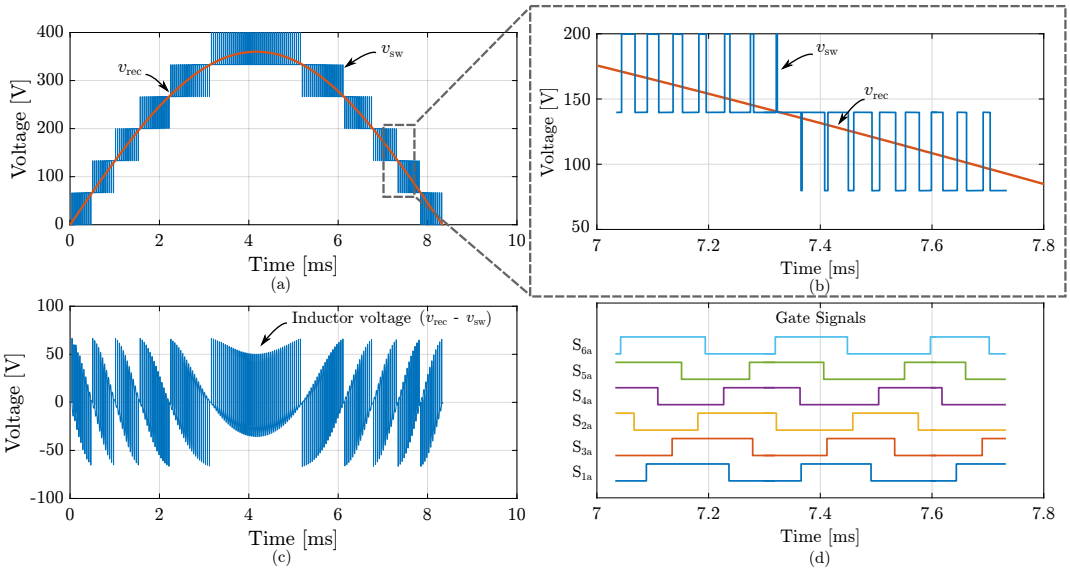


Fig. 2: (a) rectified input voltage and switching node voltage. (b) switching node voltage zoomed in. (c) inductor voltage ($v_{\text{rec}} - v_{\text{sw}}$). (d) gate signals zoomed in.

II. Flying Capacitor Multilevel Converter

For kilowatt level applications, the boost converter remains the prevalent topology for PFC front ends. However, the basic boost converter suffers from a number of shortcomings such as the large volume of the magnetic components, high voltage stress on the transistors and EMI challenges, which are exacerbated by the fast switching transition of GaN transistors [11].

The FCML topology can greatly alleviate the problems of the conventional boost topology. An in-depth comparison between these two topologies can be found in [12] and [6]. This section only briefly reviews the operation of a FCML converter to illustrate its advantages. The circuit schematic of a FCML converter is shown in Fig. 1 and the associated operation waveforms are plotted in Fig. 2.

Switch S_{1a} to S_{6a} in the FCML are controlled by a pulse width modulation (PWM) signal with a duty ratio of D (the "a" switches and "b" switches are complimentary), and is phase-shifted by $\frac{360^\circ}{N-1}$ from the adjacent PWM signals (the phase shift for a 7-level FCML is 60 degrees, as shown in Fig. 2d). In steady state, the N-level FCML boost converter naturally balances the voltages across $(N-2)$ flying capacitors, each of which holds voltage of $\frac{V_{\text{out}}}{N-1}$, $\frac{2V_{\text{out}}}{N-1}$, ..., $\frac{(N-2)V_{\text{out}}}{N-1}$ [1]. For example, in the 7-level FCML converter shown in Fig. 1, C_1 has a voltage of $\frac{V_{\text{out}}}{6}$, C_2 has a voltage of $\frac{2V_{\text{out}}}{6}$, etc. Detailed analysis of the balancing mechanism as well as practical implementation concerns can be found in [13] and [14]. As a result, the voltage stress of each switch, given by the difference between the voltages of adjacent capacitors, is reduced by a factor of $N-1$ compared to a conventional boost converter, i.e.,

$$V_{\text{switch}} = \frac{V_{\text{out}}}{N-1} \ . \tag{1}$$

The overall conversion ratio of the FCML boost converter is identical to a basic two-level boost converter as

$$V_{\text{out}} = \frac{1}{1-D} V_{\text{rec}} \ . \tag{2}$$

The exemplar switching patterns and corresponding voltage waveforms for multilevel and PFC operations in the FCML boost converter are shown in Fig .2. Since the voltage ripple seen by the inductor is reduced by a factor of six while the frequency seen by the inductor is increased by a factor of six, compared to a conventional boost converter with the same current ripple requirement, the filter inductor of the 7-level boost converter can be reduced by a factor of 36 to the first order estimation. The lower voltage transition between levels and higher effective frequency of the voltage on the switching node are also expected to help reduce the size of required EMI filters [6].

III. Control for Power Factor Correction

While the proposed 7-level FCML converter enables high efficiency and power density, its unique characteristics also introduce challenges to control its PFC operation. In this section, we discuss the PFC control, identify the challenges and propose our solution.

The full system of the PFC front end is shown in Fig. 3. The design specifications and key parameters are listed in Table I. The line voltage input v_{AC} is processed by an active full bridge rectifier commuting at line frequency to generate a rectified sine wave v_{rec}, which is then boosted by the 7-level FCML converter to a constant output voltage v_{out}. An electrolytic capacitor bank C_{buf} is added in addition to the output filter capacitor of the FCML converter to function as the twice line frequency energy buffer. If desired, more advanced active decoupling solutions [15]–[19] can be adopted to optimize the

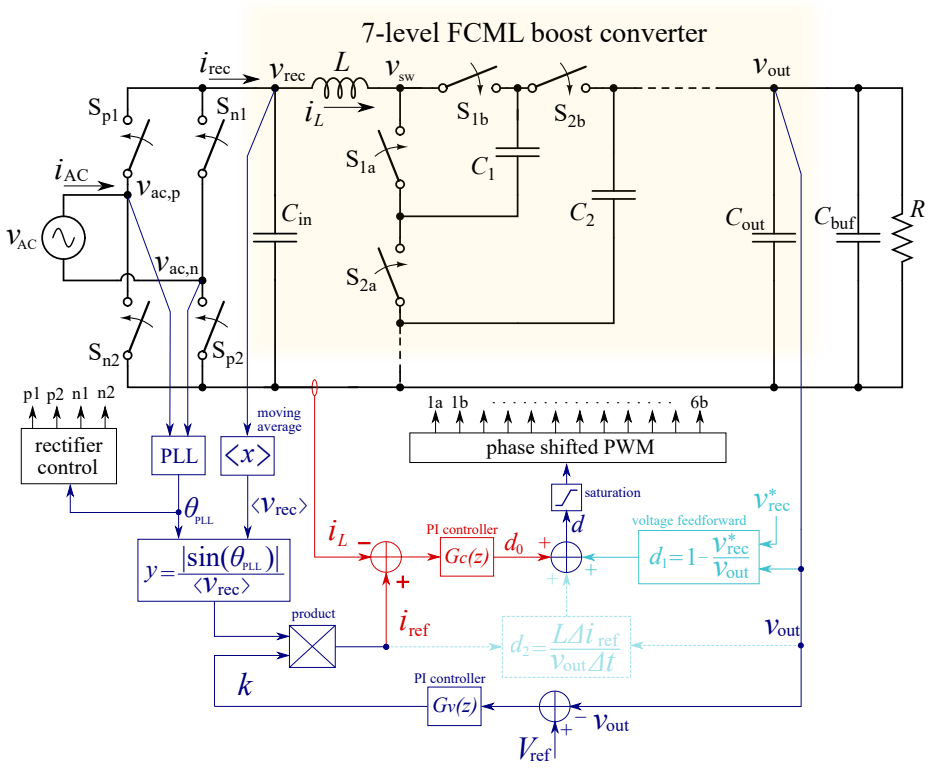


Fig. 3: Schematic drawing of the proposed PFC converter together with control diagrams implemented in a micro-controller. The control scheme consists of inner current feedback loop (red), outer voltage feedback loop (blue) and voltage feedforward (turquoise).

power density of the overall system. A PFC control scheme for boost converter operating in continuous conduction mode (CCM) similar to the classical multi-loop control [20], [21] is designed and implemented in a micro-controller as shown in Fig. 3.

A. Inner current loop

An inner current loop regulates the inductor current i_L to follow a desired current reference i_{ref} generated in phase with v_{rec}. To precisely match the phase of the input current to the input voltage and reject disturbance due to measurement noise, a phase-locked loop (PLL) based on an adaptive notch filter [22] is adopted in this design to generate the current reference.

To study the dynamics of the input current of the FCML converter, we first make the observation that the flying capacitors in this design (i.e., C_1 to C_5) are two orders of magnitude smaller than the buffer capacitor C_{buf} connected to the output. In the frequency range of interest to the PFC control (i.e., up to tens of kilohertz), the effect of the flying capacitors on the circuit dynamics can thus be ignored compared to C_{buf}. Then the dynamics of the FCML converter can be approximated by that of a boost converter. The control input to inductor current transfer function of the boost converter

$$G_{i_L d} = \frac{\tilde{i}_L}{\tilde{d}} = \frac{2V_{\text{out}}}{R(1-D)^2} \cdot \frac{1+\frac{sRC}{2}}{1+\frac{sL}{R(1-D)^2}+\frac{s^2LC}{(1-D)^2}} \quad (3)$$

Specifications	Value
Input voltage	90 Vac – 260 Vac (RMS)
Output power	1500 W
Output voltage	400 Vdc
Output voltage ripple	< 5 V
Power factor	> 0.98
Input current THD	$< 3.5\%$
Transistor switching frequency	150 kHz
Effective switching node frequency	900 kHz
Input filter inductor L	44 μH
Input filter capacitor C_{in}	0.2 μF
Output filter capacitor C_{out}	10 μF
Flying capacitors C_1 - C_5	5 μF
Twice-line-frequency buffer capacitor C_{buf}	1560 μF

TABLE I: Specifications and key component selection of the PFC converter prototype.

as well as the disturbance to inductor current transfer function

$$G_{i_L v_{\text{rec}}} = \frac{\tilde{i}_L}{\tilde{v}_{\text{rec}}} = \frac{1}{R(1-D)^2} \cdot \frac{1+sRC}{1+\frac{sL}{R(1-D)^2}+\frac{s^2LC}{(1-D)^2}} \quad (4)$$

can be applied here to analyze the FCML boost converter [23]. With a controller G_c to close the inner current feedback loop, the small signal input current can be expressed as [24]

$$\tilde{i}_L = \frac{G_c G_{i_L d}}{1+G_c G_{i_L d}} \tilde{i}_{\text{ref}} + \frac{G_{i_L v_{\text{rec}}}}{1+G_c G_{i_L d}} \tilde{v}_{\text{rec}}. \quad (5)$$

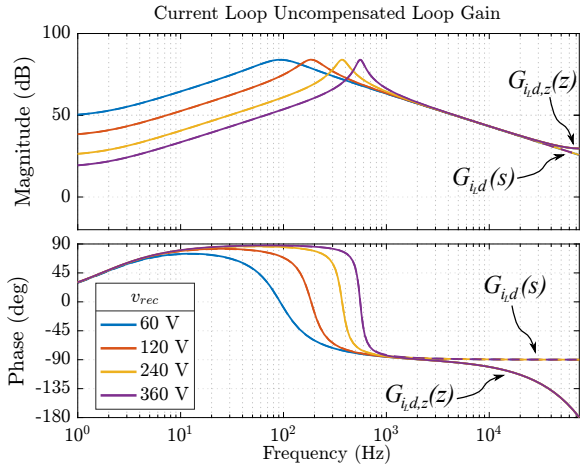
As discussed in the beginning of this section, i_{ref} is ideally generated in phase with v_{rec} by the PLL, i.e., $\tilde{i}_{\text{ref}} = R_{\text{eq}}^{-1}\tilde{v}_{\text{rec}}$, where R_{eq} is the desired equivalent resistance of the input port. Note that R_{eq} is a known value that only changes with output power, i.e., $R_{\text{eq}} = R\frac{V_{\text{rec}}^2}{V_{\text{out}}^2}$. Then (5) can be further simplified to

$$\tilde{i}_L = \underbrace{\left(\frac{G_c G_{i_L d} R_{\text{eq}}^{-1}}{1+G_c G_{i_L d}}\right)}_{Y_1} + \underbrace{\frac{G_{i_L v_{\text{rec}}}}{1+G_c G_{i_L d}}}_{Y_2} \tilde{v}_{\text{rec}} = Y\tilde{v}_{\text{rec}}, \quad (6)$$

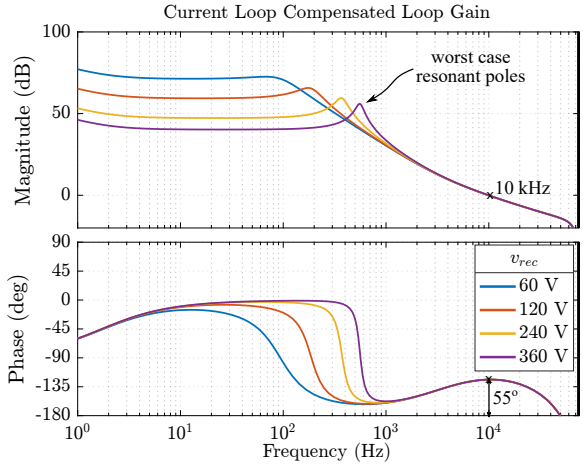
which readily gives the small signal admittance of the input port. According to (5), since the reference signal i_{ref} as well as v_{rec} contains DC component as well as AC component at twice line frequency and its harmonics, an adequate loop gain $G_c G_{i_L d}$ is needed at these frequencies to ensure that i_L closely tracks i_{ref} and the disturbance from v_{rec} is rejected. In other words, since ideally we would like the input port to appear resistive, i.e., $\tilde{i}_{\text{L}} = R_{\text{eq}}^{-1}\tilde{v}_{\text{rec}}$, we can make the observation from (6) that this requires an adequate loop gain $G_c G_{i_L d}$ such that Y_2 approaches zero while Y_1 reduces to R_{eq}^{-1} and dominates the total admittance Y.

Equation (3) is evaluated with the parameters in Table I and is plotted in Fig. 4a. Notice that since the control is implemented digitally, there is a significant phase lag due to the modulation delay, which is represented as $G_{i_L d,z}$ in the same figure. Therefore, in the following analysis we consider only the discrete model $G_{i_L d,z}$. A type-II compensator [25] denoted as $G_{c,z}$ is implemented in the micro-controller to stabilize the feedback loop with closed-loop bandwidth of 10 kHz. The compensated loop gain is shown in Fig. 4b.

For $G_{i_L d,z}$, a pair of resonant poles occur at $f_o = \frac{1-D}{2\pi\sqrt{LC}}$. It can be observed from Fig. 4b that starting from the crossover frequency, if we traverse the loop gain magnitude curve from right to left, the loop gain increases at 40 dB per decade as the frequency decreases until the resonant poles at f_o. To the left of f_o, the loop gain magnitude remains flat expect for very low frequency. In other words, with a certain crossover frequency, the loop gain at twice line frequency (100 Hz or 120 Hz) might be limited by the resonant poles. The frequency of the resonant poles f_o varies within each line cycle according to the instantaneous value of v_{rec} (since $1-D = \frac{V_{\text{rec}}}{V_{\text{out}}}$). The highest resonant pole frequency (i.e., worst case condition) occurs at the peak input voltage under high line condition. For a conventional PFC design with a boost converter, the filter inductor L is typically large (i.e., on the order of mH),



(a) Uncompensated current loop gain $G_{i_L d}(s)$ and $G_{i_L d,z}(z)$. Note the phase lag introduced by the digital control delay near sampling frequency.



(b) Compensated current loop gain $G_{c,z}(z)G_{i_L d,z}(z)$. The feedback loop is closed at 10 kHz with 55^o phase margin.

Fig. 4: Loop gain of the inner current feedback loop (highlighted in red in Fig. 3). The magnitude and phase varies with different instantaneous input voltage v_{rec}.

leading to the worst case f_o below 100 Hz. The gain at twice line frequency is therefore not affected and a loop gain crossover frequency of 10 kHz results in 80 dB gain at twice line frequency. Such high gain is adequate to achieve a close-to-unity power factor according to the aforementioned analysis on (5) and (6). However, for the 7-level FCML converter in this work, the inductor is two orders of magnitude smaller than that in a typical design of an equivalent boost converter. The worst case resonant pole frequency f_o in this design thus occur well above 100 Hz, as illustrated in Fig. 4b. With 10 kHz crossover frequency, the loop gain at twice line frequency could then be below 40 dB. As given in (6), the admittance of the 7-level FCML converter in this case is plotted in Fig. 5a. As expected, the term Y_2 in the input admittance starts to dominate above 100 Hz. Thus, the total admittance Y exhibits a large variation of magnitude above 100 Hz, and its phase has

a large leading phase angle at twice line frequency (i.e., 33^o), leading to distortion of the input current, poor power factor and zero-crossing distortion [26].

B. Feedforward control

One of the effective methods to solve current phase leading in PFC for high frequency AC input (i.e., a few hundred hertz to a few kilohertz) in airborne system or other microgrid applications is the feedforward control in [27]. The phase-leading problem in the 7-level FCML converter happens in a different scenario with line-frequency and small inductors, but the root cause is essentially the same.

With the addition of the complete feedforward control term in (7) to the main duty ratio

$$d_{ff} = 1 - \frac{v_{\text{rec}}}{v_{\text{out}}} + \frac{L}{v_{\text{out}}} \frac{\mathrm{d}i_{\text{ref}}}{\mathrm{d}t} \tag{7}$$

the input admittance can be calculated to be $Y = R_{\text{eq}}^{-1}$ for the entire frequency range. Because i_{ref} only changes at line frequency and the inductor L is especially small in the 7-level FCML converter, the contribution from the derivative term is very small compared to the voltage ratio term. Therefore, the derivative term can be dropped to simplify the calculation, i.e.,

$$d_{ff} = (1 - \frac{v_{\text{rec}}}{v_{\text{out}}}). \tag{8}$$

With the disturbance from v_{rec} being canceled, the input impedance under partial feedforward [27] can be derived to be Y_1 in (6). The resulting input admittance under partial feedforward is plotted and compared with complete feedforward and no feedforward in Fig. 5b. The input admittance under partial feedforward approaches constant R_{eq}^{-1} with almost zero phase shift up to a few kilohertz, enough to guarantee satisfactory PFC performance. Therefore, partial feedforward is implemented in the hardware prototype.

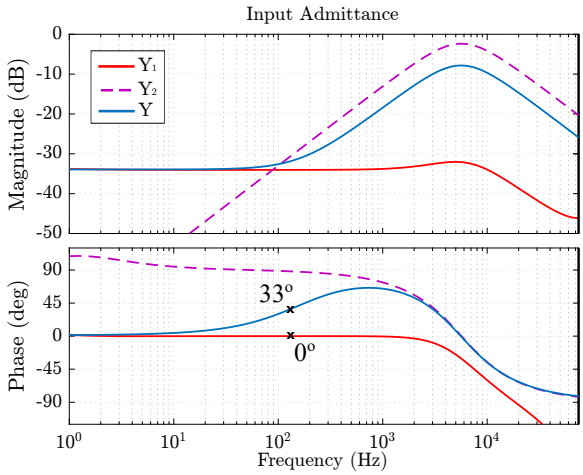
C. Voltage Loop

The outer voltage loop regulates the output voltage to the desired DC value (i.e., 400 V) by scaling the magnitude of the input current. As shown in Fig. 3, the output voltage loop provides a multiplying factor k to the current loop reference. The multiplying factor cannot change faster than 60 Hz, since it will introduce extra harmonics in the input current. For this reason, the crossover frequency of the voltage loop has to be designed well below 60 Hz [24]. The crossover frequency of the voltage loop is designed to be 10 Hz.

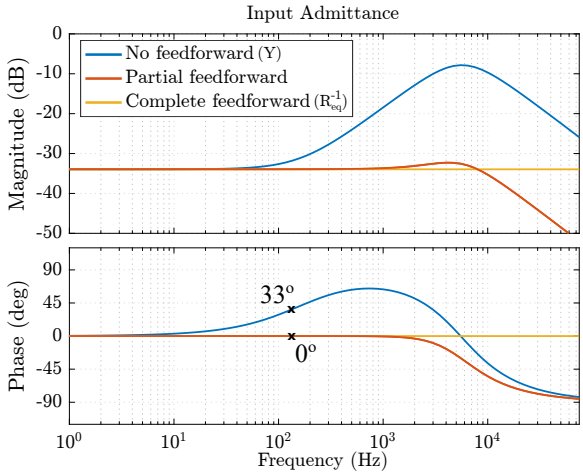
IV. Hardware Prototype

A hardware prototype of the 7-level FCML converter based PFC front end is designed and implemented as shown in Fig. 6. All the elements shown in Fig. 3 except C_{buf} and R are included in the hardware prototype.

The power stage consists of the active rectifier and the 7-level FCML converter. The switches in the active rectifier (i.e., S_{p1}, S_{p2}, S_{n1}, S_{n1} in Fig. 3) are each implemented by 4 MOSFETs in parallel to reduce conduction loss. The 400 V, 7-level FCML converter has a nominal transistor voltage stress of



(a) Input admittance of the 7-level FCML converter with no feedforward but only feedback control as specified in (6).



(b) Comparison of input admittance with and without feedforward control.

Fig. 5: Input admittance of the 7-level FCML converter with different control methods at peak input voltage.

67 V, so 12 of 100 V rated GaN transistors are used. Each GaN transistor has much smaller power loss compared to its high voltage counterparts. While the combined power loss of all the GaN transistors is comparable to that of a conventional boost converter, this loss is distributed among the GaN transistors in a relatively large area, allowing more surface for effective cooling. The gate driver floating power is supplied by low-cost and compact cascaded bootstrap scheme in [28]–[30] to further improve the overall power density and efficiency.

V. Experimental Results

The hardware prototype has been tested in various experiments to verify its performance. The experimental setup consists of an AC voltage source (Pacific power source 112-AMX), a DC load (Chroma 63204 DC electronic load) and

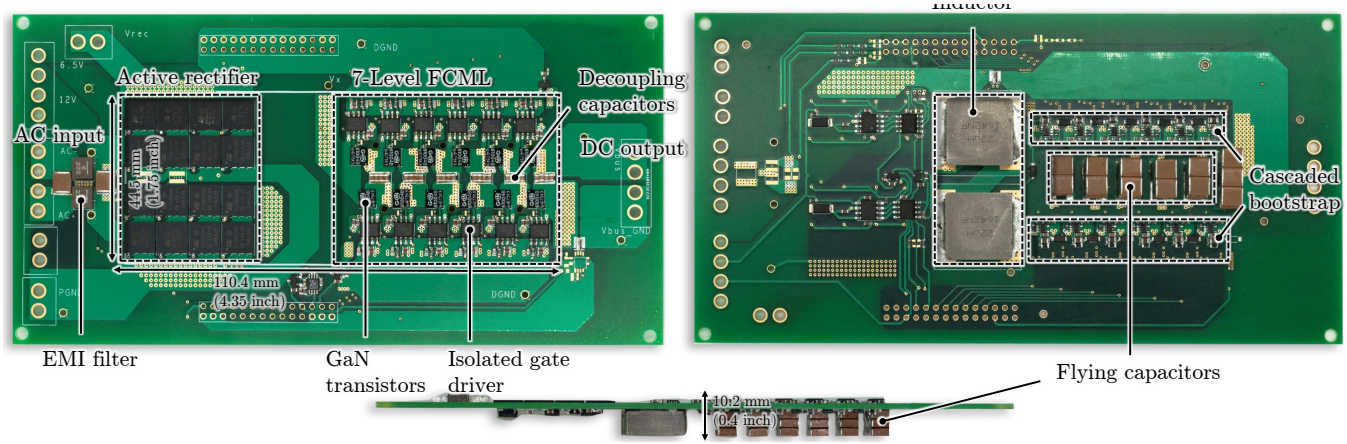
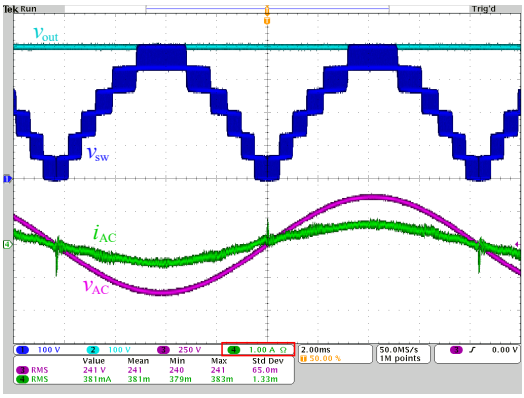
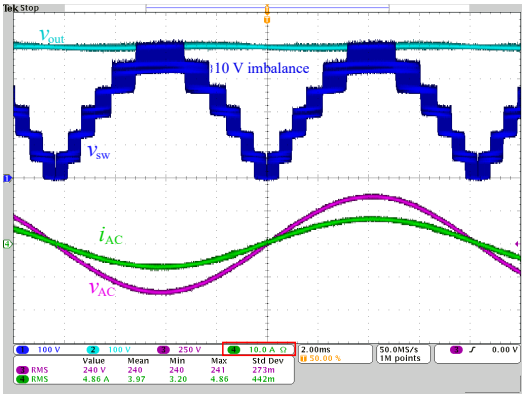


Fig. 6: Front, side and back view of the hardware prototype with key components highlighted.

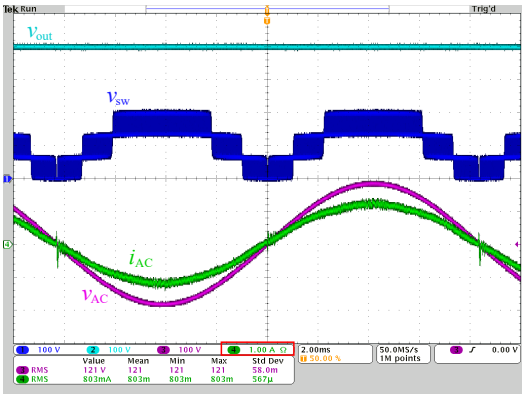


(a) Light load (100 W) operation.

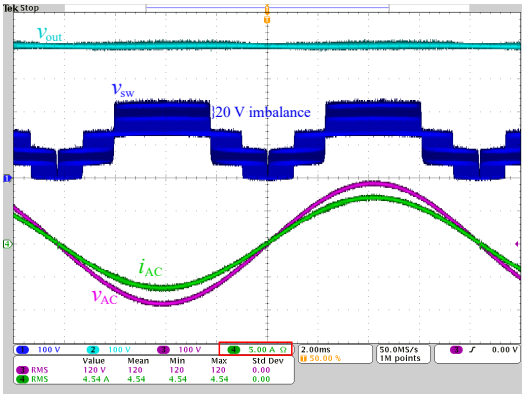


(b) Heavy load (1300 W) operation.

Fig. 7: Waveforms illustrating the PFC operation under high line voltage (240 V) condition. Note the difference in y-axis scale for the current waveform.



(a) Light load (100 W) operation.

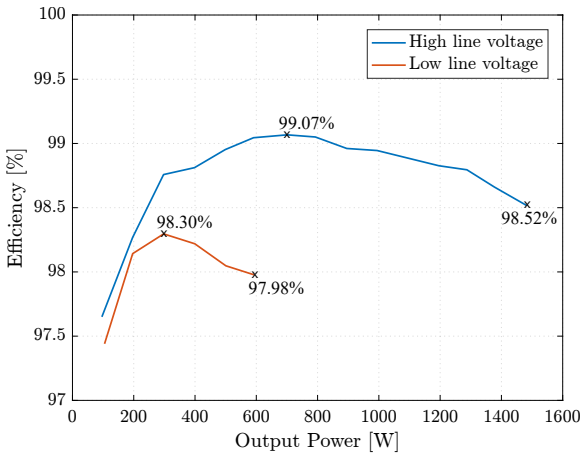


(b) Heavy load (600 W) operation.

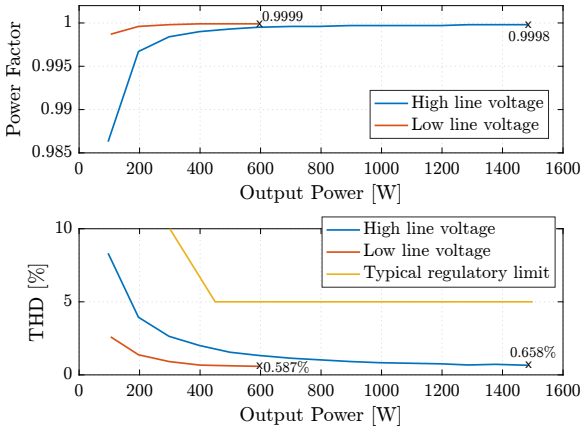
Fig. 8: Waveforms illustrating the PFC operation under low line voltage (120 V) condition. Note the difference in y-axis scale for the current waveform.

two digital power analyzers (Yokogawa WT310) to measure the input and output specifications.

The first experiment is to verify the multilevel operation of the 7-level FCML converter. This is illustrated in Fig. 7 and Fig. 8 for both high line (240 V_{rms}) and low line (120 V_{rms}) conditions. The output voltage is boosted to 400 V while the switching node voltage v_{sw} exhibits staircase waveform with 67 V increments. In high line condition, the switching node voltage v_{sw} transitions through all seven levels from 0 V to v_{out} and follows the trajectory of the rectified input voltage v_{rec}. In



(a) Efficiency.



(b) Input power factor and input current THD.

Fig. 9: Measured performance of the hardware prototype under low line voltage (120 V) and high line voltage (240 V).

low line condition, only the lowest four levels are exercised as the peak of v_{rec} is lower than the 4th level.

The performance measured with the digital power analyzers (i.e., efficiency, power factor and input current THD) across the entire load range is plotted in Fig. 9. In both light load and heavy load conditions, the input current is well in phase with the input voltage; the measured power factor is close to unity across the entire load range, demonstrating the effectiveness of the proposed control scheme. It can be observed from Fig. 8a that in high line voltage, light load condition, there is a small phase lead of i_{AC} to v_{AC}. This is due to the current flowing through the input filter capacitor C_{in} [31]. This current is at its largest with high input voltage and its effect is the most noticeable when the current into the converter is small. Nevertheless, the impact of the input capacitor current on the power factor is much smaller in this design compared to most conventional solutions as the 7-level FCML topology allows for much smaller input filter capacitor.

The efficiency of the hardware prototype is measured and

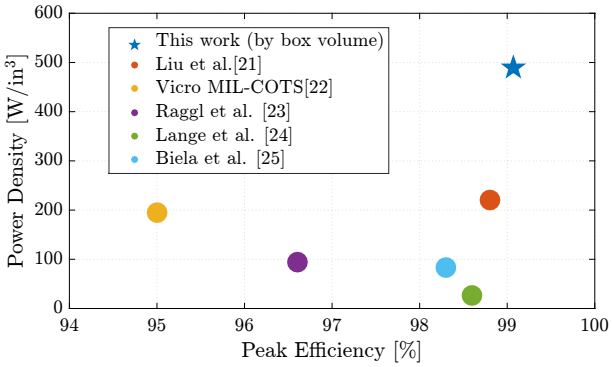


Fig. 10: Power density v.s. efficiency of this work and selected works.

TABLE II: Supplementary information of this work and selected works.

Reference	Topology & Features	Power (W)	Notes
this work	7-level FCML	1500	not including EMI filter and energy buffer
Liu et al. JESTPE 2016 [32]	interleaved MHz triangular current mode totem-pole bridgeless	1200	not including EMI filter and energy buffer
Vicor MIL-COTS [33]	N/A	1400	commercial product, not including EMI filter and energy buffer
Raggl et al. TIE 2009 [34]	interleaved boost	315	including EMI filter, heatsink and energy buffer
Lange et al. TPELS 2015 [35]	diode-clamped 3-level boost	3000	including EMI filter, heatsink and energy buffer
Biela et al. IPEC 2010 [36]	triangular current mode totem-pole bridgeless	3000	including EMI filter, heatsink and energy buffer

plotted in Fig. 9a. Note that the AC source used in the experiment (112-AMX) has a maximum current limit, so the power of the hardware prototype can only be tested up to 600 W under low line voltage condition and up to 1500 W under high line condition. The efficiency measurement includes the power loss in the output buffer capacitor C_{buf} but does *not* include the power consumed by the cascaded bootstrap circuit and the control circuit, which is about 0.5 W and 1.9 W, respectively. The peak efficiency of 99.07% occurs at about half of the nominal load. With the power stage dimension marked in Fig. 6 (i.e., 44.5 mm $\times$ 110.4 mm$\times$ 10.2 mm), the PFC front end achieves 29.9 kW/dm^3 (i.e., 490 W/in^3) power density by rectangular box volume. If we only the consider the volume of components (i.e., assuming an optimal layout and packaging), power density as high as 37.8 kW/dm^3 (i.e., 620 W/in^3) can be expected. The experimental peak efficiency and power density by box volume of this work is compared with selected best-in-class work in the literature and commercial products as plotted in Fig. 10, with corresponding supplementary information in Table II. The purpose of this survey is not to compare the absolute numbers but to provide a perspective on the potential improvements on efficiency and power density through the FCML approach.

VI. Conclusion

The main contribution of this paper is demonstrating the viability of the FCML approach in kilowatt level PFC applications. Our work shows in hardware that the FCML topology

brings significant power density and efficiency benefits. We also identify the potential control challenges in FCML based PFC and demonstrate how these problems can be solved. Lastly, we demonstrate that the practical circuit implementation complexity of the FCML topology can be managed through careful layout, new gate driving circuit design, etc.

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