Minimum Inrush Start-up Control of a Single-Phase Interleaved Totem-Pole PFC Rectifier

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Abstract: Smooth start-up to limit the inrush current is an important requirement in development of actively controlled power factor correction (PFC) rectifiers. In this paper, a thorough mathematical analysis is conducted to exploit the transient behavior during the start-up and thus, the expression for maximum inrush current is determined. Based on the analyses, a specifically designed start-up technique by controlling the time instant of engaging the PFC control loop is proposed, which achieves smooth start-up with zero current over/undershoot. As a proof-of-concept, experimental measurements are conducted at 1.5kW to validate the theoretical predictions. It is observed that there is no occurrence of inrush during the PFC start-up and also, unity power factor is maintained along with an efficiency of 98% and input current THD below 5%.

I. INTRODUCTION

Power factor correction (PFC) rectifiers are widely used front-end AC-DC power electronics interfaces in variety of applications like Electrical Vehicle (EV) chargers, mobile phone chargers, personal computer (PC) power supplies and LCD monitors. PFC rectifiers can provide unity power factor and low THD of the grid current to prevent the power electronics from polluting the power grid by drawing or injecting reactive power and unnecessary harmonics. Meanwhile, the output DC voltage is regulated tightly at the desired level for a wide range of grid AC inputs. To meet such challenging requirements, massive efforts are dedicated to investigate and develop suitable control strategies for PFC rectifiers. Along the path, majority of the conducted research works can be categorized into development of the following control methods: (i) average current control [1-3]; (ii) peak current control [4-7]; and (iii) one-cycle control [8-10] (iv) input voltage sensorless duty compensated feedback control [11]. Furthermore, studies have been conducted to establish control techniques with unique features, such as voltage mode control for a boundary conduction mode (BCM) boost PFC rectifier in [12] and boost PFC control loop without sensing the input inductor current in [13].

With various attentions on developments of different control methods and compensators, the problem of achieving unity power factor, low THD, and tight regulation of DC link voltage with universal AC input are fundamentally resolved. Further, researchers are looking into the theory and engineering efforts to improve the reliability and response speed of the converters under harsh load transients. However, the start-up procedure analysis of the PFC rectifier has been overlooked. The current consensus between both academia and industry is limiting the inrush current by start-up resistors to the level, which the hardware can tolerate. Only limited researches were conducted to analyze the start-up procedures [14-17]. A non-linear compensator was proposed to limit the inrush current and simultaneously minimize the start-up time for a three-phase boost PFC in [14]. Besides, an innovative start-up scheme was proposed for three-phase isolated boost PFC with an innovative topology configuration that couples an auxiliary flyback inductor and PFC input inductors in [15]. In addition to the aforementioned compensator design and topology innovation, a more practical and easy-to-execute start-up technique was proposed in [16], where the PWM signal is multiplied with a linear ramp signal before it is applied to the PFC MOSFETs. Furthermore, a variable step-size control technique was proposed in [17] to limit the inrush current during the start-up procedure. Above-mentioned literatures are mainly focused on start-up procedure of three-phase PFC rectifiers; however, the research for analyzing and improving the start-up procedure of a single-phase PFC rectifier, more specifically interleaved totem pole PFC, in a systematic fashion is currently in absence.

In order to address the aforementioned issues and concerns with the start-up process in a PFC rectifier, an algorithm to achieve minimized inrush current is discussed in this paper. The main contributions of this paper are: (i) mathematical analyses and modeling the start-up procedure of a single-phase interleaved totem pole PFC; and (ii) developing a specifically designed start-up technique by controlling the engage timing of the PFC controller to achieve zero inrush current. It is mathematically proved that the inrush current can be zero if the PFC action control is triggered at the negative-to-positive zero crossing of the input AC voltage. The paper is organized as follows: The mathematical expression of inrush start-up current is derived and thus, the suitable time instant for the transition of the converter operation from passive diode-bridge to actively controlled PFC with minimum inrush current is determined in Section II. The theory and analyses are validated by a set

of experimental results, presented in Section III. Section IV puts forward conclusions with relevant discussions.

II. Start-up Events and Inrush Current Control in a Three-Phase Boost-type PFC Rectifier

A simplified circuit of the single-phase interleaved totem-pole PFC structure is shown in Fig. 1(a). The two high-frequency legs maintain 180° phase difference in their switching operations, which effectively reduce the input current ripple. During the positive and negative half-cycles of the input AC voltage, the switches S_6 and S_5 are ON throughout, respectively. Therefore, the equivalent switching circuits during the positive and negative half-cycles are demonstrated in Fig. 1(b) and 1(c), respectively. The detailed operation principle of single-phase interleaved totem pole PFC can be referred to the well-established literatures in [1-9, 18-19].

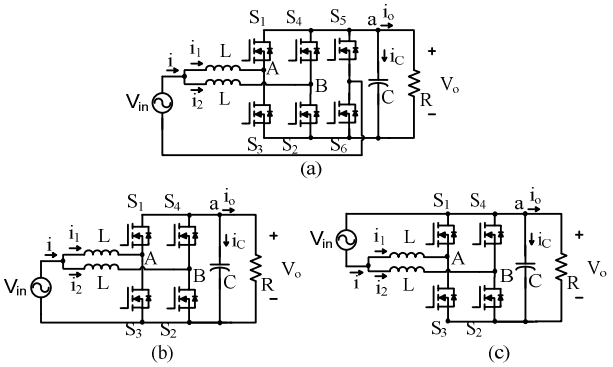


Fig. 1. Topology of an interleaved totem pole PFC rectifier: (a) basic circuit structure, (b) equivalent circuit in positive half line cycle, and (c) equivalent circuit in negative half line cycle.

For limiting the inrush current during start-up, a relay along with a protective resistor in parallel is placed at the input side between the AC grid and interleaved inductors, as shown in Fig. 2. The inrush current amplitude is dependent on the event sequence involved in PFC start-up action. From a practical point of view, the event sequence used in this design is as follows: (i) after power-up, the uncontrolled bridge rectifier turns on and the relay is turned off so that protective resistor comes in the current path, (ii) the relay is turned on and the protective resistor is bypassed, and (iii) the closed loop PFC control is engaged.

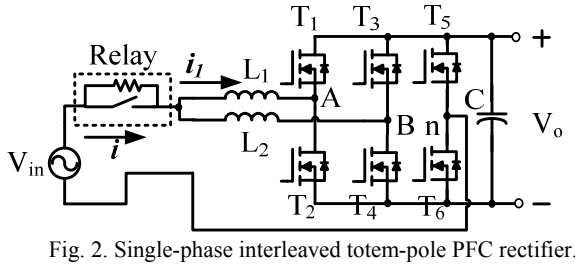


Fig. 2. Single-phase interleaved totem-pole PFC rectifier.

The first inrush can be limited to a desired current level by putting a suitable value of relay protection resistor. The major concerns for inrush current arising from all the transitions are discussed as follows.

First inrush: After powering up the circuit, it is assumed that the active semiconductors are disabled, as the auxiliary power supply driving the control ICs requires a minimum time to start-up. Therefore, the converter works as a passive three-phase diode bridge rectifier. In this mode of operation, the relay is kept turned-off and hence, the inrush phase current is limited by the ratio of the peak-peak input AC voltage to the parallel resistor of the relay i.e., as shown in Fig. 3. By suitable selection of protective resistor, the inrush current amplitude can be limited to a desired value. In this design, 20Ω resistor is used, which limits the inrush below 8A at 120V AC RMS input.

$$i_{max} = \frac{V_{in,max}}{R_{relay}} \quad (1)$$

With identical selection of inductors and semiconductor devices, the input grid current will be split uniformly between the two phases, with their individual maximum values shown as follows.

$$i_{1,max} = i_{2,max} = \frac{V_{in,max}}{2R_{relay}} \quad (2)$$

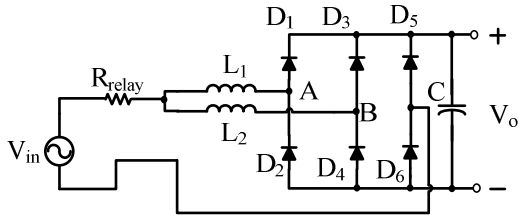


Fig. 3. Equivalent circuit during first inrush

Second inrush: At the instant when relay turns on i.e. paralleled resistor is bypassed, there would be a transient in the input current. Equivalent circuit in this mode of operation is shown in Fig. 4, which assumes that the relay-ON event occurs during the positive half-cycle. Applying KVL relationship for phase 'A' and KCL at the node connected to the DC link capacitor and output load, the following equations are formed.

$$V_{in} = \frac{L}{2}\frac{di}{dt} + V_O \quad (3)$$

$$C\frac{dV_O}{dt} + \frac{V_O}{R} = i \quad (4)$$

Substituting dV_O/dt in the derivative expression of Eq. (3), the relationship in Eq. (5) is formulated. Solving the differential equation (5), V_O can be obtained.

$$V_{in} = LC\frac{d^2V_O}{dt^2} + \frac{L}{R}\frac{dV_O}{dt} + V_O \quad (5)$$

$$V_O(t) = \exp\left(-{}^{tR}/_{L}\right)[Asin(\omega t) + Bcos(\omega t)] + V_{in} \quad (6)$$

Assuming $V_O(t=0-)=V_1$, B is obtained as $B=(V_1-V_{in})$. Since the inductor current always maintains a continuous function profile, $i(0-)=i(0+)=i_0$ holds true, which yields the expression of 'A' as follows.

$$A = \frac{1}{\omega C}\left(i_0 - \frac{V_1}{R}\right) + \frac{R}{\omega L}(V_1 - V_{in}) \quad (7)$$

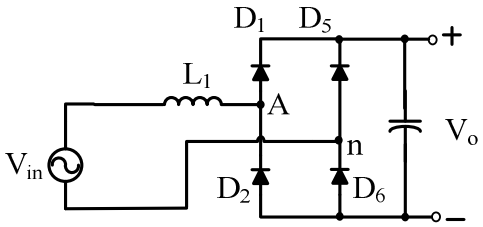


Fig. 4. Equivalent circuit for phase 'A' after relay-ON

The grid current at t=0+ can be expressed as follows.

$$i(0+) = C\frac{dV_O}{dt} + \frac{V_O}{R} = C\left[A\omega - \frac{R}{L}(V_1 - V_{in})\right] + \frac{V_1}{R} \quad (8)$$

Substituting the expression of 'A' in Eq. (8), the instantaneous grid current expression is restructured as follows.

$$i(t) = \exp\left(-Rt/L\right)\left[\left\{AC\omega + \frac{CR(V_{in}-V_1)}{L} + \frac{V_1-V_{in}}{R}\right\}\cos(\omega t) + \left\{\frac{A}{R} - \frac{ACR}{L} - \omega C(V_{in}-V_1)\right\}\sin(\omega t)\right] + \frac{V_{in}}{R} = \exp\left(-Rt/L\right)\left[\left\{\left(\frac{1}{\omega C}\left(i_0 - \frac{V_1}{R}\right) + \frac{R}{\omega L}(V_1 - V_{in})\right)C\omega + \frac{CR(V_{in}-V_1)}{L} + \frac{V_1-V_{in}}{R}\right\}\cos(\omega t) + \left\{\left(\frac{1}{\omega C}\left(i_0 - \frac{V_1}{R}\right) + \frac{R}{\omega L}(V_1 - V_{in})\right)\left(\frac{1}{R} - \frac{CR}{L}\right) - \omega C(V_{in}-V_1)\right\}\sin(\omega t)\right] + \frac{V_{in}}{R} \quad (9)$$

As can be seen from the above relation, the start-up current expression is dependent on the current level at the turn-on instant of the relay. By setting the turn-on instant at zero current, the inrush can be minimized to 5A at 1.5kW load power, using the converter specifications, as shown in Table I. The variations of inrush current at this transition with different input voltages at rated power and with different load powers at rated input voltage are shown in Fig. 5 and Fig. 6, respectively. The plots indicate that the inrush current magnitude is limited even below the peak current at rated power, which does not impose any additional constraints on the selection of device ratings.

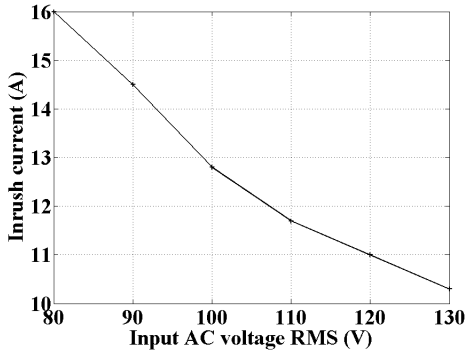


Fig. 5. Inrush current variation with input AC voltage at 1.5kW load

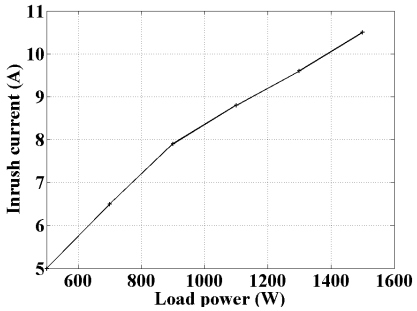


Fig. 6. Inrush current variation with various loads at 120V AC RMS

Third inrush: The third inrush occurs due to the transition from uncontrolled rectifier to active controlled PFC. Since the third inrush arises due to the involvement of switching, it cannot be passively controlled, rather has to be controlled by the enable timing of PFC action. Due to the switching, the output side of inductor (point *A*) and source neutral point (point *n*) become duty cycle (*D*) dependent, as shown in Fig. 7. Furthermore, the current flowing through the parallel branch of capacitor and load resistor is also duty cycle dependent, as shown in the KCL relation in Eq. (10).

$$i(2D-1) = C\frac{dV_O}{dt} + \frac{V_O}{R} \quad (10)$$

The duty is generated by the current loop PI controller in following way.

$$D(t) = k_p e(t) + k_i \int_0^t e(\tau)\, d\tau \quad (11)$$

where, *e(t)* is the instantaneous error in input current expressed by $e(t)=GV_{in}-i_1$, *G* is the DC voltage controller output implying the equivalent input trans-conductance. Therefore, expression of duty cycle can be restructured in Eq. (12). Substituting Eq. (12) into Eq. (10), the inter-relation between the input current and output voltage is synthesized in Eq. (13), where i_1 is the current flowing through phase 'A'.

$$D(t) = k_p(GV_{in} - i_1) + k_i \int_0^t (GV_{in} - i_1(\tau))\, d\tau \quad (12)$$

$$i_1\left[2k_p(GV_{in} - i_1) + 2k_i \int_0^t \left(GV_{in} - i_1(\tau)\right) d\tau - 1\right] = C\frac{dV_O}{dt} + \frac{V_O}{R} \quad (13)$$

In order to determine the dynamics of i_1, it is necessary to replace the output voltage in terms of input current, which can be found by implementing KVL in the loop V_{in}- *B*-*n*, as shown in Eq. (10).

$$V_{in} = L\frac{di_1}{dt} + DV_O \quad (14)$$

$$\frac{dV_O}{dt} = \frac{D\left(\frac{dV_{in}}{dt} - L\frac{d^2 i_1}{dt^2}\right) - \frac{dD}{dt}\left(V_{in} - \frac{di_1}{dt}\right)}{D^2} \quad (15)$$

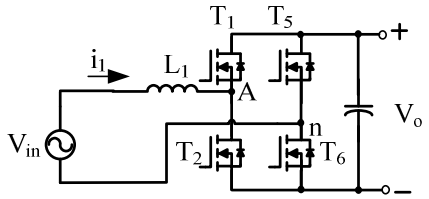


Fig. 7. Equivalent circuit for phase 'A' at steady state PFC operation

For the simplicity of the calculation, the duty cycle expression is transformed as follows.

$$D(t) = Ai_1 + B\int_0^t i_1(\tau)\,d\tau + Y \quad (16),$$

where $A = -k_p; B = -k_i;\ Y = k_pGV_{in} + k_iG\int_0^t V_{in}(\tau)\,d\tau$

Substituting the duty expression from Eq. (16) into Eq. (15) and thereby writing V_O and dV_O/dt in terms of i_1, the differential equation of i_1 is derived as follows.

$$i_1\left(2A\frac{d1}{dt} + 2Bi_2 - 1\right)\left(Ai_1 + B\int_0^t i_1(\tau)\,d\tau + Y\right)^2 =$$
$$\left[C\left(\frac{dV_{in}}{dt} - L\frac{d^2i_1}{dt^2}\right) + \frac{\left(V_{in} - \frac{di_1}{dt}\right)}{R}\right]\left(Ai_1 + B\int_0^t i_1(\tau)\,d\tau + Y\right) -$$
$$C\left(V_{in} - \frac{di_1}{dt}\right)\left(Ai_1 + B\int_0^t i_1(\tau)\,d\tau + Y\right) \quad (17)$$

For the simplicity of analyses, the following variables are defined.

$$X = Ai_1 + B\int_0^t i_1(\tau)\,d\tau + Y \quad (18)$$

$$y = V_{in} - \frac{di_1}{dt} \quad (19)$$

These defined variables further simplify Eq. (17), as shown below.

$$i_1\left(2\frac{dX}{dt} + i_1 - 1\right)X^2 = \left(C\frac{dy}{dt} + \frac{y}{R}\right)X - Cy\frac{dX}{dt} \quad (20)$$

This further simplifies to the following, which is a first order differential equation with a particular integral term, dependent on i_1.

$$i_1\left(2\frac{dX}{dt} + i_1 - 1\right) = C\frac{d}{dt}\left(\frac{y}{X}\right) + \frac{1}{R}\frac{y}{X} \quad (21)$$

The general solution of the above differential equation can be expressed as follows.

$$\frac{y}{X}\exp\left(\frac{t}{RC}\right) = \int_0^\tau \frac{y}{X}i_1\left(2\frac{dX}{dt} + i_1 - 1\right)dt \quad (22)$$

Since obtaining the deterministic expression of i_1 through particular integral solution would be challenging, the variation of input current is determined using the initial and final values of 'y' in Eq. (22). In the expression of 'y', di_1/dt is replaced in terms of dX/dt, i_1 by taking derivative on Eq. (21).

$$\frac{di_1}{dt} = \frac{\frac{dX}{dt} - Bi_2 - \frac{dy}{dt}}{A} \quad (23),$$

which yields to the simplified expression for 'y': $y = V_{in} - L\frac{\frac{dX}{dt} - Bi_1 - \frac{dy}{dt}}{A}$ (24)

At t=0-, X holds a constant value, which is the upper saturation level of the current loop PI compensator; therefore dX/dt=dY/dt=0 holds. Due to diode bridge operation, the input current will be held at zero for a significant portion of line cycle. Assuming the control being turned on while i_1=0, 'y' simply equates to V_{in}. Assuming the peak current occurs at t=t*, di_1/dt=0 holds at the current maximum value, which again makes 'y' equal to V_{in}. Therefore, the general expression of input current can be formulated as follows.

$$i_1 = GV_{in}[1 - \exp(-Bt/A)\sin(\sqrt{\frac{B}{A}}t + \varphi)] \quad (25)$$

If the control is turned on during the transit from positive to negative half-cycle, the maximum input current can be $i_{1,max1}$, which can be as large as $2GV_{in}$ given $t^* \rightarrow 0$ as shown in Eq. (26).

$$i_{1,max1} = GV_{in}[1 + \exp(-Bt^*/A)] \quad (26)$$

On the other hand, if the control is applied near the zero crossing from negative to positive half-cycle, the peak input current can reach $i_{1,max2}$, whose maximum value is GV_{in} i.e. the rated steady state value as shown in Eq. (27).

$$i_{1,max2} = GV_{in}[1 - \exp(-Bt^*/A)] \quad (27)$$

In order to determine the accurate peak input current value and its corresponding time instant, it is necessary to solve for di_1/dt=0, which gives as follows.

$$\tan\left(\sqrt{\frac{B}{A}}t^* + \varphi\right) = \sqrt{\frac{B}{A}} \quad (28),$$

which implies $t^* = \sqrt{\frac{A}{B}}[\tan^{-1}\left(\sqrt{\frac{B}{A}}\right) - \varphi]$.

Although the circuit operation and the implementation of control algorithm are symmetric at both zero crossings from positive-to-negative and negative-to-positive half cycles, the inrush transient dynamics after enabling the control is not symmetric in both zero crossings.

Due to reduced peak current, the PFC control loop is engaged during the zero crossing from negative to positive half-cycle, which is represented in the overall control block diagram in Fig. 8. PFC control algorithm is enabled by a trigger signal, which becomes HIGH during the negative to positive zero crossing of the input AC voltage. Detection of the zero crossing of the input AC voltage is performed through implementation of second order generalized integrator (SOGI)-based phase locked loop (PLL). The SOGI sampling time is kept same as the switching cycle i.e. 10μs. Since the switching cycle is 1600 times smaller than a line cycle period, the maximum deviation of zero crossing accuracy can be limited by $\pm\frac{360^0}{1600} = \pm 0.225^0$.

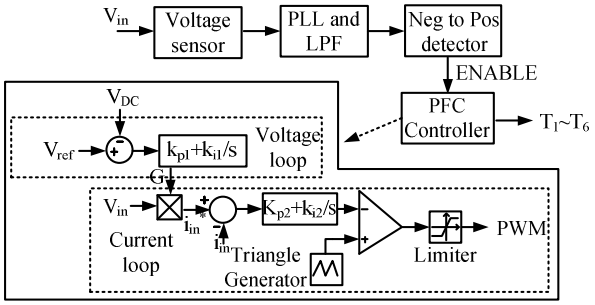


Fig. 8. Block diagram for PFC control with minimized inrush current

III. Experimental Results

In order to validate the proof-of-concept, the proposed algorithm is implemented in a laboratory prototype of interleaved totem-pole PFC, shown in Fig. 9. The key design parameters along with the detailed converter specifications are provided in Table I. The control algorithm is digitally implemented in DSP TMS320F28335.

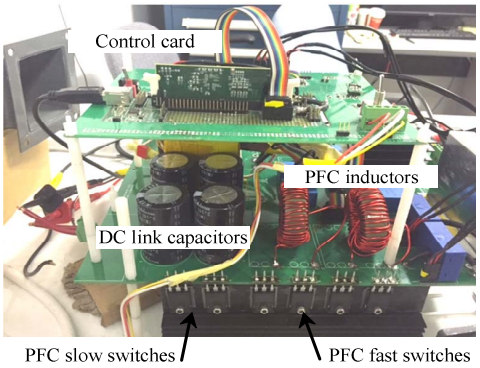


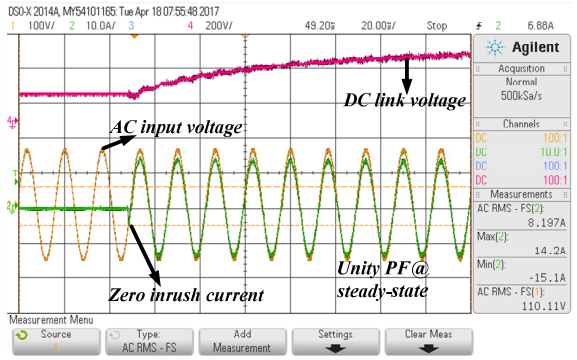
Fig. 9. The image of the 1.5 kW prototype

Table I. Key design parameters and their specifications

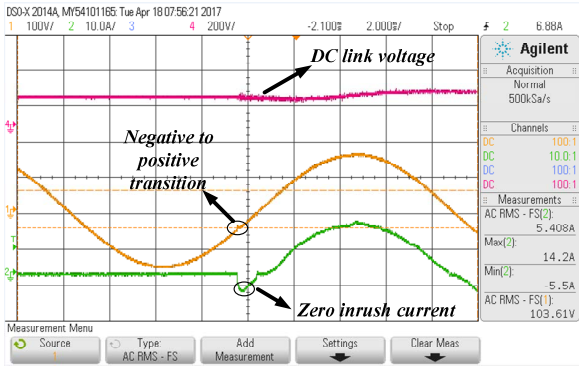
Parameters	Values	Quantity
Input AC voltage (V_{in})	120V, 60 Hz, single-phase	-
Output voltage reference (V_o*)	400V	-
Output power (P_{out})	1.5kW	-
Boost inductances (L)	0.3mH	2
Output DC capacitance (C)	1mF	1
High frequency MOSFETs	CMF80120D	4
Low frequency MOSFETs	CMF40120D	2
Switching frequency (f_{sw})	100 kHz	-

The PFC converter waveforms are shown in Fig. 10 (a), which indicates an efficiency of 98%, input current THD of 4.7% and power factor of 0.996 at the steady state operation. The start-up waveforms of the interleaved totem pole PFC with the proposed start-up scheme are shown in Fig. 10(a) and Fig. 10(b). The DC link voltage is settled at its reference level within 8 line cycles i.e. ~130ms. Although voltage settling takes relatively longer time, the current loop PI compensator is fast enough to ensure unity power factor within one line cycle only. It is worth mentioning that the current loop zero is placed at ~400Hz and loop bandwidth is kept at 8 kHz considering the tradeoffs between transient dynamics and attenuation offered to the high frequency components.

At a rated power (1.5kW) operation, the first inrush occurring during the turn-on of uncontrolled diode bridge circuit is limited to 8A, which is determined by the input AC voltage, output capacitor and load resistance. The most significant inrush (i.e. third inrush) occurring during the turn-on of control is non-existent while the transient happens near the zero crossing from negative to positive half-cycle. On the other hand, Fig. 10(c) demonstrates a higher start-up current of 40A, if the transition is made at crossing from positive to negative half-cycle, which maintains good agreement with the analytical prediction. Therefore, this start-up algorithm allows us to select the MOSFET current rating based on rated load nominal operation without any additional considerations from start-up inrush.



(a)



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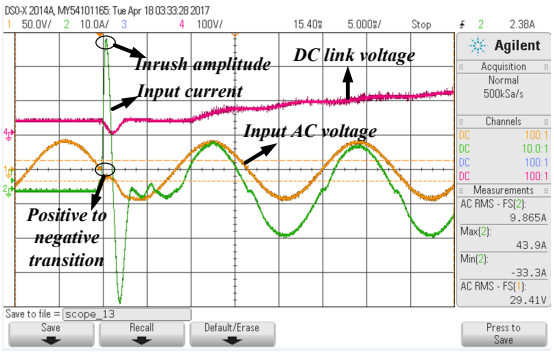

(c)

Fig. 10. (a) PFC start-up waveform at 1.5kW load, V_{in}=120V 60Hz AC RMS, V_{DC}(ref)=400V (b) the transition of the converter from uncontrolled to controlled PFC action during negative to positive zero crossing; (c) PFC start-up waveform while the PFC control is engaged during positive to negative zero crossing of input voltage; the inrush current goes as high as 40A

IV. CONCLUSIONS

In this paper, a start-up algorithm for minimizing the inrush current in an interleaved totem pole PFC is proposed and analyzed. In the overall event sequence of PFC start-up, the maximum current inrush can potentially occur during the transition of converter operation from passive diode-bridge to actively controlled PFC stage. By properly adjusting the time instant of engaging the PFC controller in the start-up process, the inrush current can be made zero. The proposed approach is verified using a 1.5kW experimental prototype of a single-phase interleaved totem-pole PFC converter,

which exhibits a power factor >0.996 in the steady state and 130 ms start-up time with zero inrush current during the transition to PFC operation.

V. ACKNOWLEDGEMENT

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