

Improving Light Load Power Factor for GaN Based Totem Pole Bridgeless PFC using Digital Phase Locked Loop Based Vector Cancellation & Tracking Error Compensation

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Abstract— The paper proposes a digital based control method which can be used on power factor correction (PFC) circuit to improve converter power factor (P.F.) at light load conditions. A major contributor to a non-unity P.F. is the need of input capacitor to alleviate differential mode electromagnetic interference (EMI) conducted back to the AC source. At light load, the overall system impedance (EMI filter and PFC circuit) becomes more capacitive which leads to large phase difference between voltage and current and results in a low power factor. A digital phase locked loop based vector cancellation (DPLLVC) technique is proposed in this digest to improve the light load P.F. This technique improves upon the previously proposed Phase Leading Filter Current Compensation (PLFCC) technique as it no longer requires a derivative of the input voltage, which can add noise. In addition to DPLLVC technique, a tracking error compensation scheme is added to further improve the PF under light loads. The scheme is tested and results reported on a 3.3KW Gallium-Nitride (GaN) based Totem Pole bridgeless PFC (TTPL PFC) design. With DPLLVC and tracking error compensation techniques, over 37% P.F. improvement is observed when compared to the results with PLFCC technique at 2% load.

Keywords—Totem Pole Bridgeless PFC; PLL; PF; GaN

I. INTRODUCTION

To improve energy efficiency and power quality, there are more and more standards which require high power factor at light load. For example, 80PLUS Titanium requires Power Factor (PF) > 0.95 with 20% load. Additionally, electric vehicle (EV) chargers – specially on-board chargers – can spend significant time doing trickle charging; and as more of these loads connect to the grid effort has to be made to improve light load power factor and power quality [1] [2]. In order to achieve high P.F. in an AC-DC application, a bridge rectifier followed by a PFC Boost converter is generally applied, Fig 1. In the recent years, the development of wide bandgap semiconductors like GaN enable the possibility of using TTPL PFC to achieve both high P.F. and high efficiency at the same time [3] [4] [5] [6], Fig 2. Regardless if it is a PFC with or without bridge rectifier, input capacitor is always required to alleviate differential mode EMI conducted back to the AC source. At light load, the overall system impedance (EMI filter and PFC circuit)

becomes more capacitive which leads to large phase difference between voltage and current and results in a low power factor, as depicted in Fig 3 and [7] [8] [9]. By interleaving the Boost PFC stage, the differential mode noise as well as the required input capacitance can be greatly reduced [7]. However, low P.F. at light load issue still exists.

Recently a Phase Leading Filter Current Compensation (PLFCC) technique was proposed [9], where a phase lead is provided to the current reference by adding a scaled version of the derivative of the input voltage. Use of derivative can result in additional noise because of harmonics and noise on the sensed signal. Furthermore application of this technique to TTPL PFC is not discussed in [9]. One key difference in application to totem pole topologies when using this technique is the drive

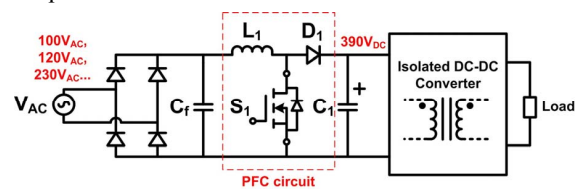


Fig. 1 PFC circuit with Rectifier Bridge

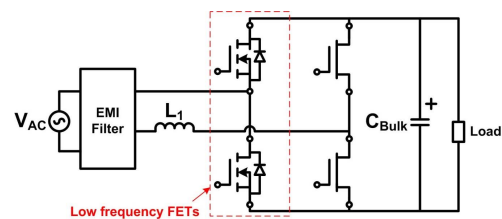


Fig. 2 Bridgeless PFC Circuit

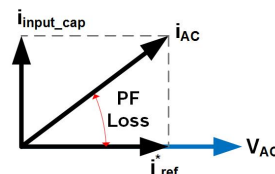


Fig. 3 Input capacitor current related PF degradation when current reference is in phase with voltage exactly.

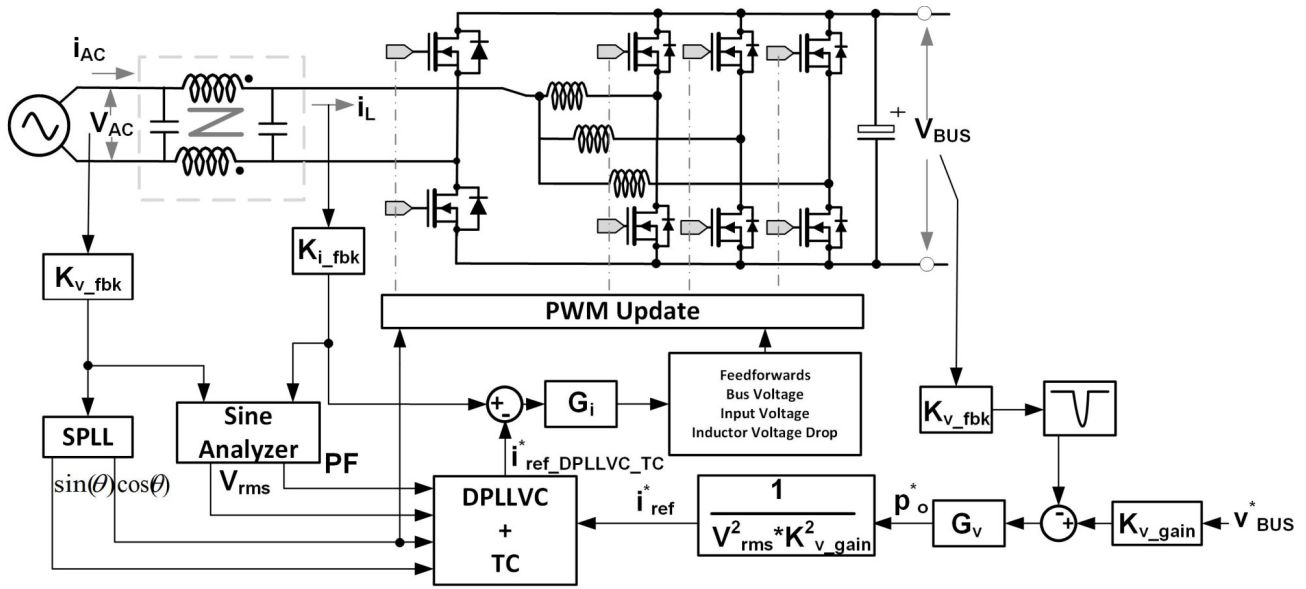


Fig. 7 Control Structure of Single Phase CCM Totem Pole PFC with DPLLVC and Tracking Error Compensation.

single controller across a wide load range, but at ultra-light loads the open loop gain is still reduced. Due to interaction with the EMI filter it is not possible to increase the gain and hence tracking error is observed at light loads.

The control structure with the proposed enhancements of DPLLVC and tracking error compensation is shown in Fig. 7. The enhancements are discussed in the following section in detail.

III. DIGITAL PHASE LOCKED LOOP BASED VECTOR CANCELLATION (DPLLVC)

Input capacitance current draw results in loss of power factor as shown in the phasor diagram in Fig. 1, where a current i_{ref}^* is commanded from the voltage loop compensator such that it is in phase with the input voltage v_{AC} . With the DPLLVC $i_{ref_DPLLVC}^*$, shown in Fig. 2, is used as the current command of the PFC circuit and is composed of two components one is the current command from the voltage loop compensator that is denoted as i_{ref}^* and an adjustment $i_{input_cap_comp}$. Given ω is the AC frequency the $i_{ref_DPLLVC}^*$ can be written as (1).

$$i_{ref_DPLLVC}^* = i_{ref}^* \sin(\omega t) - i_{input_cap_comp} \cos(\omega t) \quad (1)$$

Thus the total input current can be written as (2)

$$i_{AC} = i_{ref}^* \sin(\omega t) + (i_{input_cap} - i_{input_cap_comp}) \cos(\omega t) \quad (2)$$

If $i_{input_cap} = i_{input_cap_comp}$ unity power factor is achieved, however it is hard to achieve in a practical system because of input cap tolerance and change with temperature and aging [9]. Nevertheless applying this correction results in improvement relative to no correction at all. This analysis assumes the inductor current follows the reference current. Under ultra-light loads this might not be the case due to open loop gain reduction. Hence a tracking error compensation scheme is proposed in addition to DPLLVC in the following section.

IV. TRACKING ERROR COMPENSATION

Using DFF, good tracking of the reference is possible under a wide variety of loads [12]. However under ultra-light loads, because of the non-linearity of the inductance, tracking error is observed because of reduced gain in the system. This results in a phase lag in the actual inductor current with respect to the reference. Thus an additional phase lead component is added to compensate for this tracking error as shown in (3). Unlike input cap compensation used in DPLLVC, this tracking error needs to be reduced as power level increases and open loop gain improves hence a scaling term with power is incorporated in the tracking error correction.

$$\begin{aligned} i_{ref_DPLLVC_TC}^* &= i_{ref}^* \sin(\omega t) \\ &- i_{input_cap_comp} \cos(\omega t) \\ &- i_{tracking_error_comp} \Big|_{power_dependent} \cos(\omega t) \end{aligned} \quad (3)$$

TABLE I. TEST DATA OF THE DESIGNED CONVERTER OPERATING AT 220VRMS, 50HZ AC INPUT UNDER VARYING LOAD CONDITION AND WITH DFF CONTROL (NO CORRECTION APPLIED), WITH DFF PLUS DPLLVC AND WITH DPLLVC AND TRACKING ERROR COMPENSATION

Input Power (Watts)	No Correction			With DPLLVC				With DPLLVC and Tracking Error Compensation				
	Input Current (Amps)	iTHD (%)	PF	Input Current (Amps)	iTHD (%)	PF	$i_{input_cap_comp}$	Input Current (Amps)	iTHD (%)	PF	$i_{input_cap_comp} + i_{tracking_error_comp}$	
28.36	0.486	16.2	0.2528	0.337	20.5	0.3632	0.01	0.161	65.1	0.7666	0.028	
46.61	0.505	15.8	0.3997	0.367	18.2	0.5487	0.01	0.226	41.5	0.8911	0.028	
64.80	0.537	14.3	0.5212	0.412	15.6	0.6812	0.01	0.298	30.2	0.9386	0.028	
138.20	0.738	10.5	0.8121	0.659	9.8	0.9074	0.01	0.606	15.2	0.9839	0.028	
211.54	1.003	8.1	0.9141	0.952	7.1	0.9642	0.01	0.921	9.2	0.9937	0.025	
284.83	1.293	5.8	0.9554	1.257	5.4	0.9832	0.01	1.239	6.3	0.9964	0.022	
358.72	1.596	4.9	0.9741	1.569	4.7	0.9911	0.01	1.559	5.2	0.9976	0.020	
503.95	2.209	3.8	0.9894	2.191	3.5	0.9968	0.01	2.188	3.8	0.9987	0.018	



Fig. 8 Designed 3.3KW Totem Pole Bridgeless PFC Board.

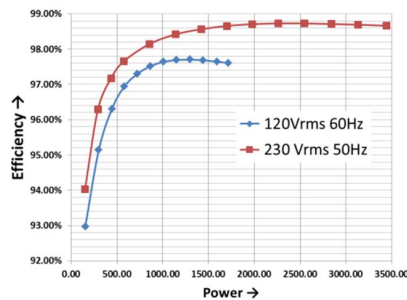


Fig. 9 Efficiency of the converter at high line and low line across power levels.

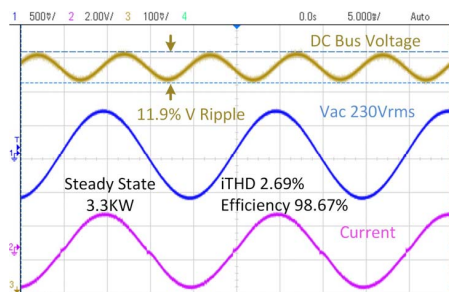


Fig. 10 Steady state condition at high line and full load.

V. EXPERIMENTAL RESULTS

A 3.3kW Totem Pole Bridgeless PFC board was designed as shown in Fig 8. The input EMI filter is on the top left hand side of the board. Texas Instruments TMS320F280049M device is used to implement the control of the power stage and Texas Instruments LMG3410 is selected for the GaN switches. 100kHz is selected as the PWM switching frequency. Fig. 9 shows the efficiency of the design at low line and high line condition and Fig. 10 shows the waveform at steady state and full load. Figs. 11 through 13 show the voltage and current waveforms under ultra-light load (2% load) for the rectifier with DFF control, DFF control plus DPLLVC, and DFF control plus DPLLVC plus tracking error compensation respectively. As can be observed, input current is smoother and RMS value is lower with DFF plus DPLLVC & tracking error compensation under the same load condition. Table 1 lists the complete input, output power and current THD and PF for the tests performed. The data is graphed in Fig. 14 which illustrates the results of improved PF.

A power dependent tracking error element is shown to improve the power factor further. For example on the designed converter the EMI filter cap is around 2.2 uF which translates to roughly 0.01 per unit (pu) current under high line condition. Therefore when applying DFF plus DPLLVC a fixed value of 0.01 is used, whereas when using DFF plus DPLLVC and tracking error compensation the factor is changed as shown in Table 1 empirically, which results in further improvement of PF. With the addition of the proposed control changes, an apparent degradation is observed on current THD, when it is plotted with respect to power Fig 15. However this apparent degradation is because RMS value of the current changes as PF improves. Whereas sources of THD, such as deadtime distortion, remain the same. Hence a better metric to determine THD degradation is plotting THD with respect to RMS current, which takes into account the power factor improvements, Fig 16. With which it is seen that the THD difference is much less or negligible.

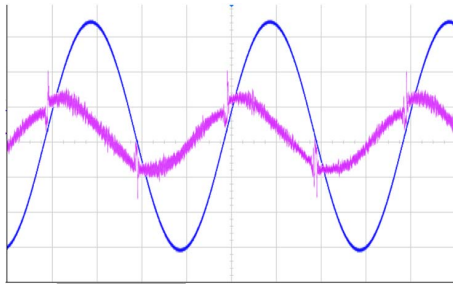


Fig. 11 Voltage(blue) and current(pink) waveform with DFF control at $I_{in,rms}=0.5368$ Amps, $P_{in}=64.80W$.

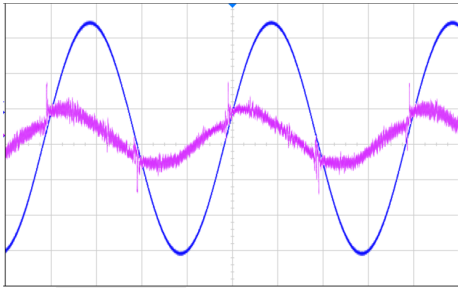


Fig. 12 Voltage(blue) and current(pink) waveform with DFF plus DPLLVC $I_{in,rms}=0.4118$ Amps, $P_{in}=64.80W$.

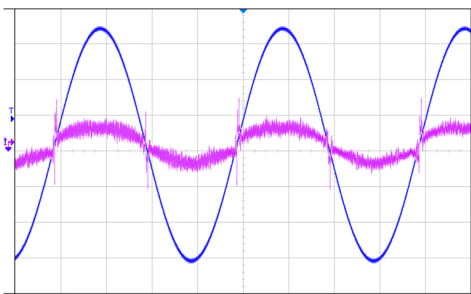


Fig. 13 Voltage(blue) and current(pink) waveform with DFF plus DPLLVC & tracking error compensation, $I_{in,rms}=0.2983$ Amps, $P_{in}=64.80W$.

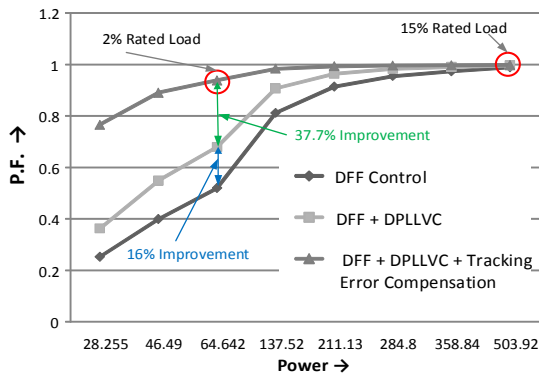


Fig. 14 PF with only DFF Control, DFF Control plus DPLLVC and DFF Control plus DPLLVC and Tracking Error Compensation.

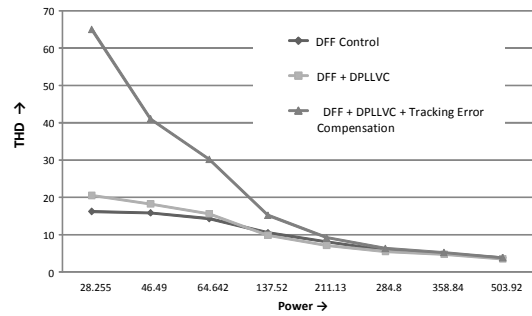


Fig. 15 Current THD w.r.t Power using DFF Control, DFF plus DPLLVC and DFF plus DPLLVC and Tracking Error Compensation.

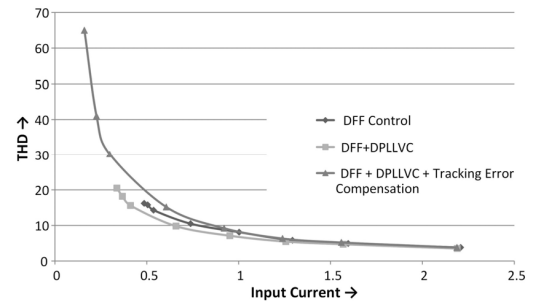


Fig. 16 Current THD w.r.t RMS Input Current using DFF Control, DFF plus DPLLVC and DFF plus DPLLVC and Tracking Error Compensation

VI. CONCLUSION

In this work, enhancements to the PLFCC method using DPLVCC is proposed, which enables its application in distorted grid conditions. Furthermore, application to interleaved TTPL PFC is discussed in this paper, which has not been addressed in literature so far. Tracking error is identified as an additional source of PF degradation and a compensation scheme is proposed. It is shown that with DPLVCC PF at 63W (2% Load) is improved by 16%, which is what will be expected with PLFCC. With tracking error compensation added 37% additional improvement is observed along with 44% reduction in the current draw from the mains. Under even lighter loads the improvement is even higher.

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