Design Considerations of Highly-Efficient Active Clamp Flyback Converter Using GaN Power ICs

Lingxiao Xue, Jason Zhang
Navitas Semiconductor
El Segundo, CA, USA
lingxiao.xue@navitassemi.com
jason.zhang@navitassemi.com

***Abstract*— High switching frequency and high efficiency are critical in reducing power adapter size. The active clamp flyback (ACF) allows soft switching under all line and load conditions, eliminating all leakage inductance and snubber losses. This paper discusses key design considerations for high density ACF converters by looking into ZVS condition, RMS current reduction, and EMI optimization. Current-dip effect and secondary resonant scheme are found to significantly improve efficiency. GaN power ICs, with low output charge & integrated drive with reduced parasitics, are ideal for high frequency ACF. A 65 W USB-PD adapter was built to 24 W/in^3 cased power density and 93.4% worst case efficiency. The design met European CoC Tier 2 and US DoE Level VI efficiency requirement and the EN55022 Class B conducted EMI standard.**

Keywords*— *Gallium Nitride; GaN power IC; Active Clamp Flyback; ACF; Power Adapter; Soft Switching; High Frequency; Critical Conduction Mode; USB Power Delivery; EMI

I. INTRODUCTION

With the rapid market adoption of fast charging and USB-PD standards, there is a growing need for significant power density improvement for travel adapters. In a fully enclosed adapter, any size reduction through package innovation or high frequency switching must be accompanied by efficiency improvement to maintain low adapter case temperatures. The single switch quasi-resonant (QR) flyback is popular in power adapter application but suffers from snubber loss, hard-switching loss, and excessive EMI, especially at elevated switching frequency above 150 kHz.

Active clamp ZVS flyback (ACF) [1][2][3][4], shown in Fig. 1, replaces the diode clamp with an active switch (S2). During operation, the energy stored in the leakage inductance (L_r) is transferred to the clamping capacitor (C_r) when S1 is turned off. By turning on S2 in Fig. 1, C_r recycles the leakage inductance energy and delivers it to the load and achieves zero voltage soft switching for the main switch S1.

Due to clamping switch S2, the switch node (V_{SW}) sees a stable voltage without overshoot, improving the device voltage margin, as shown in Fig. 2.

More importantly, S2 allows magnetizing inductance to conduct reverse current (i_{Lm}<0). When the magnetizing inductance accumulates enough energy, it will be utilized to achieve soft switching for S1, recycling the energy stored in output capacitance of S1 and S2 and transformer winding capacitance.

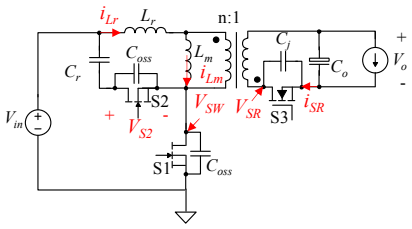


Fig. 1. Active clamp flyback (ACF) with parasitic capacitors

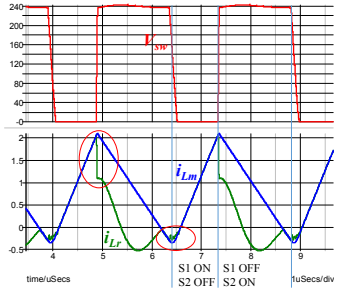


Fig. 2. Typical ACF waveforms with parasitic capacitance considered

However, due to the use of high output charge switches or un-optimized ACF operation/control, large negative magnetizing current would build up. Large negative current needs to be compensated with larger peak current, which increases conduction loss for the transformer and switches and core loss. Therefore, it is critical to minimize negative magnetizing current. GaN power ICs only need 0.2 A of magnetizing current to achieve full ZVS, where equivalent silicon requires more than 0.5 A. The optimal negative value will be discussed in Section II. Section III addresses additional methods to minimize the RMS current and reduce conduction loss. Section IV discusses EMI reduction. One design example is provided in Section V.

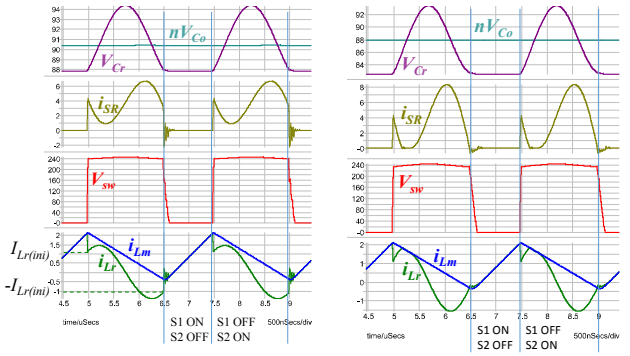
II. ZERO-VOLTAGE-SWITCHING CONDITION

Zero-Voltage-Switching (ZVS) is initiated by a freewheeling stage where the switch current flows from the

source to drain terminal and discharges the switch output capacitance. As shown in Fig. 1, after S1 turn-off, L_r current has sufficient energy to automatically rise to the clamping voltage, allowing S2 turn-on under zero voltage condition, assuming adequate deadtime.

The ZVS condition for S1 is more complicated. Some earlier ACF operates in CCM mode where magnetizing current stays positive [1]. In this case, ZVS is achieved with the energy stored in leakage inductance L_r. Quite often, ZVS cannot be achieved in light load or at high line. In addition, the secondary synchronous rectifier (SR) device cannot be turned off under zero-current-switching condition.

Driving the magnetizing current negative [2] (DCM or CrM mode) provides more consistent ZVS under all line and load conditions. The secondary SR could also be turned off with ZCS, as shown in Fig. 3(b), depending on the resonant parameters of L_r and C_r. ZCS SR switch turn-off allows simple SR control and avoids potential shoot through and body-diode reverse-recovery loss. Therefore, Fig. 3 (b) is preferred mode of operation.



(a) (b)

Fig. 3. ACF waveforms: (a) without secondary ZCS; (b) with secondary ZCS.

In case of ZCS Fig. 3 (b), after S2 is turned off, the magnetizing inductance L_m resonates with the lumped switching node capacitance C_{SW}, which includes output capacitance of primary switches, reflected SR output capacitance, transformer winding capacitance, and other parasitic capacitances. The resonant period and characteristic impedance is

$$T_r = 2\pi\sqrt{L_r C_{sw}},\ Z = \sqrt{L_r / C_{sw}} \tag{1}$$

This resonant process can be described by the state trajectory chart in Fig. 4, with the horizontal axis representing the switch node voltage V_{SW} and the vertical axis the product of magnetizing current i_{Lm} and characteristic impedance Z. Fig. 4(a) shows the case when the input voltage V_{in} is lower than the reflected voltage $n*V_O$, ZVS can be naturally achieved if the deadtime is longer than

$$T_{d1} = \frac{\pi - \cos^{-1}(V_{in} / nV_o)}{2\pi} \cdot T_r \tag{2}$$

Typically, designs can tolerate a deadtime up to $T_r/2$. Longer deadtime re-charges the switch-node voltage, and then the S1 turn-on would incur partial hard switching. Note that in this case, the resonance starts with zero magnetizing current.

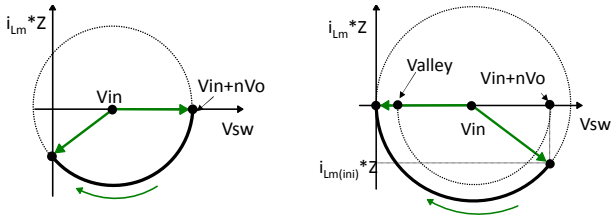
If input voltage (V_{in}) is higher than $n*V_O$, as shown in Fig. 4 (b), the resonance starting with zero magnetizing current swings V_{SW} to the minimum valley point, where S1 can turn-on with minimum V_{DS} voltage. This is typically called valley switching. In order to achieve full ZVS, S2 should stay on long enough until i_{Lm} becomes

$$i_{Lm(ini)} = -\frac{\sqrt{V_{in}^2 - (nV_o)^2}}{Z} \tag{3}$$

and then the deadtime should last for

$$T_{d2} = \frac{\pi - \cos^{-1}(nV_o / V_{in})}{2\pi} \cdot T_r \tag{4}$$

before S1 turns on. Equation (3) shows the minimum negative current for full ZVS, and (4) represents max deadtime. Note that from in Fig. 4 (b), any deadtime other than (4) with minimum negative current (3) will cause switching loss, due to due to partial hard switching. To add margin, practical implementation uses slightly more negative. However, too much negative current will results in a bigger trajectory loop and increased circulating energy. In general, (3) and (4) criteria should be satisfied as close as possible with added design margin in deadtime.



(a) (b)

Fig. 4. State trajectory for ZVS of S1. (a), $V_{in} < n*V_O$. (b) $V_{in} > n*V_O$

The negative magnetizing current rises when S2 is on:

$$i_{Lm(ini)} = i_{Lm(pk)} - \frac{nV_o \cdot T_{on(S2)}}{L_m} \tag{5}$$

where $i_{Lm}(pk)$ is the magnetizing peak current and Ton(2) is the S2 ON time. In order to maintain (3) and (4) under all input and output voltages, $T_{on}(S2)$ needs to be updated for different input, output conditions by ACF controllers, which is called Critical Conduction Mode (CrCM) operation.

III. Minimizing Conduction Loss

After achieving soft-switching, switching loss is eliminated, especially when fast GaN power ICs with integrated gate drive are used [5]. However, ZVS requires extra circulating current and ZVS transition incurs duty cycle loss, which increases RMS current and conduction losses. Following the control scheme in Section II, negative magnetizing current is minimized. In Fig. 3, i_{Lr} will conduct through the primary-side circuit including the two high-voltage switches and the

transformer primary side; i_{SR} will flow through the SR device and the transformer secondary side. Both i_{Lr} and i_{SR} should be designed to carry minimized RMS current. In this section, two techniques are discussed to reduce conduction loss.

A. Secondary Side Resonance Technique

In traditional ACF converter, after S1 turns off, the leakage inductance L_r will resonate with the primary clamping capacitor C_r, and the clamping-capacitor charge balance is achieved within the S2 ON time. In order to achieve SR ZCS, the clamping capacitor is selected to be small which leads to high resonant current i_{Lr} that touches the magnetizing current i_{Lm} and reduces SR current to zero, which prematurely turns off the SR. Later on, i_{Lr} will deviate again from i_{Lm} and SR turns on again. This output-current 'double-dipping' phenomena confuses the SR controller and may end up with long and lossy body-diode conduction time.

A secondary side resonant technique was proposed in [3] primarily to solve the SR double turn-on issue. The patent-pending idea is to use a small output capacitor to dominate the resonance so that the current always dips down in the beginning due to the factor that reflected output voltage is lower than the clamping voltage, as shown in Fig. 5.

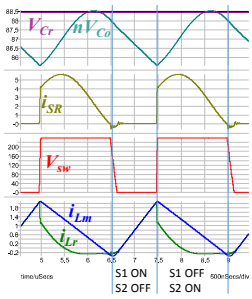


Fig. 5. ACF waveforms with secondary resonant scheme.

The ACF with primary resonant used C_r = 94 nF and C_o = 330 μF while with the secondary resonant, C_r = 1 μF and C_o = 33 μF / 25 V (ceramic), with a 1 μH inductor and 330 μF bulk capacitor inserted to filter output voltage ripple. Both tests were conducted at the same input (350 V) and output voltages (20 V). The waveforms proved that secondary resonant has clean SR waveform while the primary counterpart suffers from SR double turn-on.

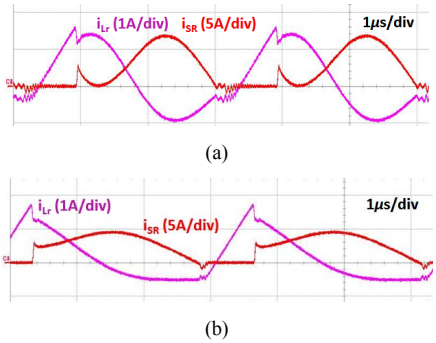


Fig. 6. Transformer current waveformss with different resonant schemes. (a) primary resonant (b) secondary resonant.

Moreover, by looking at Fig. 6, since i_{Lr} begins with a downward resonance, and i_{SR} with an upward resonance, the converter immediately starts to deliver power to the load in secondary resonant scheme while in the primary resonant scheme, load current happens much later. Since both i_{SR} waveforms bear the same average values for the same load, the RMS value for secondary side scheme would be lower. Based on a 45 W / 20 V ACF converter, the experimental results are shown in Fig. 7. There is a significant reduction of RMS current from both sides of the transformer, which reduces the conduction loss. The overall converter loss and efficiency are shown in Fig. 8.

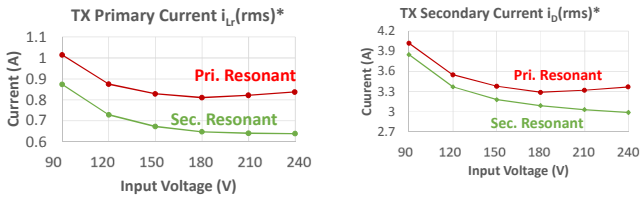


Fig. 7. Transformer RMS current with different resonant schemes. (a) transformer primary current i_{Lr} (b) transformer secondary current i_{SR}. Meausred at 45 W / 20 V.

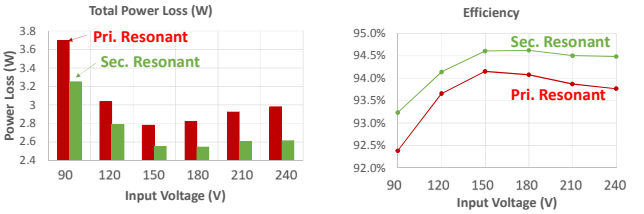


Fig. 8. Power loss and efficiency measurement on a 45 W / 20 V ACF board comparing primary and secondary resonant schemes.

B. Primary Current Dip Effect

In Fig. 2 and Fig. 5, we can see i_{Lr} current dips right after S1 turns off. Analytical expressions have been derived in [3]. This paper gives a more intuitive understanding on this phenomenon. The equivalent circuit after S1 turns off is shown in Fig. 9. The secondary side parasitic capacitance C_j and the output voltage are reflected to the primary side. At S1 turn-off, all parasitic capacitors will be charged or discharged including C_{OSS} and C_j. Primary current i_{Lr} equals to the peak of magnetizing current $i_{Lm(max)}$, which stays constant during this transition so is represented by a current source in the right figure.

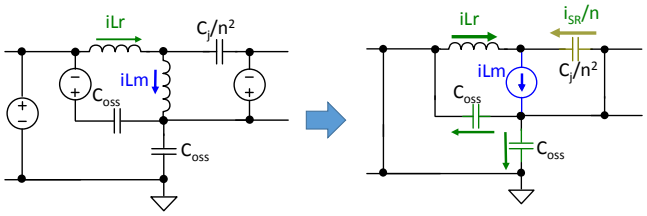


Fig. 9. Equivalent Circuit during the Current Dip

For transient AC analysis, a further simplification is possible by shorting the voltage sources. If ignoring the leakage inductor L_r, the L_m current will be immediately divided into two branches, with the amount of current at each side determined by the capacitance ratio 2 x $C_{OSS}/(C_j / n^2)$. As a result, the i_{Lr} current dip means more current has been delivered to the load side instead of circulating at the primary-side clamping loop. In order to maximize the current dip at i_{Lr}, we want the ratio to be smaller so more current is diverted to the secondary side.

GaN power ICs were selected based on their very low and linear $C_{OSS(tr)}$ as well as integrated drive - both of which translate in to higher efficiencies at increasing frequencies. Lower $C_{OSS(tr)}$ reduces the capacitance ratio between primary and secondary thus increase the current dip. The relatively linear output capacitance of GaN allows for fast soft switching transitions and short deadtimes with only 0.2A ZVS current. Shorter deadtimes enable lower duty loss, which is critical for high efficiency, high frequency operation. With silicon-based solutions, full ZVS is sacrificed in order to avoid excessive deadtimes and increased duty cycle loss. Unfortunately, partial ZVS incurs a significant increase in switching loss which degrades efficiency and limits high frequency capability. In addition, GaN power ICs, with integrated gate drive and reduced parastics between driver and FET, virtually eliminate turn-off losses, which is critical for high-frequency operations. With discrete GaN or Si solutions, the parasitics in the gate drive loop cause excess noise and unintended turn-on of the switch, thereby increasing losses. To mitigate such risks, increased gate impedance is needed but that slows down switching and increases switching losses. GaN power ICs achieve virtually zero turn-on *and* turn-off switching losses without any risk of unintended turn-on. An experimental comparison was conducted with Navitas GaN Power ICs and silicon MOSFET devices and the key parameters are summarized in TABLE I. The waveforms are compared below with the same testing setup. We can the Si converter has less current dip and larger negative and positive current. Due to the 2.5x larger output capacitance and lack of integrated gate driver, the Si converter shows 1.1 A RMS current versus GaN's 0.9 A, with 70% higher $R_{DS(ON)}$. As a result, a design optimized with GaN power ICs achieves 2 % higher efficiency compared to a silicon-based solution in the 200-300 kHz operating range. In addition, compared to discrete GaN or Si solutions, GaN power ICs offer smaller PCB footprint, ease of use, faster switching, higher noise immunity, simplified manufacturing and increased reliability. The efficiency benefit of GaN power ICs over discrete GaN or silicon becomes even greater at higher frequencies making these alternate technologies impractical.

TABLE I KEY PARAMETER COMPARISON: SI FET VS. GAN PWR IC

	IPA60R299CP	***NV6115***
Voltage Rating (V)	650	650
On Resistance $R_{DS(ON)}$ (mΩ)	270	160
Output Capacitance $C_{o(tr)}$ (pF)	120	50
Gate Charge Q_g (nC)	22	2.5
Reverse Recovery Charge Qrr (nC)	3900	0

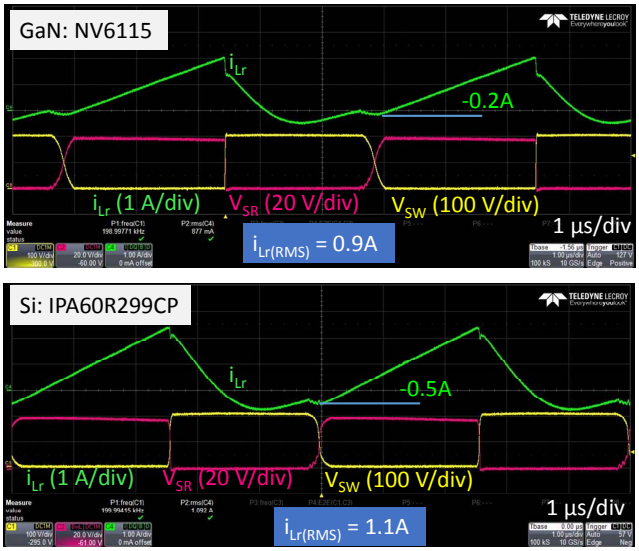


Fig. 10. Measured waveform comparison between GaN and Si. Si converter has higher i_{Lr}(RMS) due to both higher C_{OSS} and less current dip effect.

IV. EMI OPTIMIZATION

ACF in general has cleaner waveforms compared to traditional flyback. However, EMI still needs to be carefully dealt with in order to comply with standard.

In Fig. 1, SR device is placed at the low side for easy driving. For common mode (CM) EMI evaluation, the input and output capacitors can be treated as short circuits, then the equivalent circuit becomes Fig. 11 (a). The two ground symbols represent the isolated primary ground and secondary ground. Normally the two grounds are not at the same potential and the noise current between them will be captured by the LISN. In order to reduce measured common mode noise, the current between the two grounds should be minimized.

In Fig. 11 (a), V_{SW} voltage induces current through the transformer inter-winding capacitance and the loop is completed through the impedance between the primary and secondary grounds according to the blue line. The secondary noise voltage, whose amplitude equals to V_{SW}/N_p*N_s, will flow along the orange line. It is clear the currents between primary and secondary grounds from the two paths add up to each other. This configuration needs big CM filters to suppress the noise.

In contrast, if SR device is placed at V_{OUT} line, then the equivalent circuit becomes Fig. 11 (b). Following the same derivation, it can be found that the CM noise between the two grounds from the two paths cancel with each other. Since N_p does not equal to N_s, most likely the noise will not be fully canceled but the overall measured CM noise will be reduced.

In fact, this mechanism not only happens to the main windings but also to the auxiliary windings. Fig. 12 shows an ACF transformer with two main windings and two auxiliary winding. While N_p, N_s, and N_{ap} all generate CM noise in the

same direction, N_{as} induces a CM current countering the others. Since the excitation voltage potential of N_{as} is low, the induced CM current through its parasitic capacitance will not be able to fully cancel the total CM currents in the opposite direction generated by the rest three windings. Therefore, a balance capacitor C_b is added to lower the impedance of this path. The perfect value of C_b requires tuning but the method in [6] can be conveniently used. The idea is to connect an external waveform generator across N_p, measure the voltage between the two grounds by adjusting C_b value until the measured voltage has the minimum amplitude.

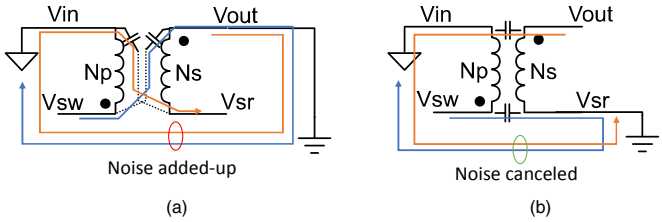


Fig. 11. Common mode noise propagation path: (a) SR device grounded; (b) SR device floated

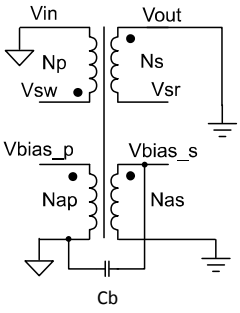


Fig. 12. Adding a balance capacitor to cancel CM noise

Fig. 13 shows the measured CM noise spectrum with/without the balance capacitor. The CM noise is suppressed by 30 dB at switching frequency by adding a balance capacitor, even without using a CM choke.

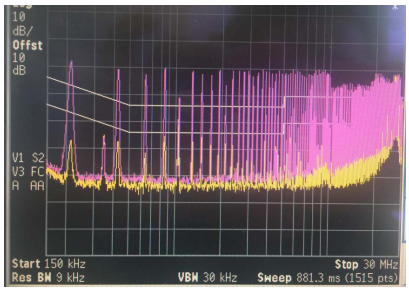


Fig. 13. Common Mode EMI Comparison: with and without balance capacitor. Significant CM reduction with balance capacitor.

CM noise balance can also be neatly achieved by artifically controlling the parasitic capacitance but will require more trial and error. With properly balanced CM noise, the bigger CM choke can be eliminated with only a small high frequency CM choke is needed since the above mentioned model does not apply due to parasitic capacitance impact at high frequency. By reducing CM chokes, efficiency can be further improved.

V. 65 W USB-PD ACF Example

A 65 W ACF adapter was built supporting USB Power Delivery (PD). The converter outputs 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, and 20 V / 3.25 A at universal AC inputs (90-264 V_{AC}). Assuming a case thickness of 2.5 mm, this board achieves size of 51 x 43 x 20.5 mm cased, and power density of 1.5 W/cc, 24 W/in^3 cased. The switching frequency is in the range of 140-490 kHz under universal AC input. The key components are listed in TABLE II.

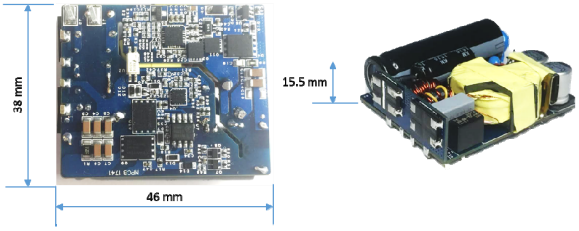


Fig. 14. 65 W USB-PD ACF Converter

TABLE II 65 W ACF USB-PD Key Components

	Part Number
Primary High-Side FET	NV6115 (160 mΩ GaN Power IC)
Primary Low-Side FET	NV6117 (110 mΩ GaN Power IC)
Secondary SR FET	150 V, 16 mΩ
Bulk Capacitors	82uF
Transformer	RM8/ILP, N49, L_m = 65 μH
Secondary Capacitor (C_o)	33μF x2
Primary Capacitor (C_r)	220 nF x2
Output Inductor (L_o)	1 μH

The efficiency at 20 V output is measured at different load the input AC voltages. The board achieves 93.5% efficiency at the worst case 90 V_{AC}.

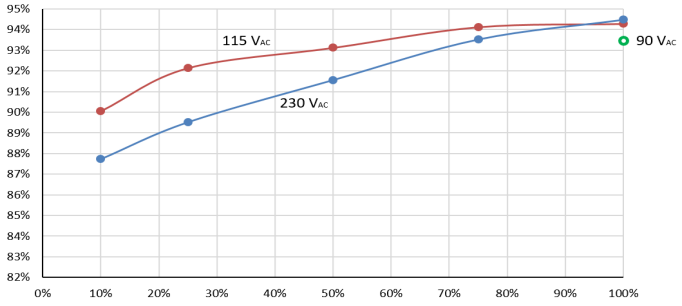


Fig. 15. Efficiency at 20 V output against load and input voltages.

The design is fully compliant with European CoC Tier 2 and US DoE Level VI efficiency standards, in addition to reaching peak efficiencies of over 94% at full load, as shown in Fig. 16.

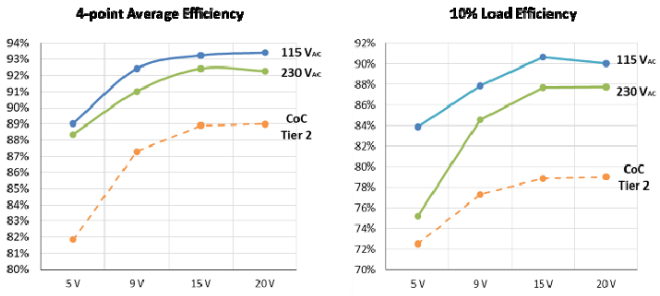


Fig. 16. Efficiency complies with European CoC Tier 2 with margin

Conducted average EMI was measured at 115 V and 230 V AC input and full load (20 V / 3.25 A) and the results are shown in Figure 17 and 18, which is below EN55022 Class B average limit.

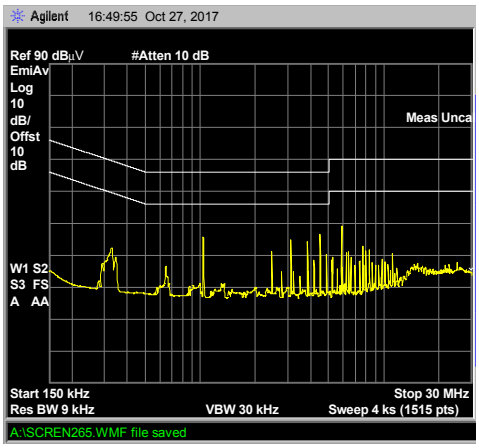


Fig. 17. Conducted average EMI measurement results versus EN55022 Class B Average limit at 115 V_{AC}.

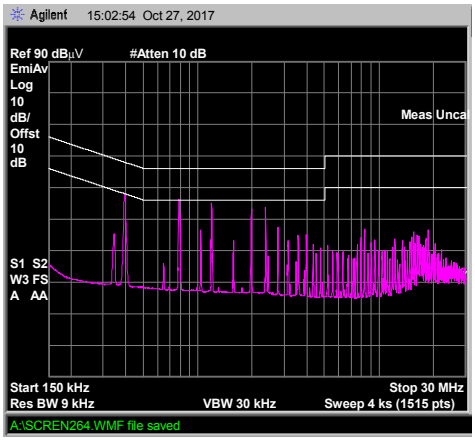


Fig. 18. Conducted average EMI measurement results versus EN55022 Class B Average limit at 230 V_{AC}.

VI. CONCLUSION

Several design considerations of active clamp flyback are provided to optimize efficiency. Using Critical Conduction Mode control and GaN power ICs, ACF can achieve ZVS in all conditions with minimum circulating energy. A patent-pending secondary-resonance scheme can be utilized to reduce conduction loss. GaN power ICs enable reduced circulating currents and lower switching losses achieving significant efficiency benefits over discrete Si or GaN alternatives, especially at increasing switching frequencies. In addition, GaN power ICs offer greater ease of use, smaller footprints, simplified manufacturing, higher reliability & lower system costs. By optimizing transformer design and utilizing the balance technique, common mode filters can be simplified. As a demonstration, a 65 W ACF USB-PD adapter was built using Navitas GaN Power ICs and achieved 24 W/in^3 cased power density and 93.4% worst case efficiency. The design is fully compliant with European CoC Tier 2 and US DoE Level VI efficiency standards and meets the EN55022 Class B EMI standard.

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