Design Consideration of Active Clamp Flyback Converter with Highly Nonlinear Junction Capacitance

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***Abstract*— Active clamped flyback converter performs zero voltage switching (ZVS) and recycling the leakage energy of transformer to boost the efficiency in higher frequency operation. Although it is well known that the switch-node capacitance determines the circulating energy for ZVS, the capacitance-nonlinearity impacts from each of the two primary-side switches and from the secondary synchronous rectifier have not been well understood. In this paper, the design tradeoff and system performance with different nonlinearity of junction capacitance from each switching device are investigated across the full load to light load operations, and then control strategies to overcome the capacitance nonlinearity are proposed. Then, analytical equations and design procedures are developed, considering the nonlinearity impact. Finally, the above studies and control method are supported with the experimental verifications on a 30W charger and a 45W adapter using state-of-the-art GaN and silicon FETs.**

Keywords—Gallium Nitride; GaN; Super Junction; Silicon; Active clamp Flyback; ACF; Zero Voltage Switching; ZVS; High Frequency; Power Density

I. INTRODUCTION

With the rapid development of portable devices and the quick charging technology of batteries, the increasing load demand requires the travel adapter to have significant power density improvement. Moreover, the migration of high-current USB Type C cable and the new USB PD standard urge the need of more efficient power conversion [1]. Higher switching frequency operation reduces the size of transformer, EMI filter, and output capacitors for higher power density design. Two transition-mode flyback converter for travel adapters have been widely used: passive-clamp flyback (PCF) with valley switching [2][3], and active-clamp flyback (ACF) with zero voltage switching (ZVS) [4][5][6][7][8]. Their circuit diagrams are illustrated in Fig. 1, and the major differences on switching waveform are compared in Fig. 2. For PCF, the power dissipation on the passive clamping circuit and turn-on switching loss of low-side switch (Q_L) with valley switching becomes a hurdle for higher frequency design, while ACF is able to eliminate the two losses.

Firstly, the high-side switch (Q_H) of ACF forces the clamp capacitor (C_{clamp}) resonating with leakage inductance of transformer (L_k) to recycle the L_k energy to output, so the clamping loss can be eliminated. Secondly, a proper control on the on time of Q_H allows magnetizing current (i_m) further changed into the reverse direction in order to store enough energy on magnetizing inductance (L_m) to achieve ZVS. After Q_H turns off, the negative magnetizing current ($i_{m(-)}$) discharges the lumped switch-node capacitance (C_{sw}) to bring switch-node voltage (V_{sw}) down to 0V before Q_L turns on, so the turn-on switching loss can also be eliminated. However, the additional $i_{m(-)}$ enlarges the flux density on the transformer magnetic, so the core loss is higher than PCF. Also, the resonance current is a part of the current flowing through both windings of transformer, so total winding loss is also higher than PCF. Therefore, it is possible that too large negative current can wash out the efficiency benefit of ACF, if C_{sw} is too large.

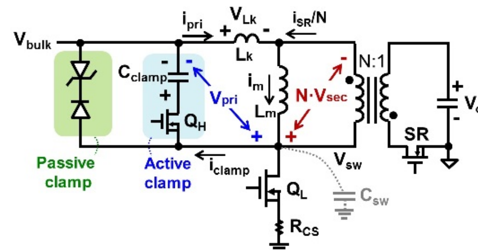

Fig. 1. Circuit diagram comparison on PCF and ACF topologies

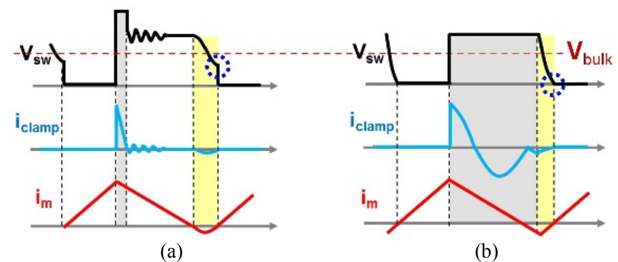

Fig. 2. Switching waveform comparison: (a) PCF, (b) ACF

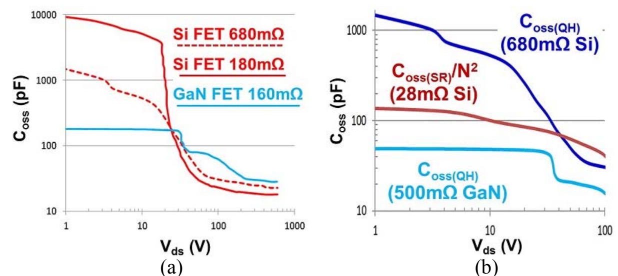

Fig. 3. C_{oss} nonlinearity: (a) comparison between Si and GaN on primary switches, (b) comparison with reflected capacitance from Si SR

The emerging gallium nitride (GaN) device provides significantly lower junction capacitance (C_{oss}) [9], so it is straightforward that the less ZVS energy of GaN-based ACF

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benefits the efficiency gain [5][6][7][8]. However, the cost-sensitive nature of the adapter market forms a hurdle on the fast adoption of GaN, while silicon (Si) super-junction FET with more mature process and competitive cost structure still dominates. Recent, the improvement on 600V Si FET opens an opportunity for ACF, due to retaining less tradeoff between turn-on loss increment and lower on-state resistance ($R_{ds(on)}$), and minimizing the hysteresis loss during soft switching [10][11]. Fig. 3(a) compares C_{oss} of the state-of-the-art GaN and Si FETs. As $R_{ds(on)}$ of Si FET reduces, C_{oss} becomes much higher for V_{ds} < 20V but slightly less at higher voltage area. Additionally, C_{oss} of new Si FET at high voltage area is even less than GaN with similar $R_{ds(on)}$. This leads to several questions to be further investigated, such as what is the advantage and drawback of the C_{oss} nonlinearity to ACF, and how to improve the performance across wide load range. So far, literatures mainly focus on addressing ACF efficiency with GaN, but the above critical and fundamental questions remain unclear. Secondly, since C_{oss} of both primary switches and synchronous rectifier (SR) are nonlinear as shown in Fig. 3(b), the analysis based on linear equivalent circuit in [8] cannot reflect the real switching behavior but more detail investigation is needed. Finally, the resonance natural of ACF makes the mathematical equations complex to describe the second-order system in many switching states, so it is difficult to generate analytical design procedure but relies on iterative numerical solutions [6][7]. Therefore, it is interesting to create a simplified analysis to benefit the design optimization.

II. Design Guide on ZVS Control for Q_L and Q_H

As shown in Fig. 4, both rising and falling edge of V_{sw} can be greatly affected by the capacitance nonlinearity. For GaN FET, C_{oss} is less nonlinear, so V_{sw} transition is close to first-order change. For Si FET, three different slopes are observed on the V_{sw} waveform, which exhibits a shallow slope at beginning, becomes a sharper edge, and then returns back to a shallow slope at the end. The upper flat region is mainly contributed by the high capacitance region of Q_H C_{oss} curve and partly from the junction capacitance of output rectifier, while the lower flat region majorly comes from the high capacitance region of Q_L C_{oss} curve.

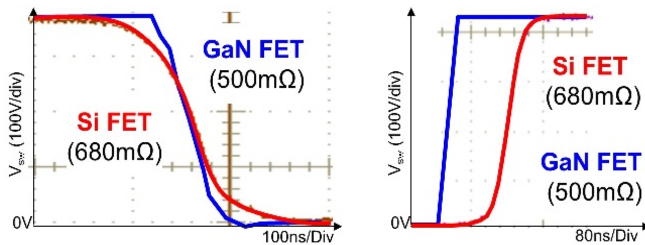

Fig. 4. Comparison of V_{sw} transition between Si FET and GaN FET

A. C_{oss} Impact and Guidelines for Achieving ZVS on Q_L

The first system impact is that Si FET requires much longer dead time waiting for the falling-edge voltage transition to 0V than using GaN FET, so the resulting duty cycle loss limits higher f_{sw} operation. The second impact is that more $i_{m(-)}$ is needed to overcome the two high capacitance regions on the falling-edge of V_{sw}. It is found that a proper C_{clamp} selection helps to reduce the impact of upper flat area on V_{sw}. Fig. 5 compares the simulation results of a Si-based ACF with two C_{clamp} values. A smaller C_{clamp} design of 100nF makes the resonance clamp current finished before Q_H turns off. In this case, $i_{m(-)}$ is the only current source to discharge the high capacitance region of Q_H. On the other hand, if C_{clamp} can be increased to a point that, 600nF as example, the resonance cannot be completed at the end of Q_H off time, the negative clamp current ($i_{clamp(-)}$) becomes an extra current source to discharge the high capacitance region of Q_H C_{oss} curve, besides of $i_{m(-)}$. With that, not only the time spend on upper flat area is shortened, but also $i_{m(-)}$ is reduced, from -0.9A to -0.8A in this case. Energy-balance equation in (1) is another prospective to understand this effect, where ZVS criteria contains not only a part of L_m energy from $i_{m(-)}$, but also a part of L_k energy from $i_{clamp(-)}$. Although Q_H and secondary rectifier does not turn off at zero current condition for the 600nF case, the turn-off loss of Si FET does not grow as fast as GaN FET, since the high-capacitance region of Q_H slows down the growth of its drain-to-source voltage during turning off Q_H.

$$\frac{1}{2}L_m i_{m(-)}{}^2 + \frac{1}{2}L_k i_{clamp(-)}{}^2 \geq \frac{1}{2}C_{sw}V_{ds}{}^2 \qquad (1)$$

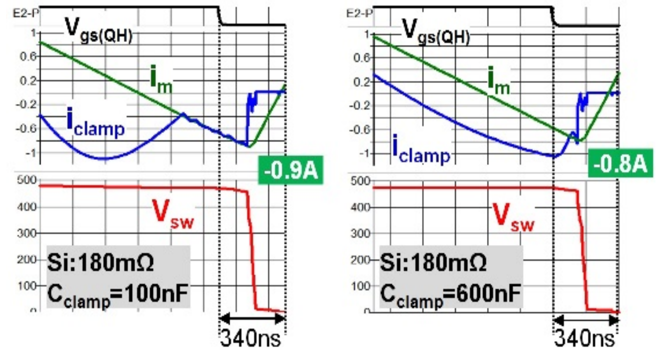

Fig. 5. Effect of different C_{clamp} value on the ZVS energy of Si-based ACF

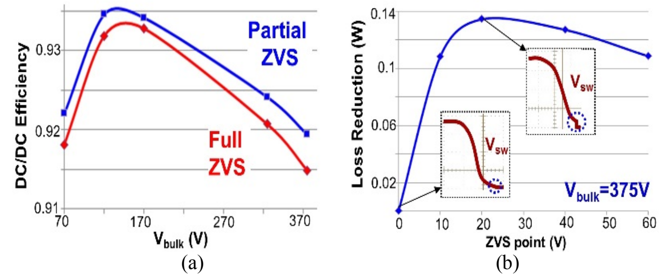

Fig. 6. Partial ZVS on a 30W Si ACF: (a) efficiency comparison with full ZVS, (b) total loss reduction under different partial ZVS points

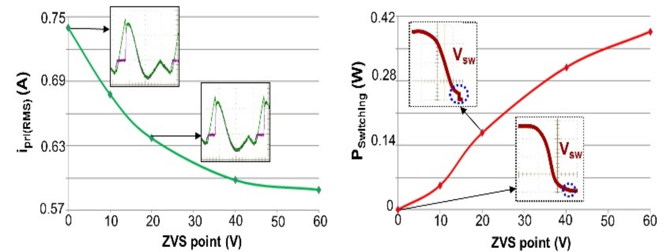

Fig. 7. Loss tradeoff under different partial ZVS points on a 30W Si ACF

Moreover, proper turn-on point of Q_L helps to reduce the impact of lower flat area on V_{sw}. As C_{oss} curve of Si FET in Fig. 3(a) indicates, if the ZVS target is to turn on Q_L by waiting for V_{sw} to reach to 0V, a large $i_{m(-)}$ is required to discharge the high capacitance region. If it is possible to turn on Q_L at a given V_{sw} voltage before C_{oss} starts to grow rapidly, $i_{m(-)}$ can be significantly reduced. This technique is called partial ZVS in this paper. The efficiency test results in Fig. 6(a) demonstrates that performing partial ZVS at 20V further improves 0.5% on the full-load efficiency of a 30W charger using two 680mΩ Si FETs on primary side. Fig. 6(b) shows a more detail study on where the optimal partial ZVS target is. From total loss reduction respective to the ZVS point moving from 0V to 60V, the result indicates that 20V obtains biggest loss reduction, but the loss reduction is into diminishing return as the partial ZVS point is higher than 20V. This effect can be understood from the design trade-off between RMS current reduction and turn-on switching loss increment, as shown in Fig. 7. As the partial ZVS point moves higher, the RMS current on the primary winding ($i_{pri(RMS)}$) still keeps reducing. However, partial ZVS point means hard switching point of Q_L, so the turn-on switching loss grows at the same time. Since the turn-on loss of Si FET can increase rapidly after 10V, the conduction loss reduction will be gradually washed out by the switching loss increasing. Therefore, this indicates 10~20V is suitable for a Si FET which turn-on loss grows rapidly above the voltage range, while full ZVS is best for GaN FET.

B. *C_{oss} Impact and Guidelines for Achieving ZVS on Q_H*

Similar to the falling-edge behavior, the rising edge also contains the asymmetric voltage transition due to the C_{oss} nonlinearity, as shown in Fig. 4. Basically, $i_{m(-)}$ is served to discharge C_{sw} on V_{sw} falling edge, while peak magnetizing current ($i_{m(+)}$) charges C_{sw} on V_{sw} rising edge. Since $i_{m(+)}$ is higher than $i_{m(-)}$ at heavy load condition, the lower and upper flat regions on the rising edge are less obvious than the falling edge. However, with lighter output load, $i_{m(+)}$ has to be reduced to keep output regulation. Then, the impact on the dead time control between Q_L off and Q_H at light load is still challenging. Specifically, after Q_L turns off, if Q_H does not turn on after V_{sw} is settled to high level, Q_H will lose ZVS which results in higher turn-on switching loss. On the other hand, if Q_H turns off too late with a conservative fixed dead time design, the body diode loss of Si FET or the reverse conduction loss of GaN FET can contribute additional conduction loss increase.

C. *Benefits of Adaptive ZVS Control*

Based on the above understanding on ZVS optimization, it is ideal for an ACF controller to be equipped with an on-line auto-tuning feature, which response is based on the real-time switching characteristic of V_{sw}, in order to eliminate any risks of losing ZVS and suffering significant efficiency drop due to all possible parameter variations in the system, no matter where they come from the input/output voltage change, the component tolerance, and the C_{oss} nonlinearity. Fig. 8 indicates the critical requirement of the ideal control scheme. Firstly, the control signal of peak current loop (V_{CST}) determines the turn-off instance of Q_L, so the peak magnetizing current can be adjusted through a feedback loop for output regulation. Secondly, in order to achieve ZVS on Q_H, the controller should intelligently vary the delay time ($T_{D(L\text{-}H)}$) from the turn-off instance of Q_L to the turn-on instance of Q_H based on the replicated signal of V_{sw} high-voltage region from a lossless observer. Thirdly, the controller should dynamically change the turn-off instance of Q_H based on the sensing signal of V_{sw} low-voltage region from the lossless observer. Through varying the on time of Q_H gradually cycle-by-cycle, the control loop can help ACF to accumulate just enough $i_{m(-)}$ for turning on Q_L at a target full/partial ZVS point within a given delay time ($T_{D(H\text{-}L)}$).

The lossless observer feeds cycle-by-cycle switching characteristic to the controller for maintaining ZVS of both primary switches. Specifically, after Q_L off, it senses the instance when the rising edge of V_{sw} overcomes the nonlinear region by comparing with a ZVS voltage threshold (V_{th1}), so as to advice the optimal turn-on point of Q_H. Moreover, after Q_H off, the observer compares the sensed V_{sw} with another ZVS voltage threshold (V_{th2}), such that the tuning direction and step size for the Q_H on-time adjustment of next switching cycle can be determined. The ZVS control scheme is implemented into a new ACF controller from Texas Instruments, UCC28780, embedded with a novel lossless observer [12]. V_{th2} can be programmed close to 10V for Si FET for partial ZVS, and set close to 0V for GaN FET to lock into full ZVS. With those features, ACF can be anchored at highest efficiency condition.

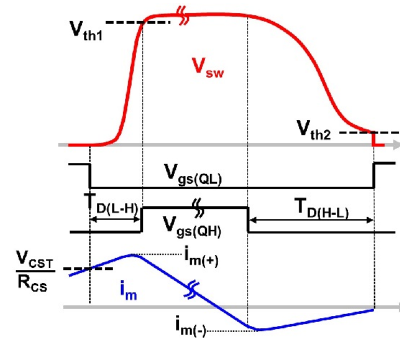

Fig. 8. Concept of the ZVS optimization in UCC28780

III. Design Guide on Minimizing Resonance Current

Actually, C_{sw} is not only contributed from the C_{oss} of two primary switches, but also from junction capacitance of the secondary rectifier, either a schottky diode or a synchronous rectifier (SR). The measurement result from a 30W ACF charger in Fig. 9 compares the switching current waveforms with the four combinations of different primary switches (680mΩ Si and 500mΩ GaN) and different 150V secondary-rectification devices. When a schottky diode is used as the rectifier, the shape of switching current waveform between GaN and silicon FET is similar, and the main difference is just the different pk-to-pk and RMS current levels. On the other hand, when a 150V/28mΩ SR is used as the rectifier, the shape of current waveform becomes significantly different.

For a Si FET as the two primary switches and a Si SR as the rectifier, there is only a small current dip on i_{pri} before the resonance of i_{clamp} starts. Then, the RMS current difference between using a schottky diode and the SR is not much, since the current dip effect on RMS current is almost negligible. On the other hand, for a GaN FET as the two primary switches

and a Si SR as the rectifier, a big current dip reduces the initial peak resonance current of i_{clamp} and significantly lowers RMS current, compared with using a schottky diode. In this example, 34% reduction on RMS current with this current dipping effect benefits both the primary-winding loss reduction and the conduction loss reduction of Q_H. The 30W full-load efficiency measurement in Fig. 10 indicates 2.5% improvement across wide line range, as a diode rectifier is replaced by a 150V/28mΩ SR. Although lower-$R_{ds(on)}$ FET on SR results in bigger current dipping, the RMS-related loss reduction could be washed out by higher driving loss with the larger gate charge and higher core loss with increased $i_{m(-)}$ to discharge the larger C_{oss} loading. Then, the efficiency test using 150V/14mΩ FET ends up similarly. Besides, this efficiency boost cannot be seen in silicon-based ACF with SR, since the current dipping effect is lost by the high capacitance region of Q_H. Generally, according to the faraday's law in equation (2), the current dip phenomenon on primary current, i.e. a di/dt current change on i_{pri}, can be understood by examining the voltage change across L_k, which is the voltage difference between the reflected voltage from secondary winding (NV_{sec}) and the voltage across the transformer primary winding (V_{pri}), as shown in Fig. 1.

$$\frac{di_{pri}}{dt} = \frac{1}{L_k}(NV_{\sec} - V_{pri}) \tag{2}$$

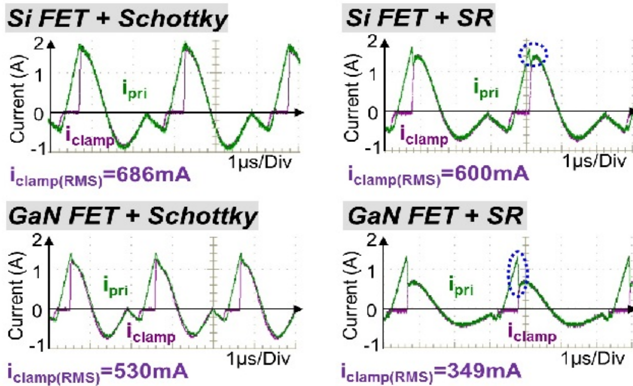

Fig. 9. Impact of switching device selection on resonance current

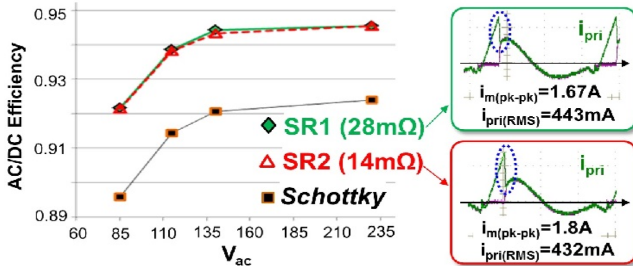

Fig. 10. Efficiency impact from C_{oss} nonlinearity of SR to GaN-based ACF

The negligible current dipping for silicon-based ACF with SR is explained as follows. Since SR is off as the current dipping occurs, NV_{sec} is equal to the voltage difference between the drain-to-source voltage on SR FET and V_o. Similarly, since Q_H is off as well, V_{pri} is equal to the voltage difference between the drain-to-source voltage of Q_H and V_{clamp}. Since both sides use Si FETs, the C_{oss} are highly dependent to V_{ds}. Fig. 3(b) compares the C_{oss} nonlinearity between the $C_{oss(QH)}$ of 600V/680mΩ Si FET and the $C_{oss(SR)}$ of 150V/28mΩ Si SR reflected to primary side. The result shows that there is a certain higher V_{ds} range where $C_{oss(QH)}$ is smaller than the reflected capacitance from SR ($C_{oss(SR)}/N^2$), and there is another lower V_{ds} range where $C_{oss(QH)}$ is significantly larger than $C_{oss(SR)}/N^2$. When peak i_m ($i_{m(+)}$) starts to discharge both, this capacitance difference creates different rising slopes on V_{pri} and NV_{sec}, as the simulation result shows in Fig. 11. In the first portion, V_{pri} rises faster than NV_{sec}, since $C_{oss(QH)}$ is smaller. In the second portion, V_{pri} rises much slower than NV_{sec}, since $C_{oss(QH)}$ becomes much larger. The rising slope variation causes a different voltage polarity across L_k in equation (2). In the first portion, the voltage across L_K is negative, so the di_{pri}/dt is negative. In the second portion, the voltage across L_k becomes positive, so the di_{pri}/dt becomes positive. This explains why current dip occurs at beginning and disappears afterward in Fig. 9. Losing the current dipping effect, the initial resonance current is almost equal to $i_{m(+)}$. Then, the benefit of SR for Si-based ACF is mainly the reduction of the conduction loss on the secondary rectifier.

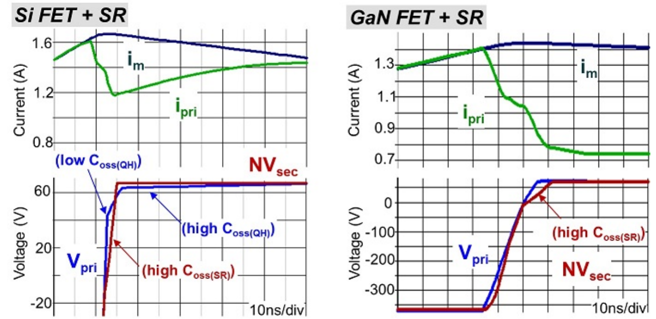

Fig. 11. Winding voltage difference and current dipping on V_{sw} rising edge

For GaN FET, the current dip is more significant, which reduces the initial resonance clamp current. This effect can also be explained by the C_{oss} difference in Fig. 3(b), which shows that $C_{oss(QH)}$ of GaN is always smaller than $C_{oss(SR)}/N^2$ across all V_{ds} range. Therefore, as $i_{m(+)}$ starts to discharge both capacitances, the rising slope of V_{pri} is always higher than NV_{sec}. With that, the voltage polarity across L_K in equation (2) stays negative, which forces di_{pri}/dt to stay negative before resonance starts. In this case, Si SR for GaN-based ACF not only reduces the conduction loss on secondary rectifier, but also benefits the conduction loss reduction on both Q_H and primary-winding of transformer. Simply speaking, a win-win situation is obtained for both primary and secondary sides.

IV. Design Guide to Maximize Light Load Efficiency

The light load efficiency of ACF is also very sensitive to C_{oss} nonlinearity. As load current becomes lighter, the peak current-mode control loop reduces positive peak current ($i_{m(+)}$) to regulate output power, while the negative magnetizing current ($i_{m(-)}$) stays the same in the same V_{bulk} condition. $i_{m(+)}$ delivers active energy to output, while $i_{m(-)}$ stores the circulating energy to achieve ZVS. If $i_{m(+)}$ and $i_{m(-)}$ become more and more comparable as load becomes lighter, it means that the transformer efficiency becomes worse, since the

contribution of the circulating energy is getting higher. For Si-based ACF with highly nonlinear C_{oss}, $i_{m(-)}$ is larger especially at high line, so the high-line efficiency is deteriorated very quickly in lighter load. Fig. 12 compares the light-load efficiency of Si and GaN-based ACF with secondary schottky diode in 30W design. For the Si-based ACF, the efficiency difference between 50% load and 25% load is as high as 7.3% at high line. For GaN-based ACF, $i_{m(-)}$ is much lower with its low C_{oss}, so the $i_{m(-)}$ impact is less severe in lighter load, which results in only 2.6% efficiency difference in the same condition. Therefore, it is important to study a proper light-load control to maintain the average efficiency above the CoC and DoE standards. Conceptually, the most critical requirement of the ideal light load mode for ACF is to preserve $i_{m(+)}$ to be relatively higher than $i_{m(-)}$. Then, the question is how to maintain regulation of the output voltage if a certain $i_{m(+)}$-to-$i_{m(-)}$ ratio would like to be maintained.

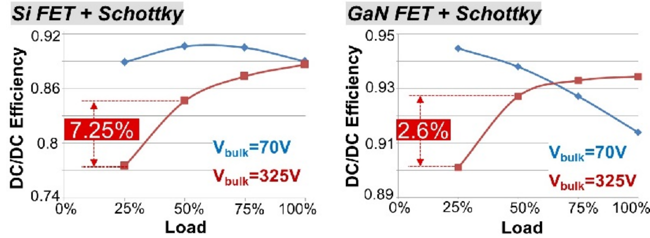

Fig. 12. Light load efficiency drop with peak current control only

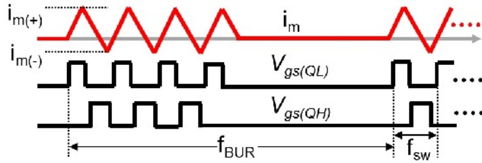

Fig. 13. Proposed switching pattern for burst mode operation

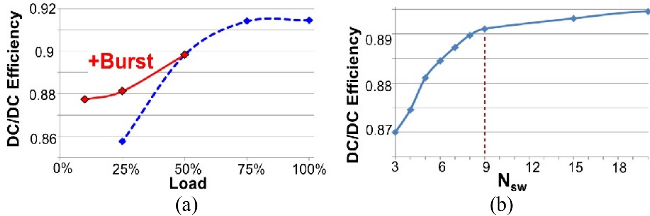

Fig. 14. Efficiency of Si ACF with burst mode: (a) vs. load, (b) vs. N_{sw}

Therefore, the burst mode control is recommended in this paper to meet this goal, and the switching pattern is shown in Fig. 13. $V_{gs(QL)}$ is set as the first pulse to build up the bootstrap voltage of high-side driver first before Q_H starts switching, and the first $V_{gs(QL)}$ pulse turns on Q_L on the valley point of DCM ringing. The following pulses operate in ZVS condition, since $V_{gs(QH)}$ is enabled. Furthermore, $V_{gs(QH)}$ of the last pulse is purposely disabled to prevent generating unnecessary $i_{m(-)}$ to trigger large DCM resonance between L_m and C_{sw}, since the excessive ringing can create additional core loss. The output power regulation is based on modulating the burst off time, as the energy per switching cycle in a burst packet is fixed, i.e. $i_{m(+)}$ is fixed and is chosen at a certain current level which provides a reasonable $i_{m(+)}$-to-$i_{m(-)}$ ratio. After the last pulse per burst packet is ended, $V_{gs(QL)}$ and $V_{gs(QH)}$ are completely off to terminate the power delivery. As the load becomes lighter, the burst off time becomes longer before next burst event. The test result at V_{bulk}=200V in Fig. 14(a) shows that after the burst control takes over the load regulation below 50% load, the efficiency drop becomes moderate. Besides, the additional benefit of the burst mode is limiting f_{sw} variation for less driving loss. Based on the transition-mode operation, lowering $i_{m(+)}$ in lighter load results in f_{sw} growth, so the driving losses increases. When the burst mode is applied below 50% load, the fixed $i_{m(+)}$ limits f_{sw} from increasing. Furthermore, the number of pulses per packet is defined as N_{sw}. The test result in Fig. 14(b) shows that as N_{sw} increases (more grouped pulses), the efficiency at 25% load becomes higher. However, more grouped pulses mean higher burst output ripple (ΔV_o). Also, higher N_{sw} makes the burst frequency (f_{BUR}) entered into the audible noise range at heavier load, and equation (3) is derived to estimate how f_{BUR} varies with output load and N_{sw}. The ratio of i_o and $i_{o(BUR)}$ indicates lighter i_o results in lower f_{BUR}, where $i_{o(BUR)}$ is the predetermined output load condition starting to burst and i_o is the lighter load condition lower than $i_{o(BUR)}$. Another dependency of this equation is N_{sw} and f_{sw} of each pulse. In other words, as N_{sw} is higher, f_{BUR} will be further reduced as well.

$$f_{BUR} = \frac{i_o}{i_{o(BUR)}} \frac{f_{sw}}{N_{sw}} \tag{3}$$

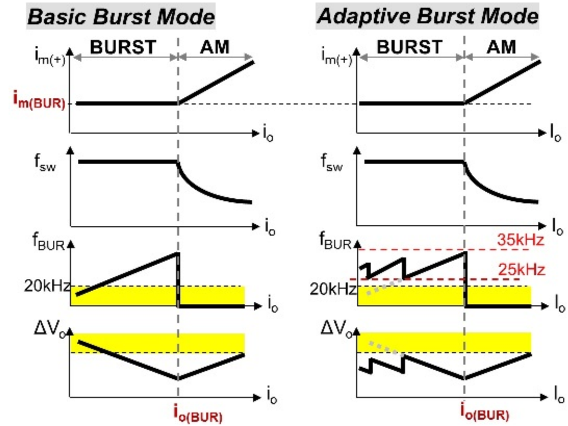

Fig. 15. Advantage of adaptive burst mode in UCC28780

The critical parameter change over wide load range with basic burst mode control is summarized in Fig. 15. At heavier load, $i_{m(+)}$ is gradually reduced by a peak current loop as the load decreases, so f_{sw} increases. This region is defined as AM operation (amplitude modulation). In AM, the burst mode has not started yet, so f_{BUR} is 0Hz. Besides, lower $i_{m(+)}$ reduces the switching-frequency ripple on ΔV_o, so the worst-case ΔV_o in AM always occurs at full load condition. After $i_{m(+)}$ is reduced to a predetermined peak current threshold ($i_{m(BUR)}$), the burst mode control starts to clamp $i_{m(+)}$ to this level, so f_{sw} is clamped at the same time. Then, f_{BUR} starts to move into lower frequency range as i_o reduces. When more pulses are grouped, the control loop enters burst operation at heavier loading. It is possible that when f_{BUR} falls into the audible noise range (below 20kHz), the transformer can generate disturbing noise. Additionally, the burst-ripple content on ΔV_o increases with more grouped pulses. It is possible that if N_{sw} is not properly

selected, the worst-case ΔV_o can occur at very light load condition but not full load condition in AM, which enlarges the output capacitor size to meet the output ripple requirement. To maximum the light-load efficiency without audible nose issue and over-sizing output capacitor, the unique burst mode operation in UCC28780 dynamically modulates N_{sw} based on comparing f_{BUR} with two frequency thresholds, as shown in Fig. 15 [12]. Specifically, as f_{BUR} < 25kHz is detected for current burst cycle, the number of both gate control signals in next burst cycle is reduced by one pulse to push f_{BUR} above 25kHz. When N_{sw} drops with load reduction, the burst-frequency ripple on ΔV_o reduces as well. On the other hand, N_{sw} will be increased by one, when f_{BUR} > 35kHz is identified.

V. Circuit Analysis Including Nonlinear C_{oss}

A. Analytical Expression of ACF Operating Condition

The technique of triangular approximation is proposed to model the magnetizing current waveform of transition–mode ACF around the V_{sw} transition, as shown in Fig. 16. Then, the analytical expression of switching frequency (f_{sw}) and input power (P_{in}) can be easily derived from the triangular waveform. First of all, by averaging the current waveform of low-side switch (i_{QL}), the input current of ACF is expressed as

$$i_{in} = \int_0^{1/f_{sw}} i_{QL}(t)dt = \frac{1}{2}[i_{m(+)}T_r + i_{m(-)}T_{m(-)}]f_{sw} \quad (4)$$

where T_r is the rising time of i_m from 0A to $i_{m(+)}$ and $T_{m(-)}$ is the transition time from $i_{m(-)}$ to 0A. With the triangular approximation, T_r is substituted with $i_{m(+)}L_m/V_{bulk}$, and $T_{m(-)}$ is approximated as $-i_{m(-)}L_m/V_{bulk}$. Next, the input power equation can be derived and simplified as

$$P_{in} = V_{bulk} \cdot i_{in} = \frac{1}{2}L_m f_{sw}[{i_{m(+)}}^2 - {i_{m(-)}}^2] \quad (5)$$

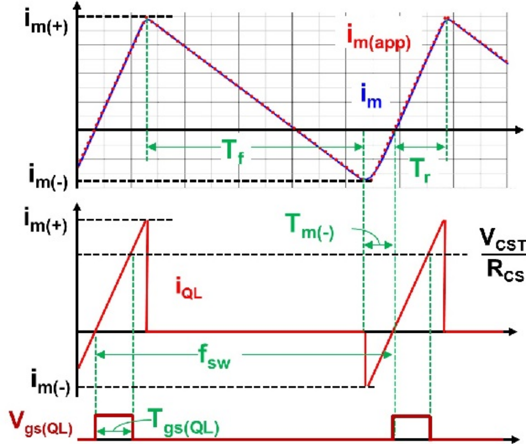

Fig. 16. Proposed approximation on ACF current waveforms

Since this equation shows that $i_{m(+)}$ needs to be increased to provide the same power as more $i_{m(-)}$ is needed for ZVS, the physical meaning is that ACF transformer stores $i_{m(+)}$ as active energy for power delivery, but $i_{m(-)}$ is like a reactive energy. After that, the f_{sw} expression in equation (6) can be obtained based on the sum of T_r, $T_{m(-)}$, and the demagnetizing time from $i_{m(+)}$ to $i_{m(-)}$ (T_f), which is $(i_{m(+)}-i_{m(-)})L_m/V_{bulk}$.

$$f_{sw} = \frac{1}{T_r + T_f + T_{m(-)}} = \frac{D^2 V_{bulk}}{2i_{in}L_m - Di_{m(-)}L_m + DT_{m(-)}V_{bulk}} \quad (6)$$

where D is not the duty cycle of Q_L on time but is calculated from the volt-second balance of i_m. Then, D can be defined as

$$D = \frac{T_r + T_{m(-)}}{T_r + T_{m(-)} + T_f} = \frac{NV_o}{V_{bulk} + NV_o} \quad (7)$$

The Q_L on time starts at 0A of i_{QL} and ends at the intersection with a current threshold (V_{CST}/R_{CS}), controlled by a peak current loop comparing with the current-sense signal on the sensing resistor (R_{CS}). Since the high C_{oss} region of Si FET on Q_L creates additional peak current overshoot after the gate turns off, the actual turn-off instance ends earlier before i_m reaches to highest level, as shown in Fig. 16. The Q_L on time including the C_{oss} effect for V_{ds} < 20V is approximated as

$$T_{gs(QL)} \approx \sqrt{{T_r}^2 - 2\frac{Q_{oss(20V)}L_m}{V_{bulk}}} \quad (8)$$

where $Q_{oss(20V)}$ is the stored C_{oss} charge from 0V to 20V of V_{ds}.

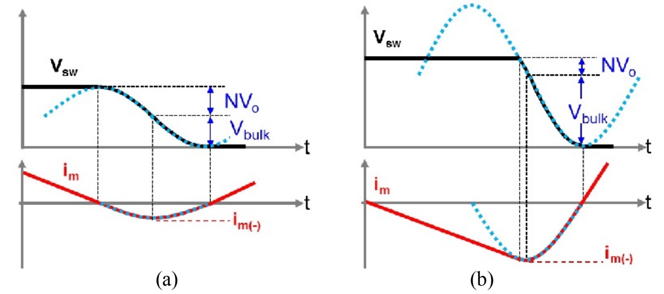

Fig. 17. Resonance during V_{sw} falling edge: (a) $V_{bulk} \le NV_o$, (b) $V_{bulk} > NV_o$

As long as analytical expressions of $T_{m(-)}$ and $i_{m(-)}$ can be obtained, the above equations can be used to calculate the operating condition of ACF and determine L_m of transformer. Since the small $i_{m(-)}$ flowing through L_m changes during discharging C_{sw}, L_m cannot be treated as a constant current source, but a part of second-order tank circuit with C_{sw} to obtain more actuate expressions. Starting from $V_{bulk} \le NV_o$ condition, Q_H can turn off at zero-crossing of i_m, since the voltage swing of the natural resonance between L_m and C_{sw} is enough to bring V_{sw} down to 0V. Based on the waveforms shown in Fig. 17(a), $i_{m(-)}$ can be derived based on the characteristic impedance (Z_n) and the resonance voltage amplitude of NV_o, while $T_{m(-)}$ is a quarter of resonance period. In this condition, the overall V_{sw} transition takes half of resonance period to complete. On the other hand, as V_{bulk} > NV_o, Q_H has to turn off later than the zero-crossing of i_m, in order to create large enough $i_{m(-)}$. Then, as shown in Fig. 17(b), the initial resonance current between L_m and C_{sw} is not zero, so the voltage swing does not start from the peak of sinusoidal trajectory but starts close to a quarter of the resonant period. For this case, $i_{m(-)}$ can be derived based on Z_n and the resonance voltage amplitude of V_{bulk}, while $T_{m(-)}$ is

still a quarter of the resonance period. Based on the above understanding, the analytical expressions of $T_{m(-)}$ and $i_{m(-)}$ under a wide V_{bulk} range are summarized as

$$i_{m(-)} = \begin{cases} -V_{bulk} / Z_n & ,if \quad V_{bulk} > NV_o \\ -NV_o / Z_n & ,if \quad V_{bulk} \le NV_o \end{cases} \tag{9}$$

$$T_{m(-)} = 0.5\pi\sqrt{L_m C_{sw}} \tag{10}$$

where $Z_n = \sqrt{L_m / C_{sw}}$, and C_{sw} is quantified in the next part.

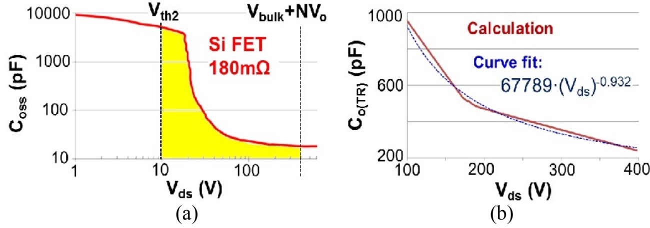

Fig. 18. $C_{o(TR)}$ calculation: (a) integrating C_{oss} curve on datasheet, (b) curve fit

B. Analytical Expression of Switch-node Capacitance

Lumped time-related capacitance (C_{sw}) is the sum of the time-related capacitance ($C_{o(TR)}$) of active switches, winding capacitance of transformer, and the junction capacitance of bootstrap diode. However, the first challenge of calculating C_{sw} is that C_{oss} of the active switches is very nonlinear and voltage dependent, as illustrated in Fig. 3. The second challenge is that the device datasheets do not provide enough data points for the equivalent time-related capacitance under different V_{ds}. For example, a primary 600V silicon super-junction FET only lists an equivalent time-related C_{oss} at V_{ds} of 400V, while the datasheet of a 150V SR FET does not even list any. The third challenge is that as the partial ZVS control is applied, the value on the datasheet cannot be used, since it assumes a V_{sw} transition between 400V to 0V. Therefore, this paper provides a simple calculation method and a useful generalized expression for the time-related capacitance under arbitrary V_{ds} of each device, as expressed in equation (11).

$$C_{o(TR)}(V_{ds}) = \frac{1}{V_{ds} - V_{th2}} \int_{V_{th2}}^{V_{ds}} C_{oss}(V)dV \approx X \cdot V_{ds}^{\ Y} \tag{11}$$

The assumption is that there is no hysteresis loss effect on the C_{oss} curve mentioned in [10] and [11], so $C_{o(TR)}$ of each switches can be directly calculated through its C_{oss} curve on the datasheet. The first step is integrating the C_{oss} curve from the partial ZVS point (V_{th2}) to a variable V_{ds}, which is sum of V_{bulk} and NV_o. Specifically, the integration is done by discretizing the C_{oss} curve, calculating the area of each segment, and then summing the areas together. Finer segments should be applied to the region with large C_{oss} change. The second step is dividing the integrated expression by the voltage difference between V_{ds} and V_{th2}, so the $C_{o(TR)}$ can be plotted as the brown-solid curve on Fig. 18(b). The third step is curve fitting the numerical values into proposed analytical form, which is a logarithmic trend-line equation with two variables, X and Y. The two variables can be easy calculated by the plotting tool in EXCEL.

VI. Experimental Verification

One of the high-density ACF hardware to support the study of the paper is shown in Fig. 19, which is also the evaluation board of UCC28780 ACF controller. For the GaN-based ACF hardware, a 650V half-bridge GaN FET with integrated driver from Navitas Semiconductor is used. For the Si-based ACF hardware, a half-bridge driver, UCC27712, is chosen to control two 600V Si FETs. UCC24612 controller is selected to drive the 150V SR FET in both Si and GaN ACF.

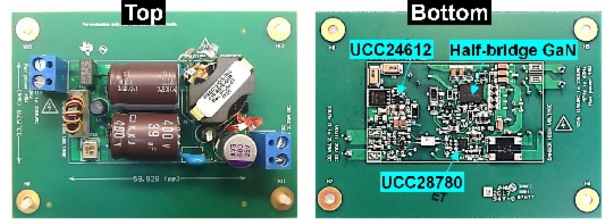

Fig. 19. UCC28780 evaluation board as the GaN-based ACF hardware

A. Verification on Adaptive Burst Mode Control

Fig. 20 shows the test results from the 45W GaN-based ACF hardware to demonstrate the high-efficient and audible-noise-free burst mode of UCC28780. The hardware is programmed to enter into the burst mode at around 60% load. The controller generates 7 pulses at 50% load, 5 pulses at 25% load, and 3 pulses at 10% load, while remains moderate efficiency drops on those load condition. The four-point average efficiency is 94.2% at $115V_{AC}$ and 93.6% at $230V_{AC}$.

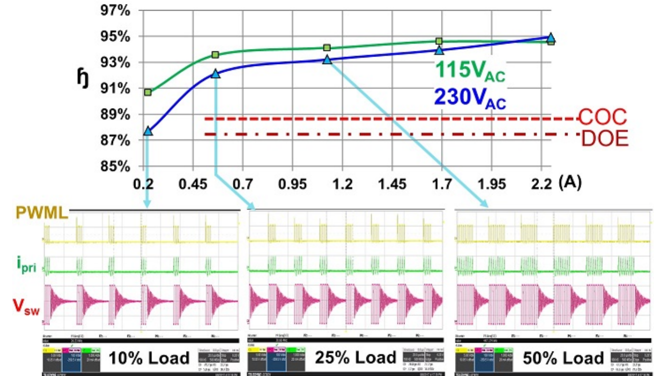

Fig. 20. Light load efficiency and operation with adaptive burst mode

B. Verification on Adaptive ZVS Control

Fig. 21 shows the test results from a 30W Si-based ACF hardware to demonstrate the auto-tuning feature of UCC28780, which helps ACF locked into partial ZVS quickly during V_o startup. At the beginning, as the ZVS observer cannot detect V_{sw} reaching V_{th2} within a given 400ns timeout of $T_{D(H-L)}$, UCC28780 will increase Q_H on time gradually on the next switching cycle. After ZVS is achieved, Q_H on time will reduce a bit to check it fails to reach V_{th2} or not, so as to ensures the loop settled at lowest $i_{m(-)}$ situation. In steady state, the actuator will toggle around its least significant bit (LSB). Since the controller enters into fine tune state automatically, the LSB effect is very small, and the test results in Fig. 22 shows every switching cycle stays around the partial ZVS target of 9V.

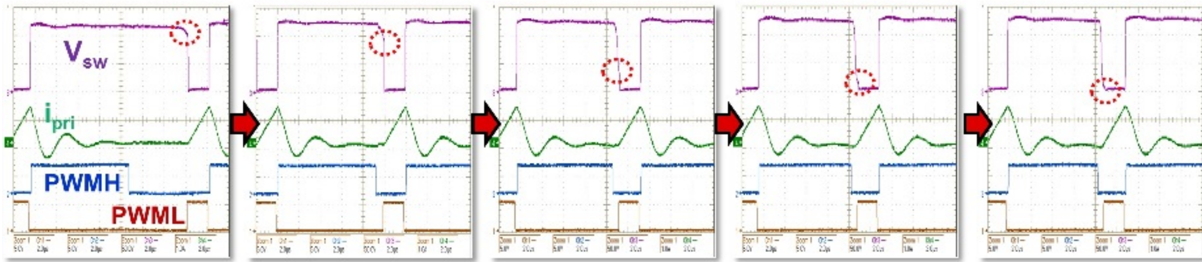

Fig. 21. ZVS auto-tuning process during output voltage startup

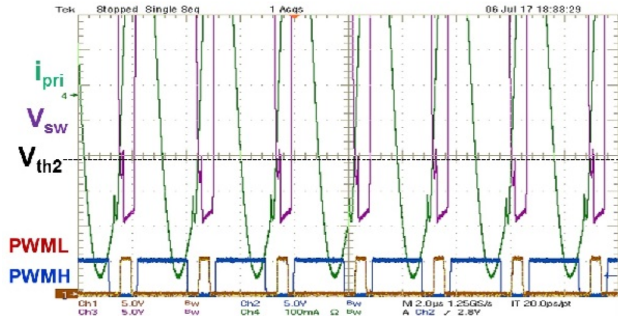

Fig. 22. ZVS auto-tuning in steady state

C. *Efficiency Comparison on GaN and Si-based ACF*

The design constraints are the same $f_{sw(min)}$ of 180kHz at $V_{bulk(min)}$=75V, N=3.25, V_o=20V, P_o=30W, a RM6 Litz-wire transformer with 3F36 core, and 150V SR (BSC360N15NS3). Based on the expressions in section V and the above design target, L_m is 85μH for Si ACF and 95μH for GaN ACF. The measurement results on primary RMS current and full-load efficiency of the two power stage designs are compared in Fig. 23. The significant $i_{pri(RMS)}$ reduction on the primary winding with GaN is contributed by not only the low peak-to-peak i_m, but also the current dipping effect explained in section III. In the end, GaN-based ACF do provides superior efficiency over optimized Si-based ACF. The difference of 2% at low line and 3% at high line is the efficiency of DC/DC stage only. As the input stage (including EMI filter, bridge diode, fuse, etc.) is included, the efficiency difference will be higher.

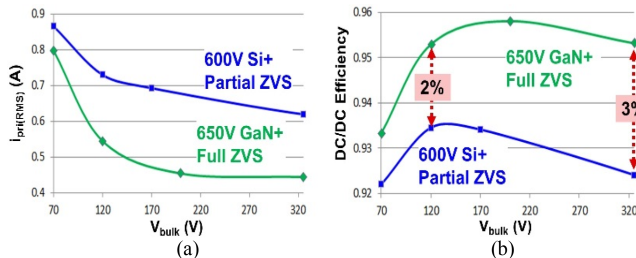

Fig. 23. Comparison between GaN and Si ACF: (a) RMS loss, (b) efficiency

VII. CONCLUSION

This paper provides compressive analysis on how C_{oss} nonlinearity from primary and secondary switching devices impacts the switching behavior and system efficiency of the ACF across the wide load range. It is found that the superior performance of GaN-based ACF is not just contributed by ultralow C_{oss}, but also the current dipping effect through the nonlinear C_{oss} effect of SR. Solutions to minimize the C_{oss} nonlinearity impact from the two Si primary switches are also investigated to reduce the efficiency gap with GaN design. The proper clamp capacitor design, partial ZVS control for soft switching Q_L, and dead-time control for soft switching Q_H are addressed. Besides, burst-mode control is proposed to exhibit greater average efficiency. The benefits of adaptive control on both ZVS auto-tuning and burst operation are identified and verified on a new ACF controller. Besides, analytical equations are derived to simplify power stage design, accounting for all C_{oss} nonlinearity. Finally, based on proposed design procedure, two ACF designs with state-of-the-art GaN and Si FETs are developed and the optimal performances are compared.

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