Study on Reducing Switching Current in Dual Bridge Series Resonant DC/DC Converter

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***Abstract*—Dual bridge series resonant DC/DC converter (DBSRC) usually works at continuous current mode (CCM), whose switching frequency is set higher than resonant frequency. Thus, soft switch-on and soft switch-off of power switch cannot be realized simultaneously with no extra snubber circuit connected. And the primary measure to reduce switching losses is to reduce the switching current of power devices. The commutations of DBSRC in different conditions are analyzed in this paper and the values of switch-on and switch-off current are derived from this model. From the view of reducing switching current, this paper gives a guideline to select the parameters of DBSRC correctly, including the voltage conversion ratio (*M*), the ratio between switching frequency and resonant frequency (*F*) and the characteristic impedance (Z_r). The simulation obtains the switching currents at different *F*, *M* and Z_r, whose results verify the effectiveness of theoretical analysis. And the experiment results prove a better system efficiency with a better selection of switching frequency.**

Keywords—Dual bridge series resonant DC/DC converter (DBSRC); modeling; switching current; voltage conversion ratio; characteristic impedance.

I. INTRODUCTION

High-frequency isolated bidirectional DC/DC converter is the core equipment of power electronic transformer (PET) and has a great influence on the system efficiency and reliability. Now the DC/DC converter used in PET includes dual-active-bridge (DAB) DC/DC converter and bidirectional LLC resonant DC/DC converter and so on. Phase-shift control is usually adopted in DAB, which is easy to realize and favorable to achieve module cascade [1]. However, due to the drawbacks of large current stress, circulating power and switching losses, DAB is restricted in high-frequency application. Bidirectional LLC resonant converter usually adopts variable frequency control, which can realize ZVS over a wide load range and improve the efficiency of system [2]. But the control target is output voltage and output power is uncontrolled , and thus bidirectional LLC resonant converter has the difficulty of module cascade, which is not suitable in PET.

Dual bridge series resonant DC/DC converter (DBSRC) adds a series resonant capacitor based on DAB and also adopts the phase-shift control. Thus, DBSRC combines the advantages of high efficiency and easy control. The first harmonic approximation method is usually used to model DBSRC [3-7]. Reference [3] first evaluates the influence of hardware parameters on the current and voltage stress and designs a prototype with a sort of optimized parameters. To reduce the current stress, the control strategy is optimized to obtain high efficiency in [4]. However, the model only considers the voltage source load, which is not suitable in resistive load. Reference [5] simplifies the topology of secondary H-bridge in DBSRC and extends the ZVS operation range, but it takes bidirectional power flow as a sacrifice. The different working modes of DBSRC are proposed in [7], but the boundaries of different working modes are incorrect. The above method that AC voltage in DBSRC is considered as the sinusoidal voltage may cause a certain error, whereas reference [8] has pointed out a method to describe the exact expression of resonant current and voltage. But a complete analysis for DBSRC using this method is not available in literature until now.

In this paper, the commutation of DBSRC under different working modes is analyzed and the expression of transformer primary current is derived from the model of DBSRC. The soft-switching condition is also discussed in section II, where the switching current is defined. The relationship between switching current and hardware parameters is analyzed in section III. To reduce the switching current, this paper gives a guideline to select the optimal parameters. Simulation obtains the switching current at different conditions on voltage source load in section IV, whose results are in good agreement of the theoretical analysis. The experiment results present an

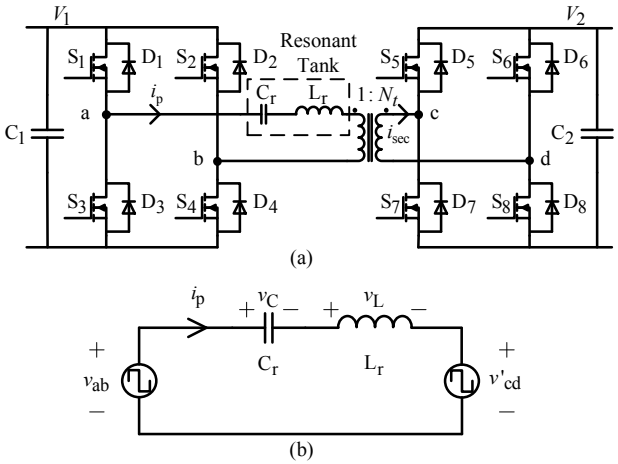

Fig. 1. (a) The topology of DBSRC; (b) The equivalent circuit of DBSRC.

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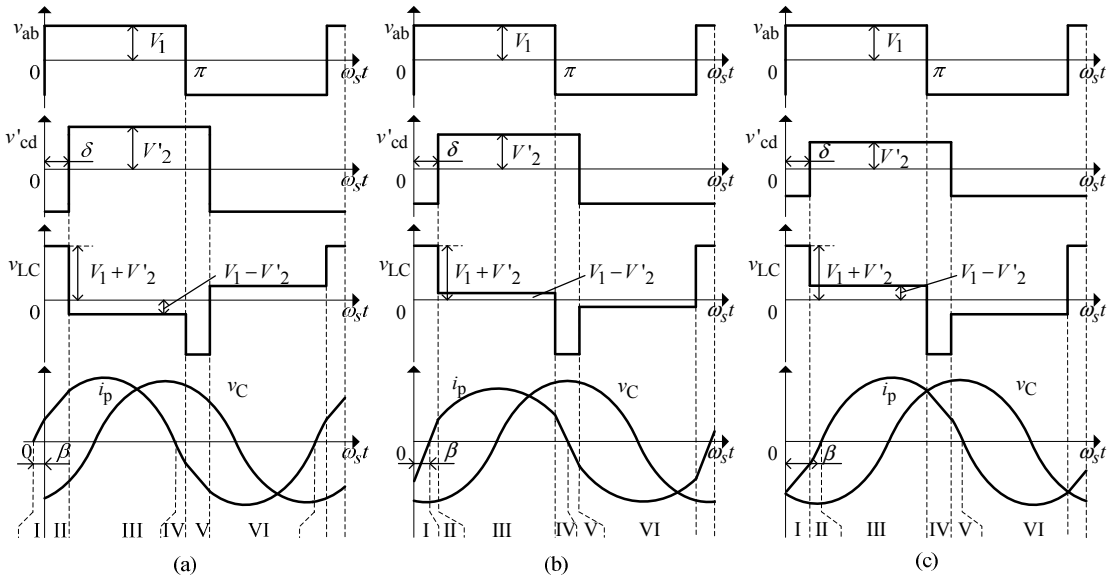

Fig. 2. The waveforms of different working modes in a switching cycle. (a) Mode I; (b) Mode II; (c) Mode III.

improved system efficiency with a better selection of switching frequency on the resistive load in section V.

II. WORKING PRINCIPLE OF DBSRC

The topology and equivalent circuit of DBSRC are shown as Fig.1 (a), which have been mentioned in [9]. The leakage inductance of high frequency transformer is used as the resonant inductor L_r, which forms the resonant tank together with a series capacitor C_r. Two H-bridges are connected through the resonant tank, and SiC-MOSFET half-bridge power modules are adopted to meet the requirements of switching speed and the capacity of voltage and current simultaneously in high-power application. Bidirectional power control can be realized in DBSRC. For the purpose of simplicity, assume that the left is source and the right is load.

The switching frequency (f_s) of power switches is set higher than the resonant frequency (f_r) of resonant tank to ensure the AC current to work at continuous current mode (CCM). Assume that all the components in the circuits are ideal and lossless, and the equivalent circuit is shown as Fig. 1(b). It is formed by two square sources with 50% duty circle and resonant tank, where v_{ab} is the AC voltage in primary H-bridge and $v'_{cd} = v_{cd}/N_t$ is the AC voltage in secondary H-bridge transferred to primary side. The active power is delivered through the phase difference between v_{ab} and v'_{cd}.

A. The Commutation and Modeling of DBSRC

According to the polarity of transformer primary current i_p in the phase-shift angle, DBSRC can be divided into three working modes, as illustrated in Fig. 2, where ω_s is the switching angular frequency; δ is the phase-shift angle; β is the phase angle when the polarity of i_p changes. And there are six intervals in a switching cycle for all working modes. For the convenience of description, the commutation of different intervals in Fig. 2(b) is selected and analyzed, and then the model of DBSRC is constructed.

Interval I ($\omega_s t \in [0, \beta]$): At the moment 0, the power switches S_2 and S_3 switch off, and i_p is forced to flow through the diodes D_1 and D_4, where the polarity of i_p does not change and v_{ab} changes to V_1. The switching-off losses of S_2 and S_3 emerge due to the hard-switching. The current in secondary side i_{sec} is still flowing through D_6 and D_7 and v'_{cd} remain $-V'_2$. Till the moment β, i_p reduces to 0 under the influence of external voltage $V_1-(-V'_2)$.

Interval II ($\omega_s t \in [\beta, \delta]$): At the moment β, i_p changes the polarity naturally. S_1 and S_4 start to carry current, and v_{ab} remains V_1. At the same time, with the alternation of i_p, S_6 and S_7 carry current, and v'_{cd} does not change until the moment δ.

Interval III ($\omega_s t \in [\delta, \pi]$): At the moment δ, S_6 and S_7 switch off, and is i_p still positive, and i_{sec} is forced to flow via D_5 and D_8. Thus, v'_{cd} changes to V_2 immediately. S_6 and S_7 bring in switching-off losses.

Interval IV to VI: The waveforms of AC voltage and current are periodically symmetrical, and the commutation in interval IV to VI is similar to interval I to III, which is not explained in detail here.

The time domain expression of current i_p and the voltage of resonant capacitance v_C are obtained through solving two second order differential equations from [9]. And the value of $i_p(\omega_s t)$ at the moment 0 and δ are shown as follows:

$$i_p(0) = -\frac{V_1}{Z_r}\left[M\sin\left(\frac{\delta}{F}\right) + \left(1 - M\cos\left(\frac{\delta}{F}\right)\right)\tan\left(\frac{\pi}{2F}\right)\right] \quad (1)$$

$$i_p(\delta) = \frac{V_1}{Z_r}\left[\sin\left(\frac{\delta}{F}\right) + \left(M - \cos\left(\frac{\delta}{F}\right)\right)\tan\left(\frac{\pi}{2F}\right)\right] \quad (2)$$

where $F = f_s/f_r$ is the ratio between switching frequency and resonant frequency and $F > 1$; $Z_r = \sqrt{L_r/C_r}$ is the

TABLE I. THE CURRENT PATHS OF DIFFERENT INTERVALS AT DIFFERENT WORKING MODES

Interval	Mode I	Mode II	Mode III
I	$D_2/D_3/S_6/S_7$	$D_1/D_4/D_6/D_7$	$D_1/D_4/D_6/D_7$
II	$S_1/S_4/S_6/S_7$	$S_1/S_4/S_6/S_7$	$D_1/D_4/S_5/S_8$
III	$S_1/S_4/D_5/D_8$	$S_1/S_4/D_5/D_8$	$S_1/S_4/D_5/D_8$
IV	$D_1/D_4/S_5/S_8$	$D_2/D_3/D_5/D_8$	$D_2/D_3/D_5/D_8$
V	$S_2/S_3/S_5/S_8$	$S_2/S_3/S_5/S_8$	$D_2/D_3/S_6/S_7$
VI	$S_2/S_3/D_6/D_7$	$S_2/S_3/D_6/D_7$	$S_2/S_3/D_6/D_7$

characteristic impedance of resonant tank; $M=V'_2/V_1$ is the ratio between output voltage transferred to primary side and input voltage, which is called voltage conversion ratio for short.

The output active power is as follows:

$$P_o = \frac{4FMV_1^2}{\pi Z_r}\sec(\frac{\pi}{2F})\sin[\frac{(\pi-\delta)}{2F}]\sin(\frac{\delta}{2F}) \tag{3}$$

Equation (3) reveals that on the condition that F, M and Z_r have been determined, the required power is transmitted by changing the phase-shift angle δ. If $\delta > 0$, power transfers from the primary side to the secondary side and if $\delta < 0$, the direction of power flow is reversed.

B. Different Working Modes and Soft-Switching Discussion

It has been pointed out from the analyzing results of commutation in section A that the current i_p in phase-shift angle determines the soft-switching condition of the power switches in both primary and secondary sides. According to the polarity of $i_p(0)$ and $i_p(\delta)$, DBSRC can be divided into three working modes, whose waveforms are shown in Fig. 2, and the current paths are summarized in Table I. In spite of the different commutation of three working modes, they conform to the unified model mentioned above, because the second order differential equations are all the same within and outside the phase-shift angle δ. The status of $i_p(0)$ and $i_p(\delta)$ as well as the soft-switching condition are illustrated in Table II, where if the power switches can achieve Zero-Voltage-Switching, it will be denoted by "ZVS"; if not, it will be replaced by the current value when switching. The primary current of transformer at the beginning and end of phase-shift angle, i.e. $i_p(0)$ and $i_p(\delta)$ are exactly the current when power devices switch on or off, which is called switching current for short.

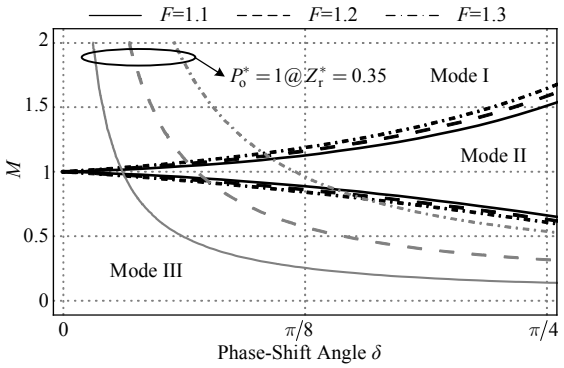

Fig. 3. The distribution of different working modes.

By solving the inequalities in Table II, the value of voltage conversion ratio M determines which mode DBSRC is working at. Specifically, boundary conditions are dependent on the ratio between switching and resonant frequency F and the phase-shift angle δ. The Distribution of different working modes is shown in Fig. 3, where the black lines represent the boundary lines of different working modes and gray lines are the conditions that output power reaches the rated power.

C. Different Load Discussion

When modeling DBSRC, output is regarded as a voltage source. Actually, the load can be voltage source load or resistive load. For voltage source load, such as an inverter, the output voltage is determined by external condition, and voltage conversion ratio M is unrestricted, and thus DBSRC is able to work at all three modes. For resistive load, M is dependent on the internal characteristic of DBSRC, which is essentially a LC series resonant DC/DC converter and its voltage conversion ratio satisfies following expression [10].

$$M = \frac{1}{\sqrt{1+Q^2\left(F-\frac{1}{F}\right)^2}} \tag{4}$$

where $Q = Z_r/R_{ac}$ is the quality factor; $R_{ac} = 8R'_L/\pi^2$ is the equivalent AC resistor of load. From (4), M is determined by Q and F, which is always less than 1. Therefore, DBSRC can only work at modes II and III on the resistive load. This paper

TABLE II. THE SOFT-SWITCHING CONDITION AT DIFFERENT WORKING MODES OF DBSRC.

Mode	Current	Boundary conditions	Switches in primary H-bridge		Switches in secondary H-bridge	
			Switch-on	Switch-off	Switch-on	Switch-off
I	$i_p(0)>0$, $i_p(\delta)>0$.	$M > \csc\left(\frac{\pi-2\delta}{2F}\right)\sin(\frac{\pi}{2F})$	$i_p(0)$	ZVS	ZVS	$i_p(\delta)$
II	$i_p(0)<0$, $i_p(\delta)>0$.	$M < \csc\left(\frac{\pi-2\delta}{2F}\right)\sin(\frac{\pi}{2F})$ and $M > \sin\left(\frac{\pi-2\delta}{2F}\right)\csc(\frac{\pi}{2F})$	ZVS	$i_p(0)$	ZVS	$i_p(\delta)$
III	$i_p(0)<0$, $i_p(\delta)<0$.	$M < \sin\left(\frac{\pi-2\delta}{2F}\right)\csc(\frac{\pi}{2F})$	ZVS	$i_p(0)$	$i_p(\delta)$	ZVS

analyzes the switching current under both two types of load.

III. Study on Reducing Switching Current

It is observed from Table II that ZVS-on and ZVS-off cannot be realized simultaneously for one power switch at any working mode with no extra snubber circuit connected. And the switching loss is either switch-on loss or switch-off loss, which is inevitable. Thus, the key to reduce switching loss of power switches in both primary and secondary H-bridge is to reduce the switching current $i_p(0)$ and $i_p(\delta)$ simultaneously as much as possible. For the convenience of analysis, all variables are normalized with the selection of output voltage V_2 and output active power P_o as base values of voltage (V_B) and power (P_B). So the base values of current and impedance are P_B/V_B and V^2_B/P_B, respectively. And the normalized variables are denoted by the superscript "*".

For voltage source load, the variations of $i_p^*(0)$ and $i_p^*(\delta)$ with respect to M on different F and Z_r^* at full load are plotted in Fig. 4 and Fig. 5, according to (1) and (2). Over the full voltage gain range, the variations of $i_p^*(0)$ and $i_p^*(\delta)$ are small when F and Z_r^* are relatively large. When DBSRC works at mode I or III, the absolute values of switching current are relatively small when choosing larger F and Z_r^*. However, when M is near 1,where DBSRC works at mode II, the absolute values $|i_p^*(0)|$ and $|i_p^*(\delta)|$ decrease obviously. And it is seen from Fig. 4(b) and Fig. 5(b) that smaller F and Z_r^* makes the switching current lower. Note that $i_p^*(0)$ is always negative and DBSRC cannot work at mode I when F and Z_r^* are too large, as shown in Fig. 4.

For resistive load, $M < 1$ and DBSRC is unable to work at mode I, and $|i_p^*(0)|$ and $|i_p^*(\delta)|$ reduce with the increase of M for all different F and Z_r^*, from Fig. 4 and Fig. 5. So the key to reduce switching current is to maintain M close to 1 and work at mode II. Similar to voltage source load, it is better to choose small F and Z_r^*. When load is heavy or switching frequency is high, M is significantly less than 1 and it is better to choose large F and Z_r^* at this time.

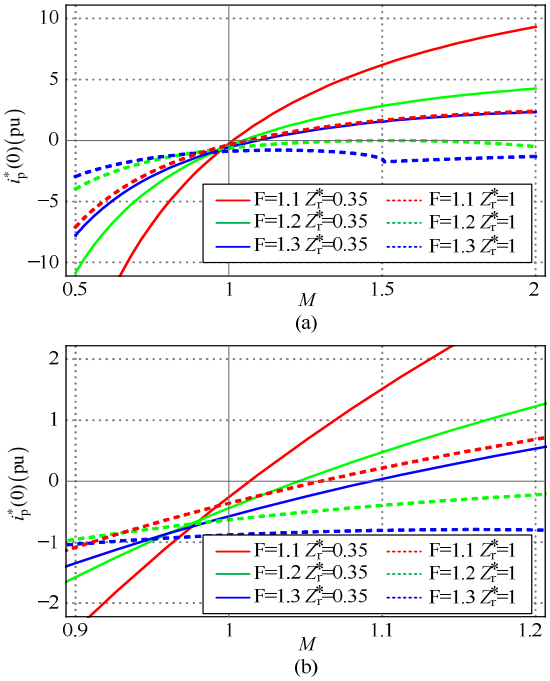

Fig. 4. The variation of $i_p^*(0)$ with respect to M on different F and Z_r^* at full load. (a) Global view; (b) Partial view.

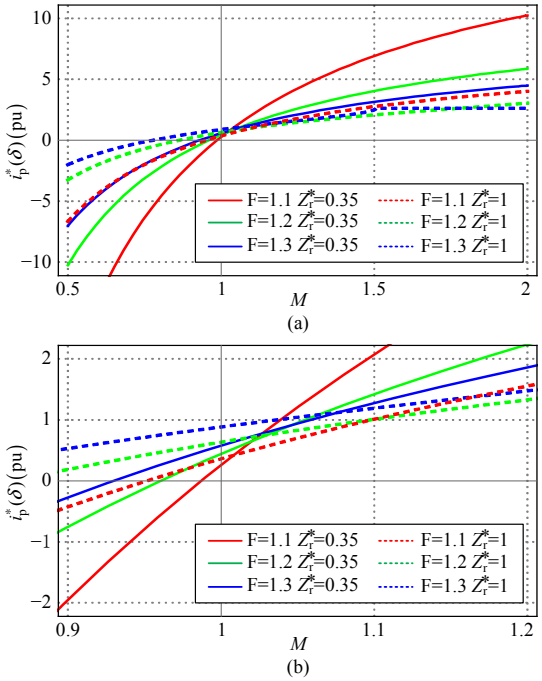

Fig. 5. The variation of $i_p^*(\delta)$ with respect to M on different F and Z_r^* at full load. (a) Global view; (b) Partial view.

IV. Simulation Verification

According to Fig. 1(a), a simulation model of DBSRC is built on PSIM. The turns ratio of transformer is 1:1. When setting different values of leakage inductance and resonant capacitance, the characteristic impedance Z_r is different, but the resonant frequency is assured to be fixed at 39 kHz, and the switching frequency is set as 43 kHz, 47 kHz and 50kHz, respectively, which is corresponding to F = 1.1, 1.2 and 1.3. The load is a voltage source, whose voltage is 500 V. And the rated output power is 23.5kW, which is consistent with the following experiment. The required phase-shift angle is obtained by solving (3).

The simulation waveforms of different M on Z_r = 3.7 Ω at full load are illustrated in Fig. 6, whose switching frequency f_s is 43 kHz. It is observed that the amplitude and phase of current differ a lot from each other due to different M. And DBSRC in Fig. 6 works at mode III, II and I, respectively. Under the same output power, the current of M = 1 at the beginning and end of phase-shift angle is obviously smaller than the condition that the input and output voltage are unequal. It proves that the switching current can be reduced when choosing to work at mode II on the voltage source load. By the way, the current stress and circulation power are also reduced at this working mode.

The simulation results of switching current on different switching frequency f_s and characteristic impedance Z_r at full

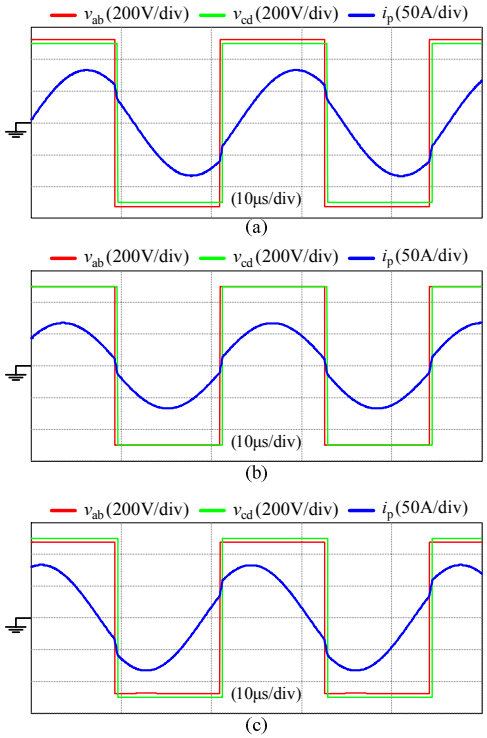

Fig. 6. The simulation waveforms on f_s = 43 kHz and Z_r = 3.7 Ω at full load. (a) M = 0.95; (b) M =1; (c) M = 1.05.

load are presented in Fig. 7. When M = 1, $|i_p(0)|$ and $|i_p(\delta)|$ reach a relatively small value at the same time, and the

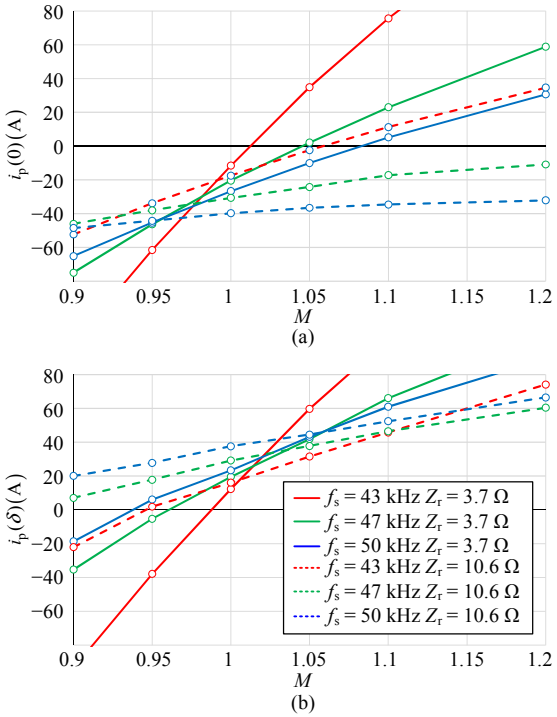

Fig. 7. The simulation results of switching current at full load. (a) $i_p(0)$; (b) $i_p(\delta)$.

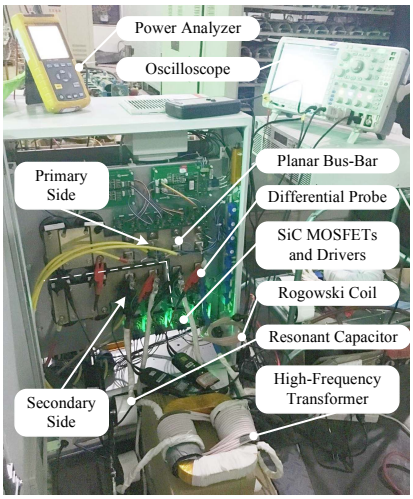

Fig. 8. A prototype of DBSRC.

selection of small f_s and Z_r makes switching currents smaller and reduces the switching loss of power switches in both H-bridges significantly. When M = 0.95 or 1.05, either $|i_p(0)|$ or $|i_p(\delta)|$ is larger than the condition that M = 1, and it is hard to say what parameters are more decent, because the variation of $i_p(0)$ or $i_p(\delta)$ is huge under different f_s and Z_r. When M = 0.9, 1.1 or 1.2, it is no doubt that the choose of larger f_s and Z_r makes switching currents smaller. Overall, the variations of $i_p(0)$ or $i_p(\delta)$ over the full M range are in good agreement with the theoretical analysis in section III, which implies the correctness of the DBSRC model and the effectiveness of method to reduce switching current.

V. Experiment Verification

A 23.5kW DBSRC prototype is set up, as shown in Fig. 8. 1200V, 300A SiC-MOSFET half-bridge modules from Cree Company are adopted as the power switches and there is no snubber capacitor connected in parallel. The turns ratio of high frequency nano-crystalline alloy transformer is 1:1, whose leakage inductance is 15 μH. The resonant capacitor is 1.1 μF, so the resonant frequency is 39 kHz and the characteristic impedance is 3.7 Ω. The switching frequency is set as 43 kHz, 47 kHz and 50 kHz, respectively. The load is a resistor, which is 10.6 Ω at rated power. The input DC voltage is generated from a three-phase rectifier, and the output voltage is regulated by a PI controller and fixed at 500 V under different load range.

The experiment waveforms on three different switching frequency f_s at full load are shown in Fig. 9, and DBSRC is all working at mode II under these three conditions. When f_s increases, the phase-shift angle increases gradually and it

TABLE III. The Switching Current of Different Switching Frequency at Various Load Levels

$i_p(0)$/ $i_p(\delta)$	f_s =43 kHz	f_s =47 kHz	f_s =50 kHz
Full Load	-19 A/11 A	-22 A/13 A	-45 A/10 A
75% Load	-13 A/ 8 A	-18 A/10 A	-25 A/10 A
50% Load	-8 A/ 5 A	-14 A/ 8 A	-17 A/ 9 A
25% Load	-4 A/ 3 A	-8 A/ 3 A	-10 A/ 4 A

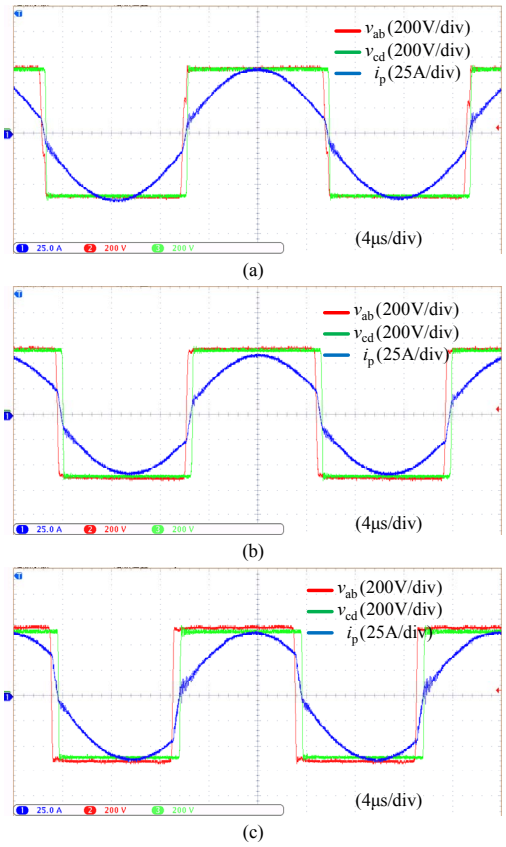

Fig. 9. The experiment waveforms on Z_r = 3.7 Ω at full load and different switching frequency. (a) 43 kHz; (b) 47 kHz; (c) 50 kHz.

makes the absolute value of $i_p(0)$ larger significantly with the amplitude of current not changing too much. This enlarges the switch-off loss of power switches in primary H-bridge. With the increase of f_s, the voltage conversion ratio M drops and is not equal to 1 strictly. Therefore, the absolute value of $i_p(0)$ and $i_p(\delta)$ are not identical and $i_p(\delta)$ is changeless. The experiment results of the switching current under various load levels are presented in Table III. Although the decline of $i_p(\delta)$ is not obvious with the decrease of f_s, the absolute value of $i_p(0)$ reduces significantly under various load levels. The above results imply that, under the condition that characteristic impedance Z_r is small relatively and M is close to 1, it is a better choice to select smaller f_s to reduce switching current. The system efficiency, illustrated in Fig. 10, is measured from the three-phase rectifier to the DC load resistor. The efficiency

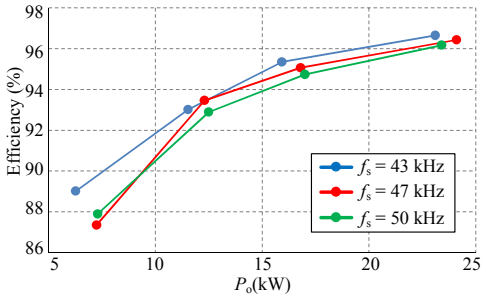

Fig. 10. The system efficiency under different switching frequency.

are all above 86% over the whole load range, and the peak value is 96.7% at f_s = 43 kHz and full load. And the efficiency when f_s = 43 kHz is substantially higher than the condition of 47kHz and 50 kHz over a wide load range, which verifies the correctness of the above conclusion.

VI. Conclusion

This paper analyzes the commutation of DBSRC and obtains its three working mode. Generated from the soft-switching condition, the transformer current at the beginning and end of phase-shift angle are the switching current, which causes switching loss. The relationship between switching current and hardware parameters under two types of load is summarized. To reduce the switching current, the following measures are expected to adopt.

1) For voltage source load: When the voltage conversion ratio M maintains near 1, DBSRC works at mode II and the switching current decreases obviously and it is better to choose small switching frequency f_s and characteristic impedance Z_r. If DBSRC works at mode I or III, select large f_s and Z_r.

2) For resistive load: Select small f_s and Z_r, to keep M close to 1 and reduce switching current.

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