Hybrid Space Vector Pulse Width Modulation Synthesis to Minimize the Common-mode Voltage

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***Abstract*—The conventional space vector pulse width modulation (SVPWM) techniques for inverters generate high-frequency common-mode voltage (CMV), which induces high frequency and amplitude shaft voltage. This can exceed the breakdown voltage of the lubricant in the bearings and result in a significant bearing current flowing through the path to the ground. The bearing current causes premature bearing failure and poses electromagnetic interference (EMI) issues, especially in high switching frequency drive systems. In this paper, a hybrid space vector pulse width modulation synthesis (HSVPWMS) is proposed to lower the frequency and amplitude of the CMV. The control algorithm divides each sector in the space vector hexagonal into three segments based on the modulation index and the angle of the reference voltage vector. In each segment, the space vectors that produce minimal CMV are selected to synthesize the reference voltage vector. Both simulation and experimental results have validated the effectiveness of the proposed approach.**

I. Introduction

Voltage source inverters (VSIs) are widely used in motor drive applications. The use of VSI ranges from high power (e.g., wind turbines) to medium power (e.g., electric and hybrid electric vehicles). Ever since the invention of the IGBT, increasing the switching frequency of the power converter has been a trend due to the reduction of the footprint and the increase of power density [1], [2]. Recent development of wide bandgap devices has equipped the power switches with even faster switching speed [3]. However, the increase in the switching frequency has generated several unwanted consequences, one of which is the high-frequency common-mode voltage (CMV) [4], [6]. The high-frequency CMV can cause electromagnetic interference (EMI) that adversely affects the other components of the system [7]. The induced over-voltage stresses the winding insulation of the drives and also can increase the shaft current [8]. In particular, the shaft current is the result of the fluctuation of the CMV, which is strictly related to the sequence of the inverter switching states [9]. Several studies presented in the literature discussed the reduction of CMV effects. They can be classified into hardware solutions and algorithmic solutions. Before using the additional passive components, it is essential to provide proper earthing paths to allow the stray current to return to the inverter frame other than through the machine bearings.

The hardware-based approaches fall into two categories: common-mode choke filters and common-mode active filters. The common-mode chokes are placed at the inverter output so that the inductance of the common-mode choke is very small for the differential mode. This occurs because the aggregate flux is zero for the three-phase diffrential currents while the inductance is significantly high for the common-mode current [11]. There is no straightforward process to obtain the optimal common-mode choke inductance. It is mostly an iterative process that requires measuring the CMV and the maximum common-mode current [12]. Most of the literature on common-mode chokes have focused on low-power applications where the current is only several amperes [13]. Besides the passive methods, active systems such as series active filters and auxiliary inverters are used to eliminate the CMV [14], [15]. The series active filter can be implemented using two complementary bipolar transistors directly triggered by the CMV without using a digital controller. Due to the limitations of the bipolar transistors, this solution is only suitable for low power applications. To overcome the aforementioned limitations, another topology is proposed uses an auxiliary inverter with lower power ratings [16]. However, full elimination of the CMV still impossible because it requires dead times, turn on/off times both inverters which is unfeasible when using switches of different ratings.

On the other hand, algorithmic approaches offer minimization of the CMV without any additional hardware circuitry. Several common-mode reduction PWM algorithms have been presented in the literature [17], [18]. The key approach is to eliminate the zero vectors that result in a CMV equal to half of the DC-link voltage $\pm V_{dc}$. The other concept of these approaches is to use only the active voltage vectors that have the same CMV (either odd or even voltage vectors). Utilizing only the odd or even active vectors has several drawbacks: decreasing the linear region with limited modulation index, degrading the inverter efficiency by increasing the switching losses, and increasing the total harmonic distortion.

In this paper, a hybrid approach for minimizing the amplitude and the frequency of the CMV is proposed. The control concept is based on dividing the space vector hexagon into various segments and synthesizing the reference voltage vector by using vectors that correspond to a minimal CMV. The proposed method features a minimum CMV amplitude and frequency throughout the entire linear region. This could be a great solution for very high switching frequency power converters.

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The rest of the paper is organized as follows. In Section II, the regular SVPWM is briefly revisited. The proposed control method is presented in Section III. Performance analysis for the CMV is presented in Section IV. The hardware results and the conclusion are presented in Section V and IV, respectively.

II. Conventional SVPWM

Consider the two-level, three-phase voltage source inverter shown in Fig. 1. The reference value of the inverter output voltage can be represented by the following space vector:

$$\mathbf{V}_{ref} = \frac{2}{3}(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}}) \tag{1}$$

where v_a, v_b, and v_c are the three phase voltages. Since the DC-link cannot be shorted, each phase voltage can only attain either V_{dc} or $-V_{dc}$. This also restricts the feasible switching state to only eight states. The eight converter states as well as the corresponding differential-mode voltage (DMV) and common-mode voltage are shown in Table I. The linear combination of the possible eight vectors span a hexagonal area as shown in Fig. 2.

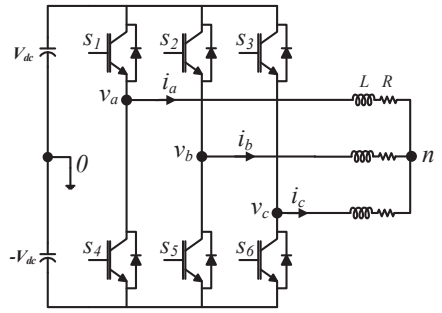

Fig. 1: Three-phase voltage source inverter.

The reference vector $\mathbf{V}_{ref}$ is synthesized at each sampling period T_s using the two adjacent active vectors and the zero vectors. This leads to six equal sectors. Because the circular trajectory of $\mathbf{V}_{ref}$ in the complex plane corresponds to a sinusoidal three-phase voltage, the maximum achievable sinusoidal output voltage amplitude is $\leq \frac{2}{\sqrt{3}}V_{dc}$. Therefore, we can define the modulation index MI as the per unit output voltage vector using V_{dc} as the base voltage $MI \in [0, \frac{2}{\sqrt{3}}]$.

TABLE I: The feasible voltage vectors and the corresponding DMV and CMV.

Voltage vector	v_a	v_b	v_c	$\mathbf{v}_{dm}$	v_{cm}
$\mathbf{V}_{(0,0,0)}$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$
$\mathbf{V}_{(1,0,0)}$	V_{dc}	$-V_{dc}$	$-V_{dc}$	$\frac{4}{3}V_{dc}$	$-\frac{V_{dc}}{3}$
$\mathbf{V}_{(1,1,0)}$	V_{dc}	V_{dc}	$-V_{dc}$	$(\frac{2}{3}+j\frac{2}{\sqrt{3}})V_{dc}$	$\frac{V_{dc}}{3}$
$\mathbf{V}_{(0,1,0)}$	$-V_{dc}$	V_{dc}	$-V_{dc}$	$(-\frac{2}{3}+j\frac{2}{\sqrt{3}})V_{dc}$	$-\frac{V_{dc}}{3}$
$\mathbf{V}_{(0,1,1)}$	$-V_{dc}$	V_{dc}	V_{dc}	$-\frac{4}{3}V_{dc}$	$\frac{V_{dc}}{3}$
$\mathbf{V}_{(0,0,1)}$	$-V_{dc}$	$-V_{dc}$	V_{dc}	$(-\frac{2}{3}-j\frac{2}{\sqrt{3}})V_{dc}$	$-\frac{V_{dc}}{3}$
$\mathbf{V}_{(1,0,1)}$	V_{dc}	$-V_{dc}$	V_{dc}	$(\frac{2}{3}-j\frac{2}{\sqrt{3}})V_{dc}$	$\frac{V_{dc}}{3}$
$\mathbf{V}_{(1,1,1)}$	V_{dc}	V_{dc}	V_{dc}	0	V_{dc}

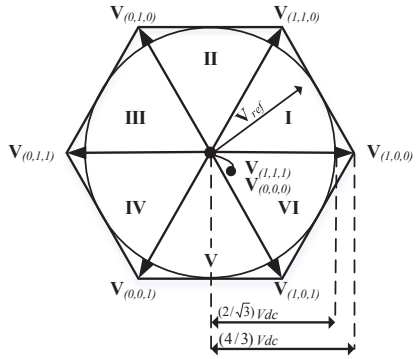

Fig. 2: Eight stationary vectors on the complex plane for a VSI.

For instance, when the trajectory of the reference voltage $\mathbf{V}_{ref}$ is passing though the first sector $\theta \in [0, \frac{\pi}{3}]$, the following volt-second equality holds:

$$T_s\mathbf{V}_{ref} = t_{v1}\mathbf{V}_{(1,0,0)} + t_{v2}\mathbf{V}_{(1,1,0)} + t_{v0}\mathbf{V}_{(0,0,0)} + t_{v7}\mathbf{V}_{(1,1,1)} \tag{2}$$

$$T_s = t_{v1} + t_{v2} + t_{v0} + t_{v7}. \tag{3}$$

By equating the real part and the imaginary part in (2), we can obtain the following dwell times:

$$t_{v1} = \frac{3}{4}T_s MI(\cos(\theta) - \sin(\theta)) \tag{4}$$

$$t_{v2} = \frac{\sqrt{3}}{2}T_s MI\sin(\theta) \tag{5}$$

$$t_{v0} = t_{v7} = Ts - t_{v1} - t_{v2}. \tag{6}$$

The same rules can be applied for calculating the dwell times of the vectors for sectors 2 through 6 if the following modified θ_k is used:

$$\theta_k = \theta - (k-1)\frac{\pi}{3} \tag{7}$$

where k is the number of the sector through which the $\mathbf{V}_{ref}$ is passing.

III. Hybrid Space Vector Pulse With Modulation Synthesis (HSVPWMS)

The HSVPWMS method further subdivides each sector into three segments. In each segment, a group of active voltage vectors is selected to match the output reference volt-seconds and achieve minimal CMV amplitude and frequency. The location of the reference voltage vector can be defined in correspondence to the modulation index MI and its angle θ.

The total eighteen segments of the space vector hexagon are divided based on their corresponding CMV, and they are of three types: i) six odd segments that result in CMV $-\frac{V_{dc}}{3}$, ii) six even segments that result in CMV $\frac{V_{dc}}{3}$, and iii) six odd-even segments that result in CMV $\pm\frac{V_{dc}}{3}$.

To understand the navigation of the reference voltage through those segments, the authors thoroughly explain the

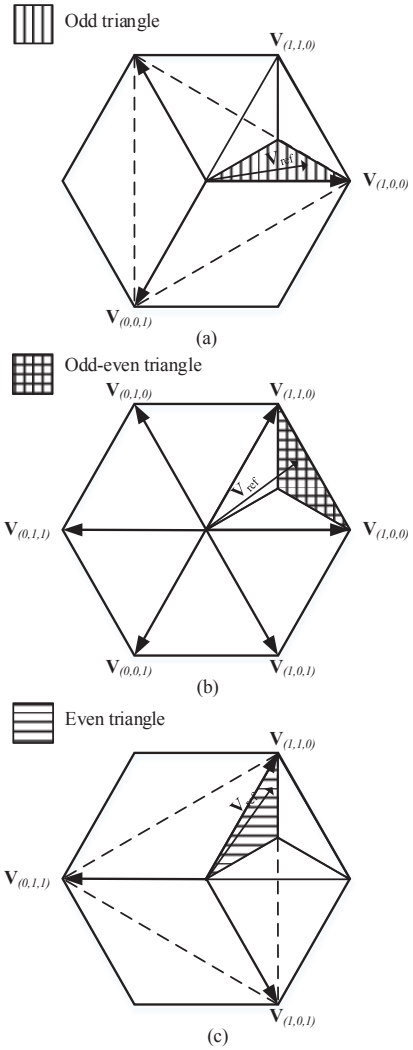

Fig. 3: Sector I is divided in to three segments: (a) odd triangle, (b) odd-even triangle, and (c) even triangle.

synthesis of the reference voltage vector though the first sector $\theta \in [0, \frac{\pi}{3})$ with reference to Fig. 3. The sector includes three segments (triangles). The reference vector in the bottom triangle (odd-triangle) can be synthesized using only the odd vectors $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$ as shown in Fig. 3 (a). The reference vector in the upper-right triangle (odd-even triangle) can be synthesized using the odd and even vectors $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, ..., \mathbf{V}_{(1,0,1)}\}$ as shown Fig. 3 (b). The reference vector in the upper-left triangle (even triangle) can be synthesized using only the even vectors $\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$ as shown Fig. 3 (c).

The synthesis of the reference voltage vector in the odd triangle and even triangle are unique, whereas the synthesis for the reference voltage vector in the odd-even triangle can be realized using different groups of vectors. The groups are classified into four groups, each group producing similar harmonic content and switching losses. The four groups are delineated in the following subsections.

A. HSVPWMS I

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and the two voltage vectors of the neighboring states to match the output and reference volt-seconds as shown in Fig. 4 (b).

For the odd triangle shown in Fig. 4 (a), the time intervals in which the inverter states $\{(\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$ are applied can be calculated by solving the following algebraic equations:

$$\mathbf{V}_{ref}T_s = \mathbf{V}_{(1,0,0)}t_{v1} + \mathbf{V}_{(0,1,0)}t_{v3} + \mathbf{V}_{(0,0,1)}t_{v5} \quad (8)$$

$$T_s = t_{v1} + t_{v3} + t_{v5}. \quad (9)$$

This leads to the following dwell times:

$$t_{v1} = \frac{T_s}{3} + \frac{T_s MI\cos(\theta)}{2} \quad (10)$$

$$t_{v3} = \frac{T_s}{3} - \frac{T_s MI\cos(\theta)}{4} + \frac{\sqrt{3}T_s MI\sin(\theta)}{4} \quad (11)$$

$$t_{v5} = \frac{T_s}{3} - \frac{T_s MI\cos(\theta)}{4} - \frac{\sqrt{3}T_s MI\sin(\theta)}{4}. \quad (12)$$

For the odd-even triangle shown in Fig. 4 (b), the time intervals in which the inverter states $\{(\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}\}$ are applied can be calculated by solving the following algebraic equations:

$$\mathbf{V}_{ref}T_s = \mathbf{V}_{(1,0,1)}t_{v6} + \mathbf{V}_{(1,0,0)}t_{v1} + \mathbf{V}_{(1,1,0)}t_{v2} + \mathbf{V}_{(0,1,0)}t_{v3} \quad (13)$$

$$T_s = t_{v6} + t_{v1} + t_{v2} + t_{v3}. \quad (14)$$

To solve the algebraic equations, we assume t_{v6} is equal to t_{v3}. This leads to the following dwell times:

$$t_{v1} = \frac{3T_s MI\cos(\theta)}{4} - \frac{\sqrt{3}T_s MI\sin(\theta)}{4} \quad (15)$$

$$t_{v2} = \frac{\sqrt{3}T_s MI\sin(\theta)}{2} \quad (16)$$

$$t_{v6} = t_{v_3} = \frac{T_s}{2} - \frac{3T_s MI\cos(\theta)}{8} - \frac{\sqrt{3}T_s MI\sin(\theta)}{8}. \quad (17)$$

For the even triangle shown in Fig. 4 (c), the time intervals in which the inverter states $\{(\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$ are applied can be calculated by solving the following algebraic equations:

$$\mathbf{V}_{ref}T_s = \mathbf{V}_{(1,1,0)}t_{v2} + \mathbf{V}_{(0,1,1)}t_{v4} + \mathbf{V}_{(1,0,1)}t_{v6} \quad (18)$$

$$T_s = t_{v2} + t_{v4} + t_{v6}. \quad (19)$$

This leads to the following dwell times:

$$t_{v2} = \frac{T_s}{3} + \frac{T_s MI\cos(\theta)}{4} + \frac{\sqrt{3}T_s MI\sin(\theta)}{4} \quad (20)$$

$$t_{v4} = \frac{T_s}{3} - \frac{T_s MI\cos(\theta)}{2} \quad (21)$$

$$t_{v6} = \frac{T_s}{3} + \frac{T_s MI\cos(\theta)}{4} - \frac{\sqrt{3}T_s MI\sin(\theta)}{4}. \quad (22)$$

The similar calculation can be conducted for the other five sectors by employing the appropriate vectors as listed in Table II.

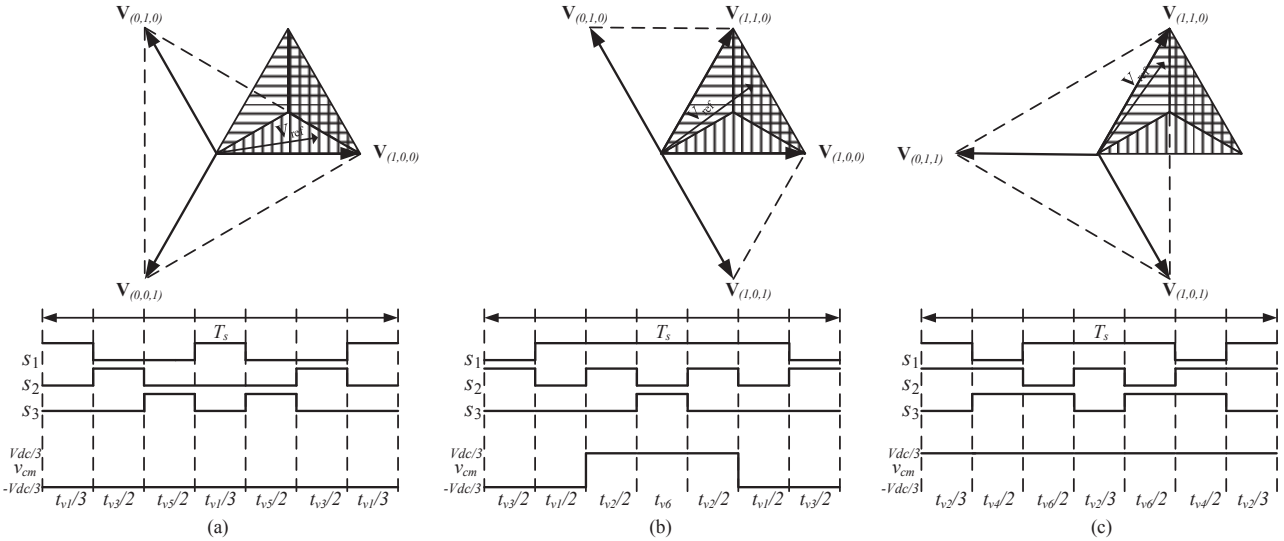

Fig. 4: Vector synthesis for HSVPWM I of (a) odd triangle, (b) odd-even triangle, and (c) even triangle.

TABLE II: The vector combinations used in the three segments of each sector using HSVPWMS I.

Sector	Odd triangle	Odd-even triangle	Even triangle
I	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
II	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
III	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
IV	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
V	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
VI	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$

B. HSVPWMS II

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and one voltage vector of either neighboring state to match the output and reference volt-seconds as shown in Fig. 5 (a). Table III shows the vector combinations used in the three segments of each sector for HSVPWMS II.

TABLE III: The vector combinations used in the three segments of each sector using HSVPWMS II.

Sector	Odd-even triangle
I	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, (\mathbf{V}_{(0,1,0)} \vee \mathbf{V}_{(1,0,1)})\}$
II	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, (\mathbf{V}_{(0,1,1)} \vee \mathbf{V}_{(1,0,0)})\}$
III	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, (\mathbf{V}_{(0,0,1)} \vee \mathbf{V}_{(1,1,0)})\}$
IV	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, (\mathbf{V}_{(1,0,1)} \vee \mathbf{V}_{(0,1,0)})\}$
V	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, (\mathbf{V}_{(1,0,0)} \vee \mathbf{V}_{(0,1,1)})\}$
VI	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, (\mathbf{V}_{(1,1,0)} \vee \mathbf{V}_{(0,0,1)})\}$

C. HSVPWMS III

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and the two voltage vectors of the far states to match the output and reference volt-seconds as shown in Fig. 5 (b). Table IV shows the vector combinations used in the three segments of each sector for HSVPWMS III.

TABLE IV: The vector combinations used in the three segments of each sector using HSVPWMS III.

Sector	Odd-even triangle
I	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}\}$
II	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$
III	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
IV	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,0)}\}$
V	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,1,0)}\}$
VI	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}\}$

D. HSVPWMS IV

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and one voltage vectors of either far state to match the output and reference volt-seconds as shown in Fig. 5 (c). Table V shows the vector combinations used in the three segments of each sector for HSVPWMS IV.

TABLE V: The vector combinations used in the three segments of each sector using HSVPWMS IV.

Sector	Odd-even triangle
I	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, (\mathbf{V}_{(0,1,1)} \vee \mathbf{V}_{(0,0,1)})\}$
II	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, (\mathbf{V}_{(0,0,1)} \vee \mathbf{V}_{(1,0,1)})\}$
III	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, (\mathbf{V}_{(1,0,1)} \vee \mathbf{V}_{(1,0,0)})\}$
IV	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, (\mathbf{V}_{(1,0,0)} \vee \mathbf{V}_{(1,1,0)})\}$
V	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, (\mathbf{V}_{(1,1,0)} \vee \mathbf{V}_{(0,1,0)})\}$
VI	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, (\mathbf{V}_{(0,1,0)} \vee \mathbf{V}_{(0,1,1)})\}$

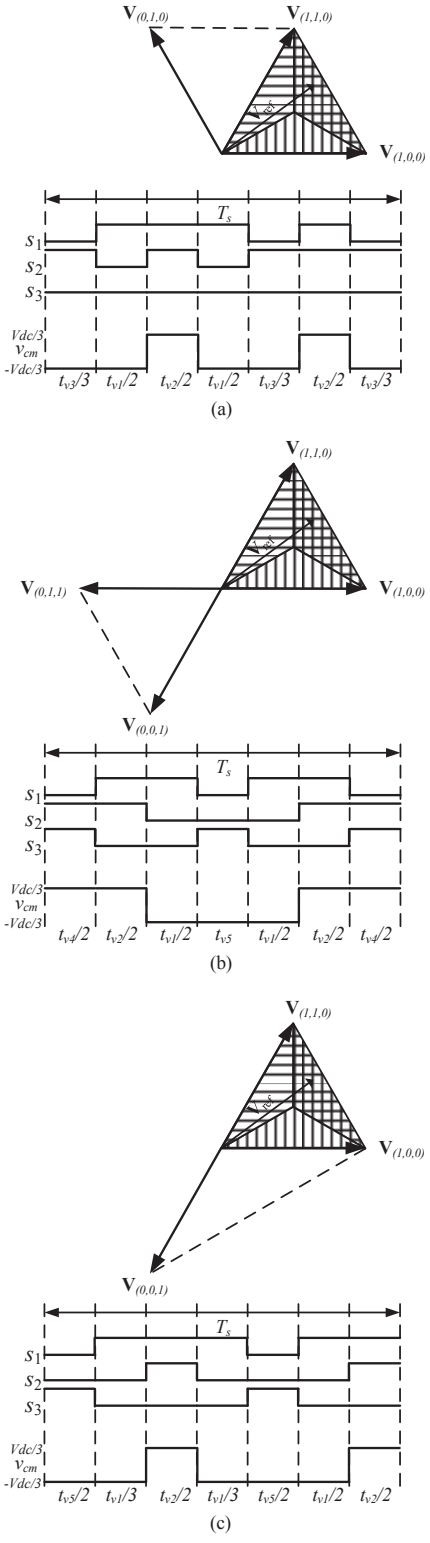

Fig. 5: Vector synthesis of odd-even triangle for (a) HSVPWMS II, (b) , HSVPWMS III (c) HSVPWMS IV. Note that the switching sequence is selected to minimize CMV and not to minimize THD or switching losses.

IV. Common-mode voltage Performance Analysis

HSVPWMS methods utilize different voltage vectors with different possible sequences. Each synthesis and combination corresponds to a different number of commutations and CMV characteristics.

Common-mode behavior for induction machines is mostly capacitive [25]. A machine model for high frequencies is develeoped in [22] and shows that the CM current is directly proportional to the frequency of the CMV.

Fig. 6 shows the frequency spectrum of the the CMV for the conventional SVPWM. The amplitude of the CMV is V_{dc} and is high due to the use of zero vectors.

All of the other HSVPWMS methods have similar CMV waveforms for $MI \leq \frac{4}{3\sqrt{3}}$ with the frequency of the main components being $3f_1$ and $6f_1$. These two frequency components result in a very small common-mode current because the impedance is very high prior to the resonance region [25]. HSVPWMS I and HSVPWMS III have harmonic components located around the carrier frequency f_c with an amplitude lower than that of the conventional SVPWM method. The f_c component increases as the MI increases as shown in Fig. 7 and Fig. 9. HSVPWMS II and HSVPWMS IV have high-frequency CMV components around $2f_c$ that increase as the MI increases. Most of the CMV harmonic components are concentrated in the fundamental component $3f_1$ Hz and base band harmonic $6f_1$ Hz as shown in Fig. 8 and Fig. 10. Generally, HSVPWMS methods have a maximum CMV amplitude equal to $\frac{V_{dc}}{3}$, which is three times less than the regular SVPWM. More importantly, the amplitudes of CMV at high frequencies are reduced tremendously, especially at $MI \leq MI_{max}$. Therefore, the resultant CM current in the HSVPWMS method can be significantly reduced.

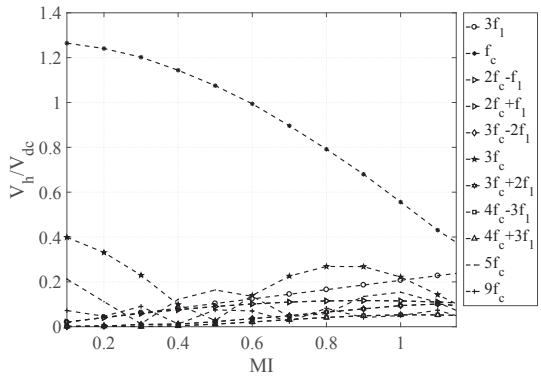

Fig. 6: Harmonic component amplitudes along a MI range for the regular SVPWM.

V. Experimental results

The experimental work has been carried out using the following parameters and operating conditions: carrier frequency $f_c = 5$ kHz to exaggerate the harmonic performance and an RL load with 2 Ω and 1 mH. The system consists of three inverter legs with each leg being realized by the IGBT module

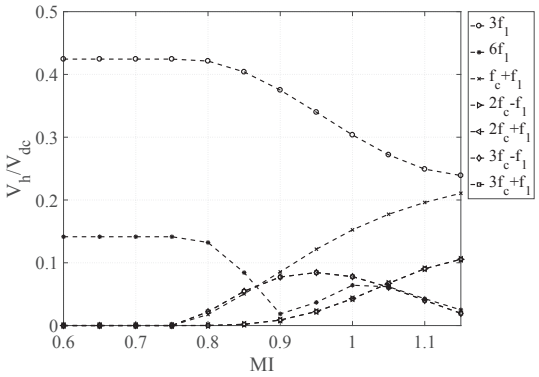

Fig. 7: Harmonic component amplitudes along a MI range for HSVPWMS I.

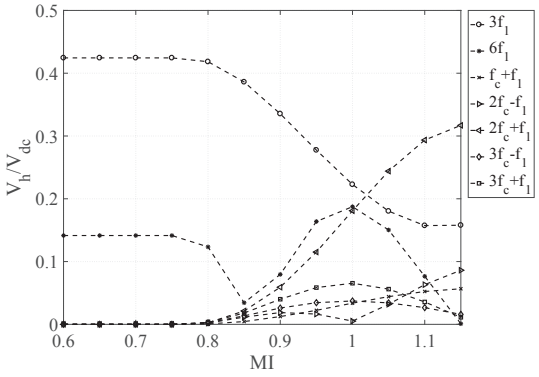

Fig. 8: Harmonic component amplitudes along a MI range for HSVPWMS II.

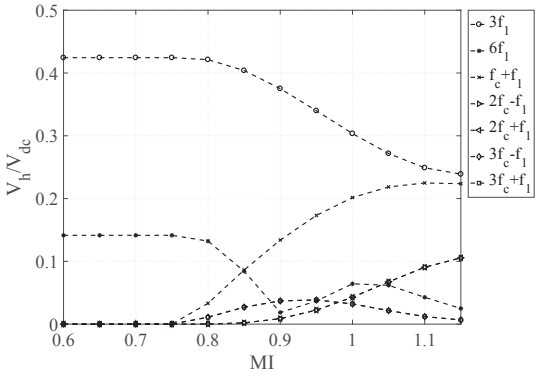

Fig. 9: Harmonic component amplitudes along a MI range for HSVPWMS III.

CM100DY-24A. The control algorithm is implemented using DSpace CP1103.

Fig. 11 shows experimental results for the current i_a, the phase voltage v_a and the CMV v_{cm} with its frequency spectrum for the conventional SVPWM method. The amplitude of the CMV is V_{dc} and harmonic components starting from maximum at 5 kHz to 54 kHz which is a multiple number of the fundamental system frequency and the carrier frequency.

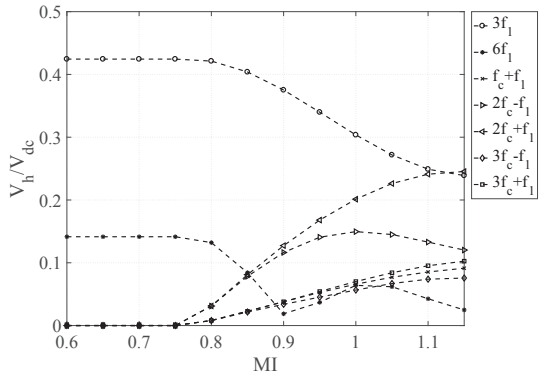

Fig. 10: Harmonic component amplitudes along a MI range for HSVPWMS IV.

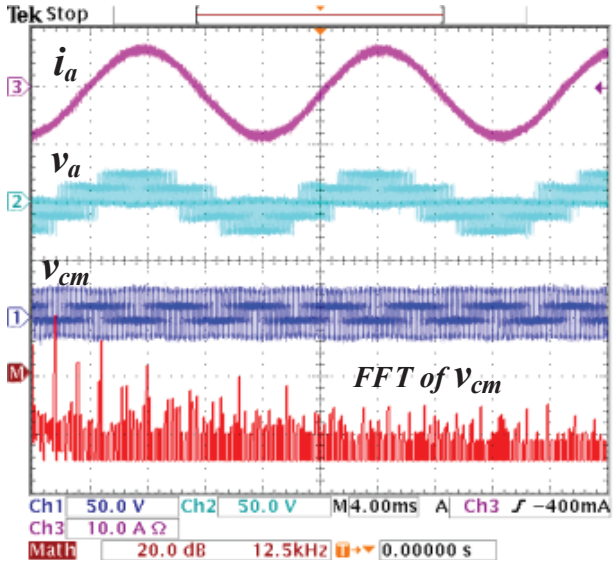

Fig. 11: Regular SVPWM experimental results of the load current i_a, phase voltage v_a, and CMV v_{cm}; $MI = 0.866$.

All of the HSVPWMS methods shows similar performance for $MI \leq \frac{4}{3\sqrt{3}}$. The CMV amplitude of the HSVPWMS methods is limited to $\frac{V_{dc}}{3}$. The frequency of the common mode voltage increases as the MI increased beyond $\frac{4}{3\sqrt{3}}$. However, the amplitudes of those high frequency components are much smaller than than that from the regular SVPWM.

Fig. 12 shows the experimental results for the current i_a, the phase voltage v_a and the CMV v_{cm} with its frequency spectrum for HSVPWMS I. Fig. 13 shows the experimental results for the current i_a, the phase voltage v_a and the CMV v_{cm} with its frequency spectrum for HSVPWMS II. Fig. 14 shows the experimental results for the current i_a, the phase voltage v_a and the CMV v_{cm} with its frequency spectrum for HSVPWMs III. Fig. 15 shows the experimental results for the results current i_a, the phase voltage v_a and the CMV v_{cm} with its frequency spectrum for HSVPWMS IV.

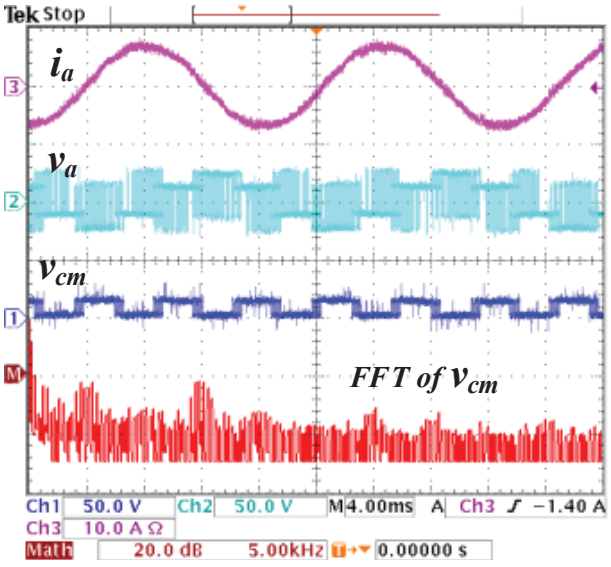

Fig. 12: HSVPWMS I experimental results of the load current i_a, phase voltage v_a, and CMV v_{cm}; $MI = 0.866$.

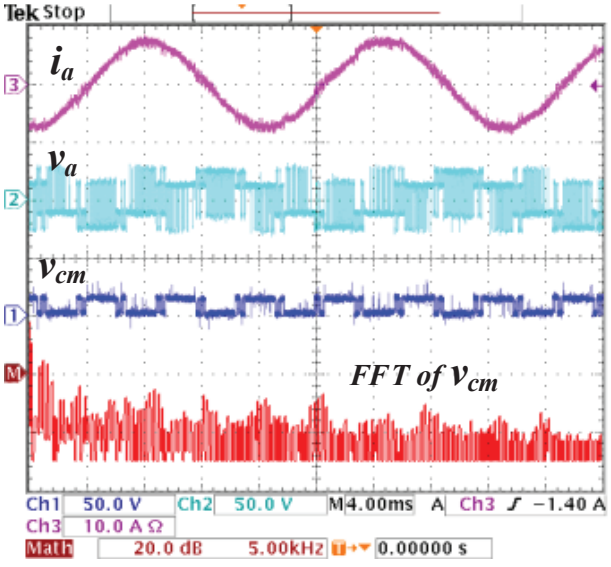

Fig. 13: HSVPWMS II experimental results of the load current i_a, phase voltage v_a, and CMV v_{cm}; $MI = 0.866$.

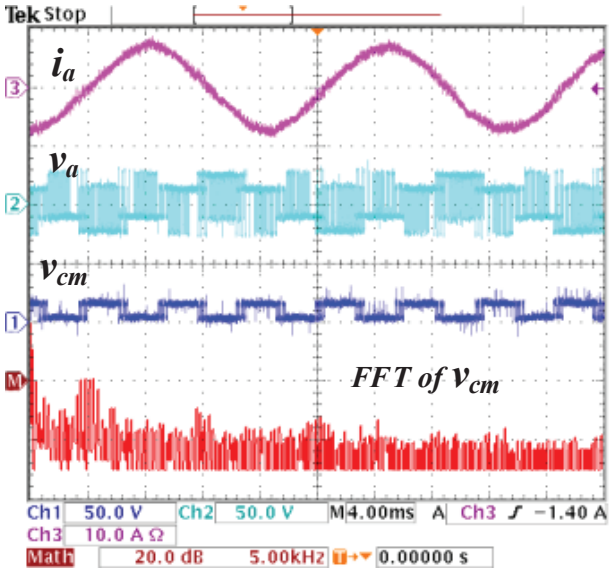

Fig. 14: HSVPWMS III experimental results of the load current i_a, phase voltage v_a, and CMV v_{cm}; $MI = 0.866$.

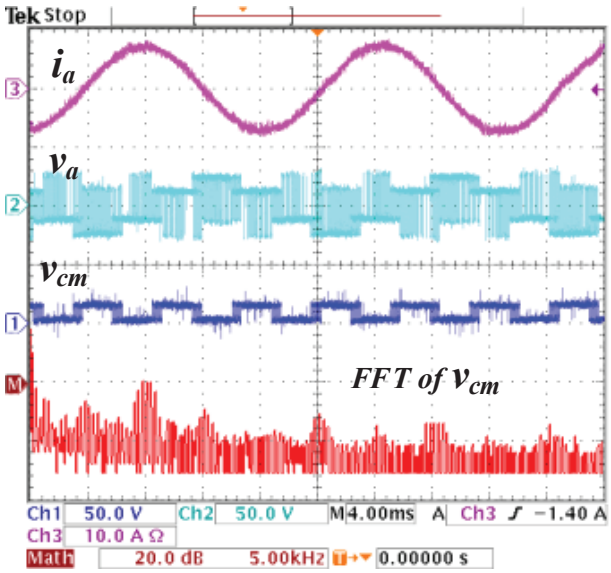

Fig. 15: HSVPWMS IV experimental results of the load current i_a, phase voltage v_a, and CMV v_{cm}; $MI = 0.866$.

VI. Conclusion

In this paper, a set of new hybrid space vector pulse width modulation syntheses (HSVPWMS) control methods are proposed to minimize amplitude and the frequency of the CMV. A frequency analysis of the CMV waveforms shows the performance of the HSVPWMS methods in terms of CMV harmonic components amplitudes and frequencies as compared to the conventional SVPWM method. The conventional SVPWM have a CMV harmonic component with high frequency equal to the carrier frequency f_c and an amplitude up to $1.2V_{dc}$. Whereas the new HSVPWMS methods proposed in the paper limit the CMV amplitude to $\frac{V_{dc}}{3}$ and concentrate the CMV harmonics to a low frequency equal to three times the system frequency $3f_1$ and with an amplitude no more than $0.4V_{dc}$. The performance of the proposed HSVPWMS algorithms has been verified via simulations and and validated by laboratory experiments. The new HSVPWMS methods can potentially enable converters to operate at a very high switching frequency using the newly emerging wide band gap devices while effectively mitigating the adverse CMV effects associated with conventional high-frequency SVPWM schemes.

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