

Opportunities and Design Considerations of GaN HEMTs in ZVS Applications

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Abstract—Gallium Nitride enhancement-mode high electron mobility transistors (GaN E-HEMTs) exhibit superior performance versus Si devices in both hard-switching and soft-switching converters. Due to the relatively higher switching-on loss compared with switching-off loss, zero voltage switching (ZVS) turn-on is still preferred to the application scope which efficiency is the primary design target. In this paper, the characteristics of GaN HEMTs under ZVS conditions is modeled. The packaging considerations on circuit parasitics and thermal management for soft switching applications is also discussed. An insulated metal substrate (IMS) based half-bridge power module consisting of two high-side and two low-side 650 V/60 A GaN HEMTs in parallel is designed and experimentally evaluated. A strong correlation is shown between simulations and experiments, verifying the power module design and GaN HEMTs' loss model.

Keywords—GaN HEMT; power module; soft switching; parasitics analysis; thermal management; loss analysis.

I. INTRODUCTION

In past several years, Gallium Nitride High Electron Mobility Transistor (HEMT) has been a focus in both academia and industry, due to the ultra-fast switching transitions and extremely low figure of merits merit ($R_{DS(on)} \times Q_G$), compared with conventional Silicon counterparts.

As the volume of production increases and the cost drops with the maturity of GaN E-mode HEMTs technology, industry is applying such devices into many power electronics systems, including wireless chargers, travel adapters, smart home appliances, high efficiency AC-DC datacenter power supplies, industrial motor drives, distributed energy generation and storage systems, aerospace, automotive traction inverters, on-board EV battery chargers, etc [1]-[9].

Although GaN HEMTs exhibit superior performance versus Si devices on both hard-switching and soft-switching converters, zero voltage switching (ZVS) turn-on is still preferred to the application scope which efficiency is the primary design target, due to the relatively higher switching-on loss compared with switching-off loss. For instance, the measured switching energy of GS66516T is shown in Fig.1. The switching-on energy is much higher than the switching-off energy in the whole device operating range.

So far, the most popular high power ZVS topologies include dual active bridge (DAB), critical conduction mode (CrM) totem-pole PFC, LLC resonant converter, phase-shift full bridge and so on. In terms of the switching loss, the power switches in

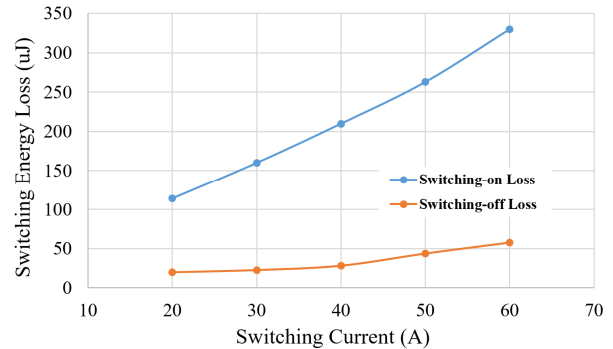


Fig. 1. Switching energy of GS66516T Vs. Switching Current at $V_{BUS}=400$ V.

these topologies only suffer from the hard switching-off loss. By waiving the hard switching-on energy loss, it is possible to further increase the switching frequencies and therefore reduce the size of passive components and increase the system power density.

Because of the characteristics and heterojunction structure of GaN, the behavior of GaN HEMTs is quite different from Si MOSFETs. The ultra-small parasitic capacitance makes it possible to deplete the two-dimensional electron gas (2DEG) even before the dv/dt period of the switching-off transition, which results in an extremely low switching-off loss [10]. Also, during the reverse conduction mode, GaN HEMTs don't demonstrate a body diode effect. Instead, the negative V_{DS} will turn on the device with the drain behaving as a source and the source as a drain. In this paper, the total energy loss dissipated on GaN HEMTs during the ZVS transition is modeled.

Furthermore, package considerations on thermal management and circuit parasitics are also discussed under ZVS conditions. As an example, an insulated metal substrate (IMS)-based 120A/650V GaN half-bridge power module is designed and experimentally evaluated to verify the GaN HEMT loss model in this paper. A test platform based on energy recirculation and storage circuit, combining frequency varying and phase-shift control is employed to evaluate the loss of GaN switches under soft switching conditions. Comparison between simulations and experiments are made to verify the power module design and GaN loss model.

The rest of the paper is organized as follows: section II presents the loss model of GaN HEMTs under ZVS conditions. The package design considerations of GaN HEMTs are discussed in section III. The experimental results are given in section IV. At last, conclusions and future work are given in the section V.

II. LOSS MODEL OF GAN HEMTs IN ZVS APPLICATIONS

The ZVS transition of a power switch can be mainly divided into four intervals. Fig. 2 shows a typical ZVS transition of S_1 in a half bridge configuration.

A. Initial state: S_2 conduction

During the state (a) of Fig. 2, the load current I_{load} is flowing through the 2DEG of S_2 as an initial condition, while the v_{GS} of S_2 is higher than $(V_{th} + \frac{I_{load}}{g})$, where V_{th} and g is the threshold voltage and transconductance.

B. S_2 switching-off transition

During the state (b), the dv/dt transition begins. S_2 will suffer from switching-off loss. Similar to Si MOSFET, Miller plateau V_{GS_miller} can also be observed during this period. The circuit equations are expressed as (1-3),

$$v_{GS_miller} = \frac{1}{R_1} (V_{DRoff} + R_G \cdot C_{GD} \cdot \frac{dv_{DS(t)}}{dt} + M \cdot C_{GD} \cdot \frac{d^2 v_{DS(t)}}{dt^2} + L_G \cdot C_{GD} \cdot \frac{d^2 v_{DS(t)}}{dt^2}) \quad (1)$$

$$R_{2DEG} = \frac{v_{DS(t)}}{g \cdot (v_{GS_miller} - V_{th})} \quad (2)$$

$$v_{DS(t)} = V_{BUS} \cdot (1 - e^{\frac{-t}{R_{2DEG} \cdot C_1 / C_2}}) \quad (3)$$

where M is the mutual inductance between the power and the gate driver loops, L_G/R_G is gate loop inductance/resistance, and C_{GD} is Miller capacitance.

R_G and V_{DRoff} determine V_{GS_miller} , then further affect the slew rate of $v_{DS(t)}$. The extremely low C_{GD} of GaN HEMT, makes it possible to pull V_{GS_miller} lower than V_{th} . In this case, the 2DEG is pinched off during the whole dv/dt period, and the switching loss of GaN is ignorable.

Adding a negative gate-source driving voltage (e.g. -3V) can expedite such switching-off transition and ensure the 2DEG is depleted during dv/dt transition, even with high switching off current. Fig. 3 shows the switching-off loss of GS66516B with different V_{DRoff} measured by double pulse test platform. With $V_{DRoff} = -5$ V, the switching off energy is ignorable even under 60A switching off current.

C. S_2 reverse conduction

During the state (c) of Fig.2, the load current is reversely flowing through S_1 , after the dv/dt transition is finished. Different from Si MOSFET, GaN HEMT does not exhibit a body diode effect. In the reverse conduction mode, the drain of GaN HEMT will behave as the source and the source will act as the drain. When V_{GD} is higher than V_{thGD} , the switch turns on. The reverse conduction characteristics of GS66516B are

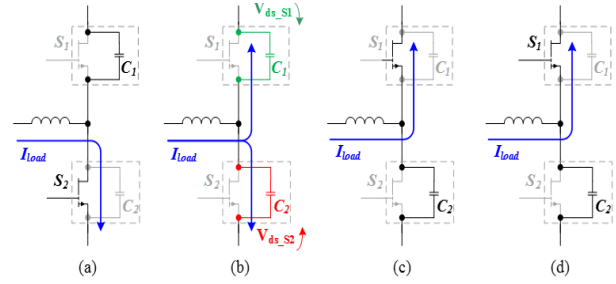


Fig. 2. ZVS transition of a half bridge power stage, (a) S_2 conduction, (b) S_2 switching-off, (c) S_1 reverse conduction, (d) S_1 conduction.

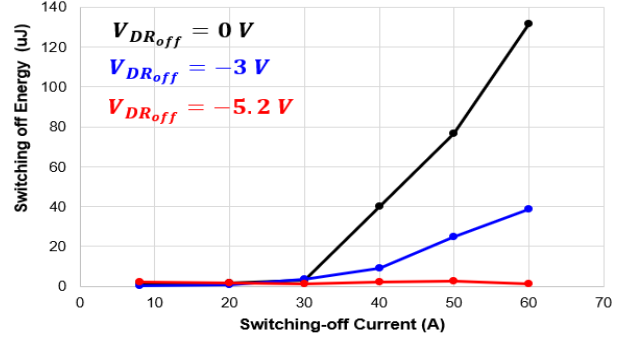


Fig. 3. Switching-off loss vs. current at $V_{BUS}=400$ V.

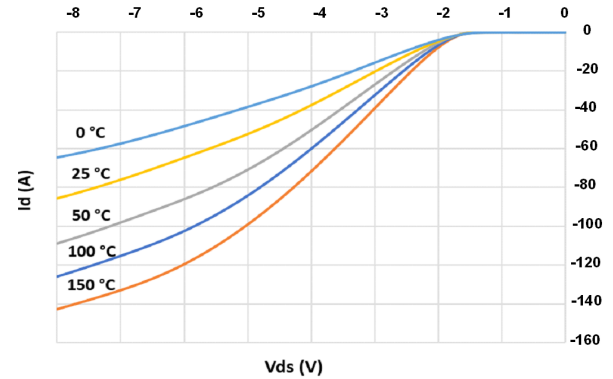


Fig. 4. Temperature-dependent third quadrant IV curves of GS66516B at $V_{DRoff}=0$ V.

measured under different temperature with $V_{DRoff}=0$ V shown in Fig.4.

The voltage drop equation of GaN HEMTs during reverse conduction mode could be expressed as,

$$v_{SD} = V_{thGD} - V_{DRoff} + I_D \cdot R_{Dson}(V_{GD}) \quad (4)$$

where $R_{dson}(V_{GD})$ is the R_{dson} in the third quadrant. Please note that the R_{dson} in the third quadrant is also temperature-dependent, and a negative V_{DRoff} will increase the reverse voltage drop across GaN HEMTs.

Dead time needs to be long enough for parasitic capacitance to be fully charged and discharged as derived in (5), where C_{eq} is energy equivalent capacitances of half-bridge.

Otherwise, the rest energy stored in the C_{eq} will be dissipated in the 2DEG of S_1 during switching-on.

$$t_d > \frac{C_{eq} \cdot V_{bus}}{i_{switching}} \quad (5)$$

In order to reduce the deadtime loss especially when a negative V_{DRoff} is applied, a short deadtime period is preferred for GaN HEMT. When deadtime is too long, the reverse conduction loss of S_1 will increase. By applying GS66516B as an example, the relation between the total loss during ZVS transition and the deadtime length is plotted as shown in Fig. 5. It is clearly that from Fig. 5, an optimum deadtime can be obtained to achieve a minimum loss. It can lead to a minimum deadtime loss and in the meanwhile, realize ZVS on the freewheeling switch.

The optimum deadtime under different operating voltage V_{Bus} and switching current is shown in Fig.6. However, in practical, it is relatively difficult to maintain the optimum deadtime across the full load range.

In order to reduce the overall loss of the whole ZVS transition process, actually, during the state (b) and the state (c), a trade-off analysis for the negative V_{DRoff} is required. A higher negative V_{DRoff} could reduce switching-off loss on S_2 , and increase system robustness. However, it will also increase the deadtime loss. Fig. 7 shows the overall loss of GS66516B-based half-bridge under different V_{DRoff} and t_D . In high power applications, the negative V_{DRoff} could significantly reduce the total loss of ZVS transition. In this paper, experimental results with $V_{DRoff} = -3V$ are presented for 120 A / 650 V IMS-based GaN power module.

D. S_1 switching-on transition

In the state (d) of Fig. 2, the freewheeling switch, S_1 is turned on after dead time. To realize ZVS on S_1 , the reactive energy stored in the inductor should be able to fully charge and discharge the energy stored in the parasitic capacitance of the power switches and PCB and to offer the dead time loss. Therefore, the condition to realize ZVS is depicted by (6). And the required minimum switching-off current i_{Smin} is derived as (7).

$$0.5 \cdot L \cdot i_{Smin}^2 > i_{Smin} \cdot V_{SD} \cdot \left(t_d - \frac{C_{eq} \cdot V_{DC}}{i_{Smin}} \right) + 0.5 \cdot C_{eq} \cdot V_{DC}^2 \quad (6)$$

$$i_{Smin} > \frac{t_d \cdot V_{SD} + \sqrt{t_d^2 \cdot V_{SD}^2 - 2 \cdot L \cdot C_{eq} \cdot V_{DC} \cdot V_{SD} + L \cdot C_{eq} \cdot V_{DC}^2}}{L} \quad (7)$$

On the contrary, introducing too much reactive power will also hurt the system efficiency as additional conduction loss are generated from semiconductors and magnetics components.

As a summary, it is important to define an accurate ZVS boundary considering both the inductive and capacitive energy. A trade-off analysis is also needed for the deadtime length and negative gate voltage to fully utilize the ultra performance of high efficiency and power density GaN-based systems.

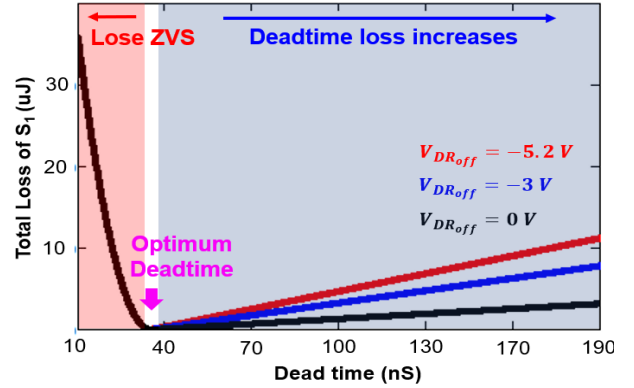


Fig. 5. Relation between total loss and deadtime of GS66516B at $I_d=10A, 25 \square$.

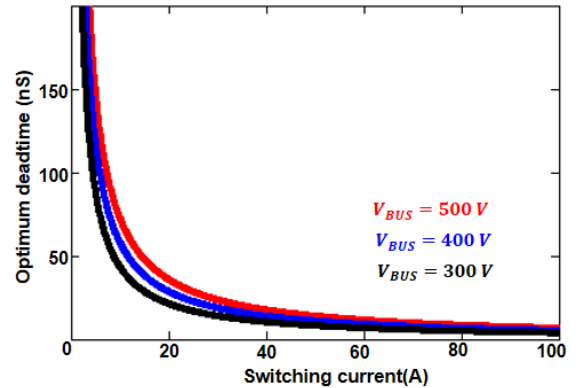


Fig. 6. Optimum deadtime Vs. switching off current at $V_{BUS}=400V$.

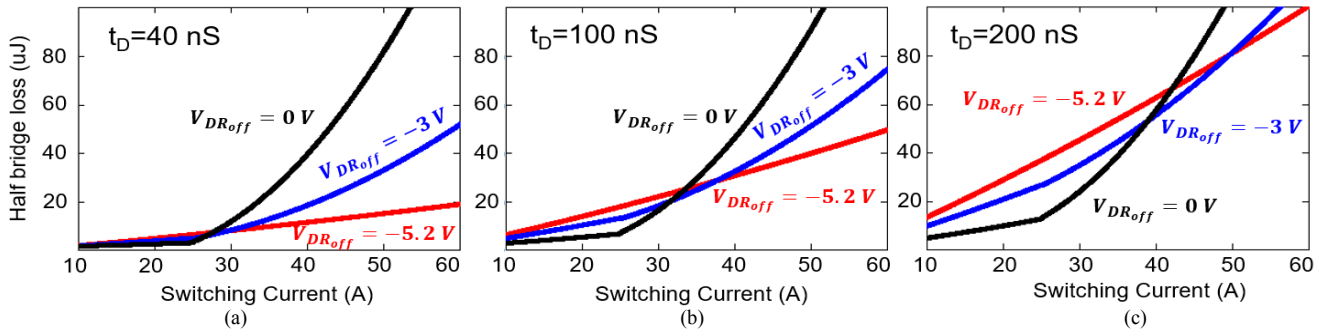


Fig. 7. Half-bridge overall loss vs. switching current under different negative turn-off gate voltage V_{DRoff} (a) with deadtime $t_D=40$ ns, (b) with deadtime $t_D=100$ ns, (c) with deadtime $t_D=200$ ns.

III. PACKAGE CONSIDERATION OF GAN HEMTs IN ZVS APPLICATIONS

A. Circuitry parasitic parameters

It is worth mentioning that, the gate loop and power commutation loop design for ZVS application is less challenging compared with hard switching applications. It is because the high di/dt transition only happens during the hard switching-on transition, and as discussed in section II, the 2DEG of GaN HEMT is pinched off during the whole switching-off transition. However, it is still recommended to make effort on the parasitics optimization and therefore increase the system robustness and also reduce EMI.

The effect of parasitics on GaN HEMT switching performance has been thoroughly discussed in the previous works [10][11]. The traditional package is starting to become the bottleneck of device performance. There is a significant trend for GaN HEMTs to move from traditional through-hole packages to SMT package, such as PQFN, D2PAK or GaN Systems' embedded GaNPX® package.

An IMS-based half-bridge power module consisting of two high-side and two low-side 30 A /650 V GaN HEMTs in parallel is designed and prototyped with 60 A /400 V hard switching on and off capability in [12]. In this paper, a very similar layout strategy is applied to design an IMS-based half-bridge power module consisting of two high-side and two low-side 650 V/60 A GaN HEMTs as shown in Fig.8. A 6-layer structure of driver board and magnetic flux cancelling layout is employed to reduce and balance the stray inductance of both gate driver loops and commutation loops.

Another design consideration is the parasitic capacitance between switching node and BUS+/- nodes introduced by passive components and substrate, e.g. PCB, insulated metal substrate, etc. Unlike hard switching-on applications, the energy stored on parasitic capacitance will not be dissipated in ZVS applications.

Instead, the energy stored on parasitic capacitance will be recycled during the soft switching-on transition. However, additional parasitic capacitance will also lower the system efficiency, as the additional required reactive energy will increase the system RMS current.

Therefore, the considerations of parasitics optimization in ZVS applications are generally the same as in hard switching-on applications, while with more error tolerant margins and more design flexibility.

B. Thermal management

The ultra-fast switching capabilities of GaN, combined with ZVS topologies, enables higher efficiency and power density of power electronic systems, also results in more concentrated heat. Proper package considerations on thermal management are required to enhance overall system performance.

Whether it is in a low-cost PCB or in a complex liquid cooling system, the substrate provides a thermal interconnection between the electrical system and the cooling system, which, is the key in terms of thermal management.

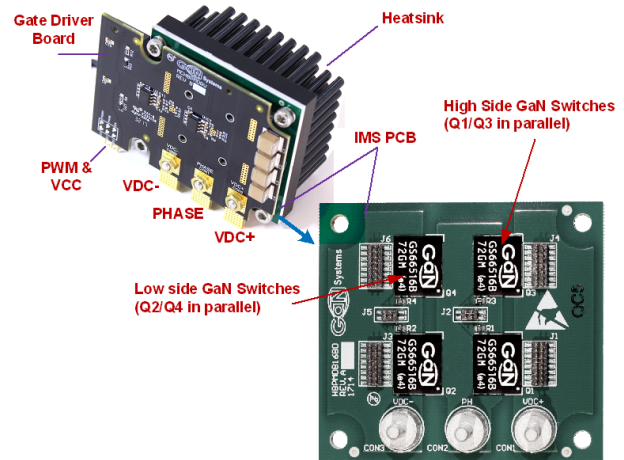


Fig. 8. IMS-based half-bridge power module and its gate driver board.

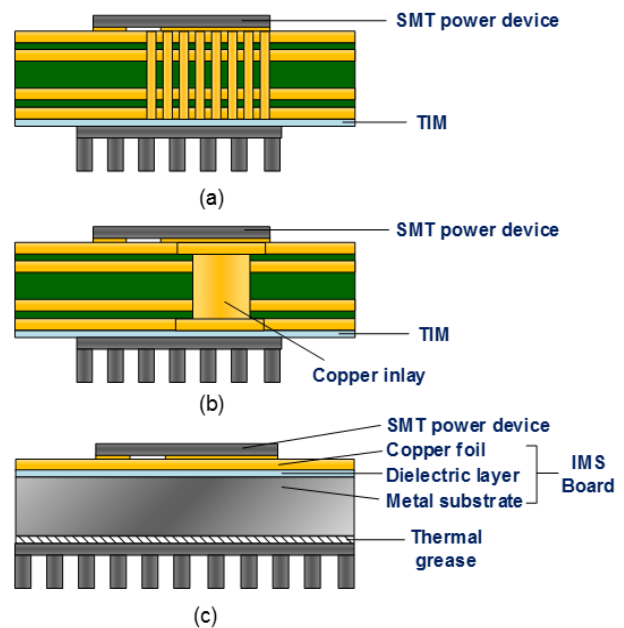


Fig. 9. Thermal design approaches for SMT devices, (a) FR4 PCB cooling with vias, (b) FR4 PCB with Copper inlay, (c) IMS PCB.

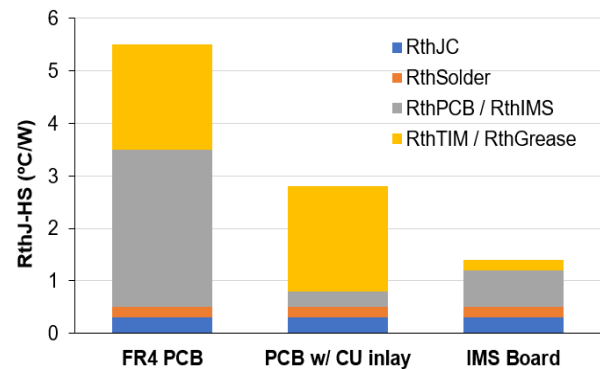


Fig. 10. Junction-to-heatsink thermal resistance comparisons of the above three approaches.

IMS consists of a copper connection layer, a dielectric layer and a metal base. The thickness of the dielectric layer ranges from 0.04 to 0.1 mm. The metal base is usually made of aluminum, which aids heat dissipation and improves system-level cooling. It offers superior thermal conductivity than standard FR4 PCB and is commonly used on the system that has high power where most of heat is concentrated in a small footprint SMT devices [13].

In addition, it also reduces the assembly cost and risk by eliminating manual assembly steps of installing heatsink components and thermal interface material (TIM) sheet for voltage insulation.

The different thermal design approaches for SMT devices and the junction-to-heatsink thermal resistance comparison are given in Fig. 9 and 10, respectively. IMS substrate reduces more than 50% junction-to-heatsink thermal resistance compared with the solution of PCB with Copper inlay, which is selected as the solution for GaN-based power stage.

IV. EXPERIMENTAL VERIFICATION

Double pulse test (DPT) circuitry is widely used to measure the switching loss of the device under test (DUT), which is also a good starting point to estimate the system efficiency. However, this approach does not reflect real world results due to factors such as unbalanced power stage temperature distribution and current distribution between paralleled transistors. On the other hand, creating an exact system to evaluate power semiconductor or power module performance is expensive and time-consuming, especially for high-power applications.

An energy recirculation and storage circuit (ERSC) is employed [14] to evaluate the GaN module under soft switching conditions as shown in Fig.11. Due to the page limitation, the detailed operating principle will not be presented in this paper. Generally speaking, the energy is recirculated inside the circuit, therefore it could emulate the high-power operating condition with a low-power supply only to compensate for system losses, successfully avoiding the use of expensive high-power supply and load. By combining frequency varying and phase shifting control, the inductor RMS current i_{RMS} and switching off current $i_{Switching}$ of DUT can be adjusted separately as (8) (9),

$$i_{RMS} = \frac{V_{DC} \cdot duty}{L_1 \cdot freq} \cdot \sqrt{\frac{(3-2 \cdot duty)}{12}} \quad (8)$$

$$i_{Switching} = \frac{V_{DC}}{L_1} \cdot \frac{duty}{2 \cdot freq} \quad (9)$$

where $freq$ is the switching frequency, and $duty$ is the phase-shift angle between the two phase-legs.

The operation of each switch is exactly symmetrical, and ZVS is achieved in all switching-on transitions. The inductor current and voltage waveforms at 4.5 kVA, 500 kHz is shown in Fig.12. The DC power supply only compensates the loss of the power switches and passive components with an average current of about 200 mA.

Temperature distribution is measured by thermal imager (FLIR-T62101), and the junction temperatures T_J of all the GaN HEMTs is shown in Fig.13.

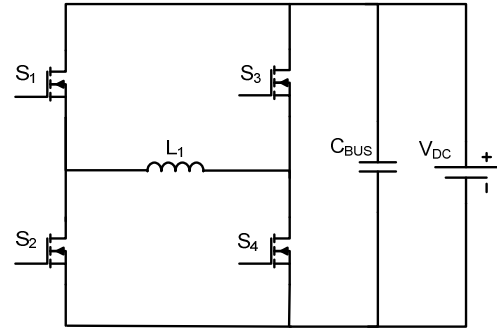


Fig. 11.a. Full power emulation platform schematic

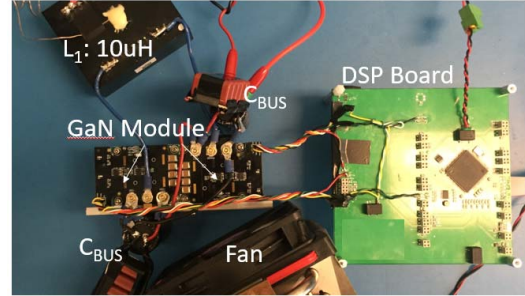


Fig. 11.b. Hardware setup of full power emulation platform

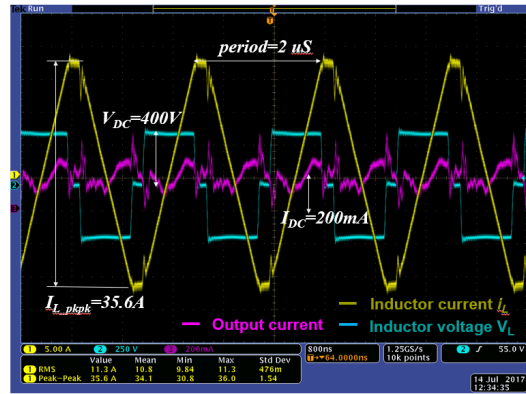


Fig. 12. Waveforms @ 4.5 kVA, $t_D = 60nS$, $V_{DRoff} = -3V$

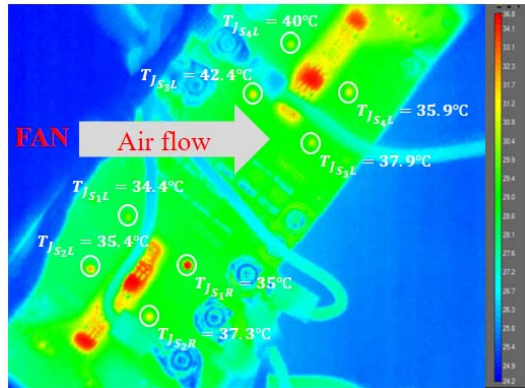


Fig. 13. Temperature Distribution of Power Stage.

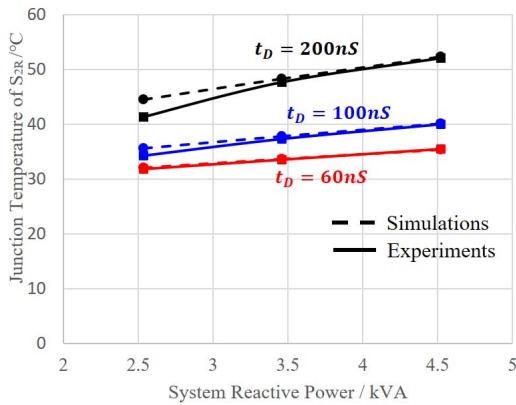


Fig. 14. Junction Temperature Simulation vs. Experiments.

These experiments are aimed to verify the loss model of GaN HEMTs in ZVS applications. A small heatsink and fan is employed in the test. The junction to ambient thermal resistance of single GaN HEMT is measured as 6.6 °C/W, while the junction to heatsink resistance is only 1.6 °C/W. The heatsink and fan has become the bottleneck of system performance. They will be enhanced for the higher power test as a future work.

According to the loss model of GaN HEMTs, the junction temperatures under different deadtime and power are also calculated and compared with experimental results shown in Fig.14.

It is clear that a strong correlation is seen between experimental results (the solid lines) and simulations (the dashed lines). The possible reason for the difference at lower power could be the diversity of dynamic $R_{DS(on)}$, the non-linearity of parasitic capacitance, unbalanced temperature distribution of GaN, etc, which will be explored in the future work.

V. CONCLUSIONS

The design rules of switching off voltage V_{DROff} and deadtime is given based on loss model of GaN HEMTs for ZVS applications. They could also be applied to hard switching topologies, but the deadtime loss and switching-off loss are less dominant compared to switching-on loss in terms of efficiency.

Packaging design considerations on parasitic parameter and thermal management in ZVS applications are discussed. An IMS-based 120 A/650 V half-bridge GaN power module is designed and experimentally evaluated by an ERSC circuit at 500 kHz, 4.5 kVA. A strong correlation between simulation and experimentation is presented verifying both the power module design and GaN loss model.

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