

Dynamic On-state Resistance Evaluation of GaN Devices under Hard and Soft Switching Conditions

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Abstract—Dynamic on-state resistance (R_{DSON}) of two commercial 600V/650V GaN power devices under hard and soft switching conditions are extracted and compared. In addition to standard double-pulse tester (DPT), a triangular current mode (TCM) soft switching circuit is built to simulate the actual applications including double-pulse and multi-pulse operating modes. The comparison between hard and soft switching conditions reveals that the devices with different internal structures exhibit significantly different dependence on the off-state voltage and frequency under hard and soft switching conditions, which should be taken fully into account for converter design and loss estimation. To avoid misestimation, a multi-pulse measurement need to be taken into considerations when evaluating R_{DSON} of GaN devices.

Keywords—GaN power device; Dynamic on-state resistance; Current collapse; Hard switching; Soft switching

I. INTRODUCTION

GaN power devices exhibit great performance in high-frequency applications. However, these devices often suffer from current collapse, leading to an increase dynamic R_{DSON} after switching from high-bias off-state. The increase of dynamic R_{DSON} originates primarily from electrons trapping into surface traps and buffer traps in the gate-to-drain access region induced by gate leakage current in the off-state [1] or hot electrons injection from channel in the switching transient state [2].

Due to uncertain R_{DSON} , it is no longer suitable for GaN devices to use R_{DSON} parameters from the datasheet (or curve tracer) as a guideline to predict the conduction losses. In addition to the impact of junction temperature, the R_{DSON} variation coefficient must be taken into consideration when designing GaN based power converters.

There are mainly two kinds of methods for dynamic R_{DSON} measurement currently. One is the pulsed I - V measurement using equipment, which mainly focus on device characteristics and mechanism analysis (e.g. [3, 4]). However, this method is not cost-efficient and induce high contact resistance as well as long response time. The other one is using a test circuit aiming at device applications (e.g. [5-14]).

A general used circuit for dynamic R_{DSON} extraction is a double pulse tester (DPT) where the DUT (device under test) switches under hard switching condition [8, 10-12]. The impact

of key operation parameters on dynamic R_{DSON} including off-state time, off-state voltage, drain current, temperature, frequency, duty cycle and gate voltage are investigated in those works. However, the impact of switching conditions on dynamic R_{DSON} has seldom been discussed. Reference [5] compared the dynamic R_{DSON} under hard and soft switching conditions with off-state voltage. However, the test circuit used resistance load, making it slightly deviate from actual applications. Reference [10] mainly focus on gate characteristics and provided a recommended V_{GS} in hard and soft switching respectively. Reference [15] compared the dynamic R_{DSON} of the devices in development phase under the two switching conditions by independently controlling the gate and drain pulses.

Moreover, GaN device's turn-on switching loss is much higher than turn-off switching loss, making the device suitable for zero voltage turn-on circuit [16]. Therefore, for application perspective, conventional DPT or other hard switching test circuit is not sufficient for a comprehensive investigation of dynamic R_{DSON} . An additional soft switching test circuit including pulsed and continuous operating modes is indispensable.

This paper provides a simple and effective method for comprehensive investigation of dynamic R_{DSON} including hard and soft switching conditions. Compared to other soft switching test circuits [5, 7, 17], the proposed circuit corresponds more to the reality because it bases on a widely used TCM soft-switching technics [18]. It has fewer components and could be easily implemented from conventional DPT.

Although GaN device manufacturers have made much progress in mitigating current collapse (e.g. use field plates) [19], commercial GaN devices still suffer from this phenomenon. In this paper, two types of commercial GaN devices representing the state of art are tested and compared with the presented setup. The key parameters of DUT are shown in Table I, where a Si MOSFET is measured for comparison.

The paper is organized as follows. Section II describe the proposed test methods including hard and soft switching test circuit with the presented setup. In Section III and Section IV, the experimental results in double-pulse test and multi-pulse

test are shown and discussed respectively. Section V concludes the paper.

TABLE I. SUMMARY OF DEVICE UNDER TEST

| Parameters | Device A | Device B | Device C |
|---------------------------|--------------------|-----------------|-----------|
| Voltage/Current Rating | 600V/13A | 650V/30A | 600V/35A |
| Technology | E-mode (X-GaN GIT) | E-mode (p-gate) | CoolMOST™ |
| Package | DFN 8×8 | GaNPTM 4 | TO-220 |
| $R_{DS(on)}$ ^a | 140mΩ | 50mΩ | 60mΩ |

^a. The $R_{DS(on)}$ values are obtained from data sheet

II. TEST SETUP AND DESIGN CONSIDERATIONS

Two types of test circuit are built for $R_{DS(on)}$ evaluation: a generally used DPT with half-bridge configuration for hard switching condition and the proposed TCM test circuit for soft switching condition. The two test circuits are integrated into one test board to avoid the device being repeatedly soldered and desoldered between different test boards.

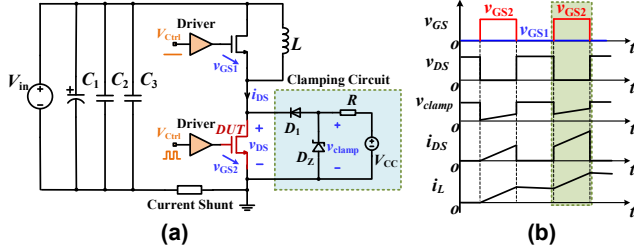


Fig. 1. Hard-switching test. (a) Double-pulse test circuit in half-bridge configuration with clamping circuit. (b) Double-pulse control signals and related waveforms.

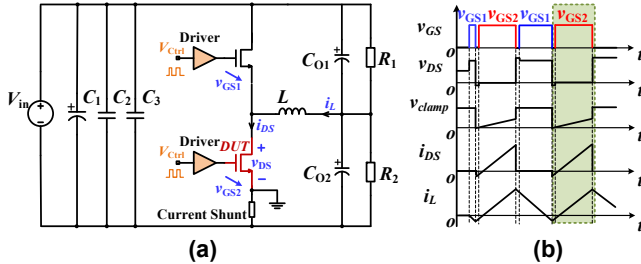


Fig. 2. Soft-switching test. (a) Proposed TCM test circuit (clamping circuit not shown here). (b) Double-pulse control signals of DUT and related waveforms.

Fig. 1(a) shows the DPT circuit and schematic waveforms. The measurement region starting from the second pulse of the DUT is highlighted in Fig. 1(b). Details about measurement issues of DPT can be found in [20, 21] and are not involved here. Fig. 2(a) shows the proposed TCM soft switching test circuit. It is similar to a synchronous Buck converter but the output capacitor has initial voltage due to the series of C_{O1} and C_{O2} . Therefore the DUT can be forced to operate in double-pulse or multi-pulse mode without additional precharge process of the output capacitor. The capacitance of C_{O1} and C_{O2} are large enough to keep the voltage of them constant during the μs level test. R_1 , R_2 are used to determine the initial voltages of

C_{O1} and C_{O2} (i.e. the duty cycle) in multi-pulse test. In this work, the value of R_1 , R_2 are selected identical to realize 50% duty cycle. The control signals and related waveforms with measured part highlighted are shown in Fig. 2(b). By controlling the on-state time of the top-side device in the first pulse, a small reverse drain current could flow through DUT before turn-on to realize ZVS.

$R_{DS(on)}$ is determined by measuring on-state voltage and drain current. In order to measure the low on-state voltage comparing with the high off-state voltage, a fast and accurate clamping circuit is required. Several circuits for high accuracy measurement of on-state voltage are proposed in previous works[5-7, 9, 22-24]. The clamping circuit in [22] was selected and simplified for $R_{DS(on)}$ evaluation in this paper. The clamping circuit is shown in Fig. 1(a), the voltage drop v_{clamp} across the Zener diode D_Z is measured instead of v_{DS} . Different to [22], the diode forward voltage V_{D1} is calibrated rather than use a constant value since the variation of V_{D1} will affect measurement accuracy especially for low $R_{DS(on)}$ devices. The I - V characteristics of the diode are measured by HP4155B semiconductor parameter analyzer to obtain a fitting formula between forward voltage V_F and forward current I_F . To avoid junction temperature rising of D_1 , the value of R is selected carefully to keep the forward current between 20mA and 25mA. The first available $R_{DS(on)}$ data can be taken after ~ 150 ns from turn-on. The delay time is optimized with full considerations by using a SiC Schottky diode with small junction capacitance and a small clamping loop with minimal parasitic inductance.

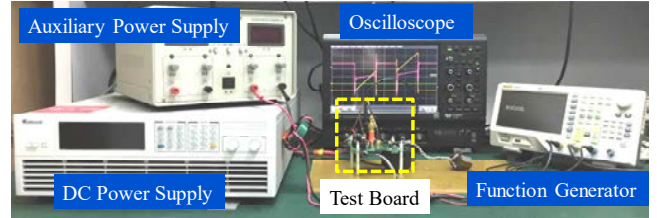


Fig. 3. Test setup for dynamic $R_{DS(on)}$ evaluation.

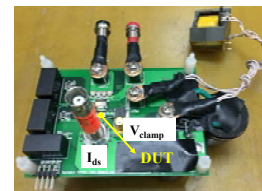


Fig. 4. Photo of the four-layer PCB test board.

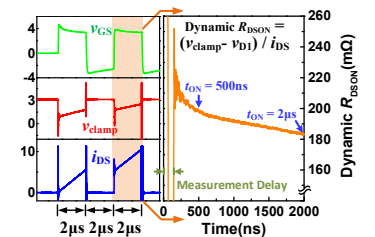


Fig. 5. Experimental waveforms and the test method.

Fig. 3 depicts the test system setup and Fig. 4 shows the photo of the four-layer PCB test board. The gate loop and power loop of the half bridge circuit are designed as small as possible to minimize parasitic inductances. The drain current is measured with a 0.1Ω coaxial shunt (SSDN-10) from T&M Research Inc. An SMA connector with coaxial cable is used to sense the clamping voltage. For more accurate measurement of $R_{DS(on)}$, it is necessary to ensure that the propagation delay between voltage and current probes are calibrated before

measurement. The V-I alignment is achieved by removing the bottom device with a low inductance resistor and measuring the voltage and current of the resistor at the same time [21].

III. DOUBLE-PULSE TEST UNDER HARD AND SOFT SWITCHING CONDITIONS

Fig. 5 depicts the method of dynamic $R_{\text{DS(on)}}$ evaluation in double-pulse operating mode including the measurement delay time. The DUT is turned on for $2\mu\text{s}$ during the first pulse. After a short interval of $2\mu\text{s}$, the DUT is turned on again due to the second $2\mu\text{s}$ pulse. Dynamic $R_{\text{DS(on)}}$ variation are measured and calculated during the second on-state time highlighted in Fig. 5. The dynamic $R_{\text{DS(on)}}$ at 500ns and $2\mu\text{s}$ after turn on are extracted for comparison. For each DUT, the $R_{\text{DS(on)}}$ is measured under different voltage stresses from 50V to 400V (50V per step) with the same drain current. For Device A, the drain current increases from 0 to 5A during the first $2\mu\text{s}$ pulse and 5A to 10A during the second $2\mu\text{s}$ pulse in hard switching condition. When operating in soft switching condition, the drain current increases from a small reverse current up to 10A during each $2\mu\text{s}$ pulse. For Device B and Device C, the drain current increases from 0 to 10A during the first $2\mu\text{s}$ pulse and 10A to 20A during the second $2\mu\text{s}$ pulse in hard switching condition. When operating in soft switching condition, the drain current increases from a small reverse current up to 20A during each $2\mu\text{s}$ pulse.

Fig. 6(a)-(e) shows the measured $R_{\text{DS(on)}}$ variation of the three DUTs in hard and soft switching conditions respectively. The time point when v_{clamp} begin to fall is set as the origin of the time axis. Therefore, the missing $R_{\text{DS(on)}}$ data during the initial part of time axis suggest the measurement delay time, which is within 150ns . In Fig. 6(b), (d), (f), the missing $R_{\text{DS(on)}}$ data time is longer than 150ns due to the deadtime set as 100ns in soft switching condition. The large oscillations at the first 500ns originate from the errors caused by small drain to source current i_{DS} at the beginning of conduction in soft switching condition, which is used as denominator when calculate the $R_{\text{DS(on)}}$.

The measured $R_{\text{DS(on)}}$ values are normalized by the static $R_{\text{DS(on)}}$ at room temperature from the datasheet. Dynamic/Static $R_{\text{DS(on)}}$ values at 500ns and 2000ns after turn on with different voltage stresses under hard and soft switching conditions are depicted in Fig. 7.

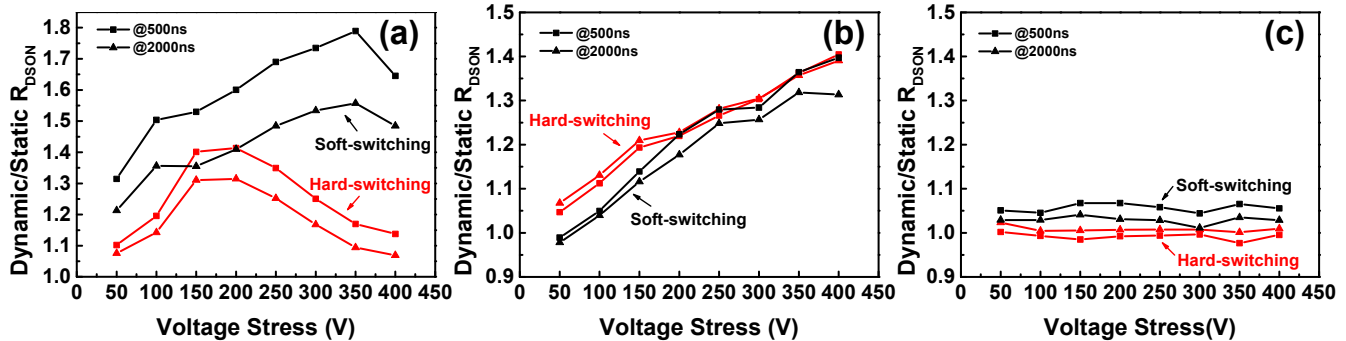


Fig. 7. Dynamic/Static $R_{\text{DS(on)}}$ under different voltage stresses in hard- and soft-switching conditions. Dynamic/Static $R_{\text{DS(on)}}$ values at 500ns and 2000ns after turn-on are plotted respectively. (a) Device A; (b) Device B; (c) Device C.

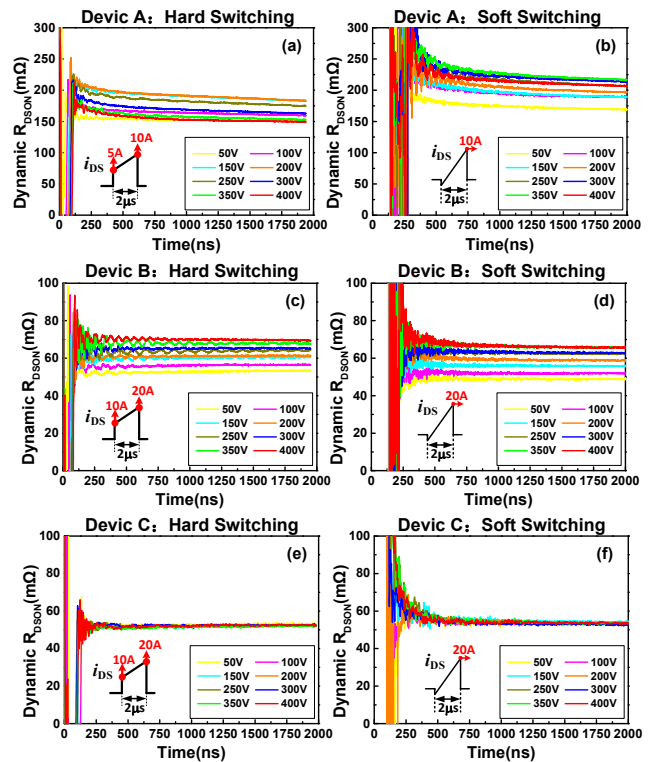


Fig. 6. Dynamic $R_{\text{DS(on)}}$ under hard and soft switching conditions with different voltage stresses from 50V to 400V (50V per step) with the same drain current. (a), (b) Device A; (c), (d) Device B; (e), (f) Device C. Inset: drain current variation during the measurement period.

It is obvious that the three devices have different $R_{\text{DS(on)}}$ variation patterns with voltage stress. As expected, there is no dynamic $R_{\text{DS(on)}}$ effect in Device C, the Si CoolMOS (Fig. 7(c)). For Device B, the dynamic $R_{\text{DS(on)}}$ under hard and soft switching conditions exhibit similar variation pattern with off-state voltage but a lower $R_{\text{DS(on)}}$ is observed under soft switching condition. The results are consistent with a general understanding of GaN devices from previous works [5, 10, 17] and the phenomenon is attributed to hot electron effect [2].

In contrast, Device A shows different characteristics. The relationship between $R_{\text{DS(on)}}$ and voltage stress in hard switching is non-monotonic, surprisingly, it exhibits nearly static $R_{\text{DS(on)}}$ under high voltage stress (400V). However, an

obvious increase of dynamic $R_{\text{DS(on)}}$ under soft switching condition is observed, which is more severe under high voltage switching condition (400V). Similar phenomenon has been shown in [15] where the GaN HFETs under test showed higher current collapse under soft switching condition, but the physical mechanism is different due to the different device structures of Device A and DUT in [15].

Compared with Device B, Device A is fabricated with an additional p-GaN drain (PD) beside the drain electrode [25]. This structure is helpful to eliminate current collapse since the injected holes from PD at high voltage stress can effectively release the trapped electrons near the drain. However, the performance of PD is affected by switching conditions as is shown in our experimental results. When operating under soft switching condition, the hole injection effect of PD is weakened, which accordingly lead to higher dynamic $R_{\text{DS(on)}}$.

The experimental results reveal the impact of switching conditions on dynamic $R_{\text{DS(on)}}$ due to different device structures. Therefore, for current commercial GaN power devices, it is not exactly proper to evaluate current collapse characteristics without considering switching conditions, which otherwise may lead to misunderstanding of dynamic $R_{\text{DS(on)}}$ and errors in loss estimation.

IV. MULTI-PULSE TEST UNDER HARD AND SOFT SWITCHING CONDITIONS

The trapping and detrapping effect of GaN device is similar to the charging and discharging process of series of RC units with specific time constants [9, 26]. It suggests that the dynamic $R_{\text{DS(on)}}$ need time to reach steady state and the response time depends on frequency. Therefore, a continuous multi-pulse operation mode with different frequencies need to be taken into considerations.

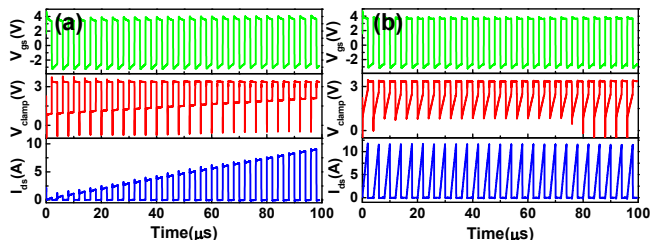


Fig. 8. Multi-pulse test waveforms (a) under hard switching condition and (b) under soft switching condition at $V_{\text{DS}}=100\text{V}$ and $f=250\text{kHz}$.

In this operation mode, only Device A and Device B are tested. Fig. 8 shows the measured waveforms and depicts the method of dynamic $R_{\text{DS(on)}}$ evaluation in multi-pulse operating mode. The total operating time is limited to $100\mu\text{s}$ to avoid self-heating. For each DUT, the dynamic $R_{\text{DS(on)}}$ is measured at 250kHz, 500kHz and 1MHz with the same drain current. For hard switching, the drain current increases during each on-state time up to the determined final value in the final cycle. For soft switching, the drain current increase from zero to the final value during each cycle. The drain current final value is determined as 10A, 20A for Device A and Device B respectively. Meanwhile, the impact of frequency on the dynamic $R_{\text{DS(on)}}$ at different voltage stresses of 100V and 400V

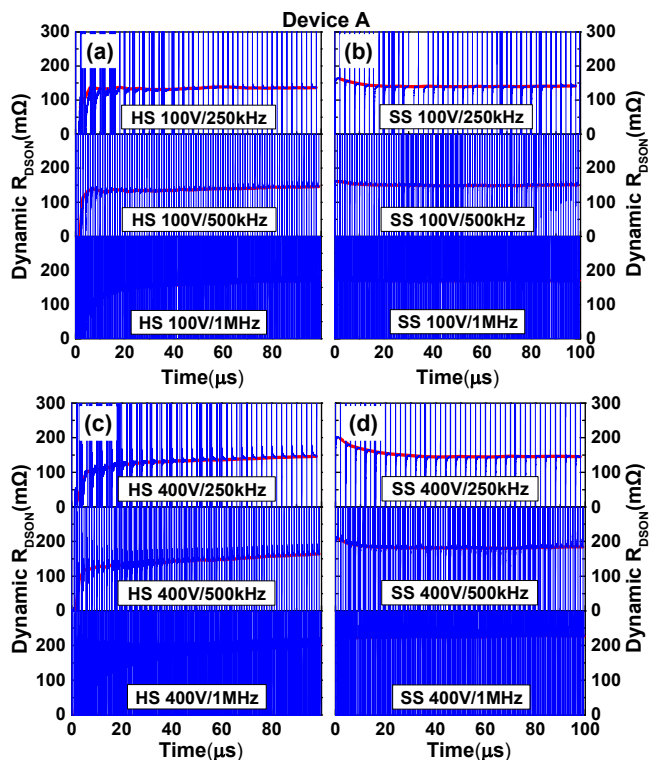


Fig. 9. Dynamic $R_{\text{DS(on)}}$ variation of Device A during the total $100\mu\text{s}$ test period under hard switching (HS) and soft switching (SS) conditions with different frequencies. (a), (b) at 100V stress; (c), (d) at 400V stress.

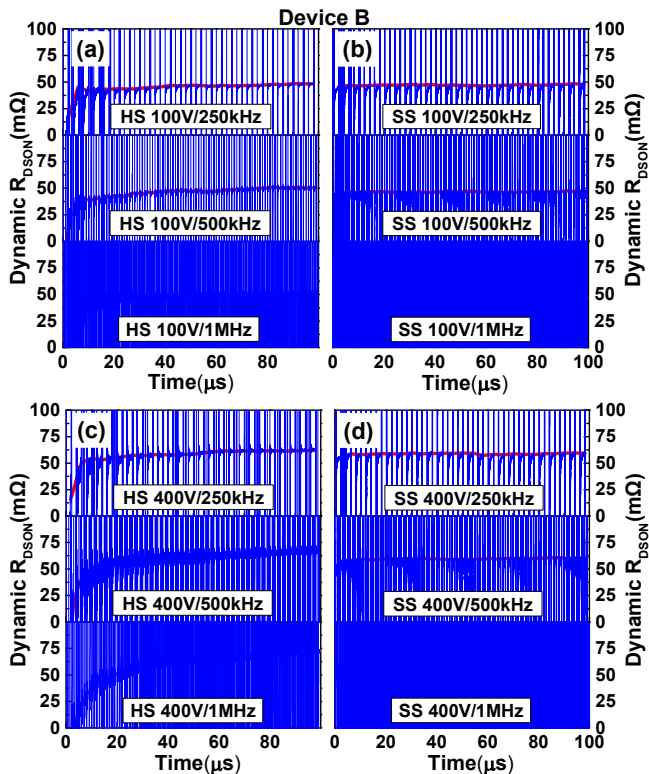


Fig. 10. Dynamic $R_{\text{DS(on)}}$ variation of Device B during the total $100\mu\text{s}$ test period under hard switching (HS) and soft switching (SS) conditions with different frequencies. (a), (b) at 100V stress; (c), (d) at 400V stress.

is observed. The duty cycle in all case is set as 50% to ensure the same stress time of DUT operating at different frequencies. Dynamic $R_{\text{DS(on)}}$ during the total 100 μs test period are shown in Fig. 9 and Fig. 10. The average $R_{\text{DS(on)}}$ during the last 20ns of the final conduction period is calculated and plotted in Fig. 11 for comparison.

An increasing $R_{\text{DS(on)}}$ is observed in hard switching condition due to the increasing drain current. However, it will not affect the comparison results since the drain current during the last 20ns of the final conduction period can be seen as constant and the same in hard and soft switching condition. It is noteworthy that for device A under soft switching condition, shown in Fig. 9(b), (d), the dynamic $R_{\text{DS(on)}}$ decrease gradually to a steady value with the increase of pulse number. The pulse numbers needed to reach the steady state are different with frequency and voltage stress, suggesting that the traditional test method using only one or two pulses is not sufficient for dynamic $R_{\text{DS(on)}}$ evaluation of GaN devices due to the trapping and detrapping effect.

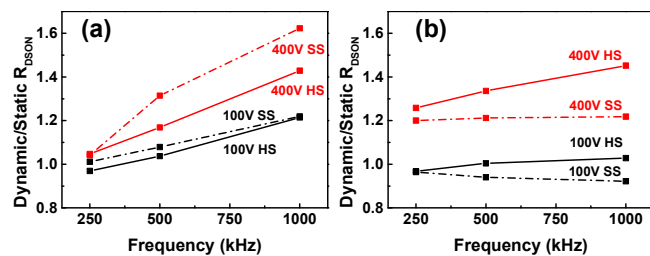


Fig. 11. Dynamic/Static $R_{\text{DS(on)}}$ with different frequencies at 100V and 400V under hard and soft switching conditions. (a) Device A; (b) Device B.

It is well acknowledged that higher frequency results in an increase of the dynamic $R_{\text{DS(on)}}$ and the increase is more apparent with higher voltage stress due to more severe trapping effect [12]. Experimental results show that the impact of frequency depends on switching conditions and DUT structure, shown in Fig. 11. For Device A with PD structure, $R_{\text{DS(on)}}$ increase with frequency in both hard and soft switching condition and a higher $R_{\text{DS(on)}}$ is observed in soft switching condition. The difference of $R_{\text{DS(on)}}$ in the two switching conditions is more obvious in high voltage and high frequency operation, suggesting a weakened function of PD structure in soft switching condition, especially for high voltage and high frequency applications. For Device B, the measured $R_{\text{DS(on)}}$ is relatively insensitive to the switching frequency in soft switching condition since it suffers no hot electron effect which usually occurs in hard switching condition.

V. CONCLUSIONS

This paper provides a simple and effective method for comprehensive investigation of dynamic $R_{\text{DS(on)}}$ under hard and soft switching conditions including double-pulse and multi-pulse operating modes.

Experimental results and discussion of the two commercial GaN devices reveal the impact of switching conditions on dynamic $R_{\text{DS(on)}}$ due to device structures. Therefore, for current commercial GaN power devices, it is not exactly proper to evaluate dynamic $R_{\text{DS(on)}}$ characteristics without considering

switching conditions, which otherwise may lead to misunderstanding of dynamic $R_{\text{DS(on)}}$ and errors in loss estimation. Moreover, experiment results show that the traditional test method using only one or two pulses is not sufficient for dynamic $R_{\text{DS(on)}}$ evaluation of GaN devices from the application point of view.

This paper aims to further enhance the understanding of the dynamic $R_{\text{DS(on)}}$ under different switching conditions and the analysis results can provide valuable information for GaN based power converter designs.

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REFERENCES

- [1] R. Vetry, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaIn/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 48, pp. 560-566, 2001.
- [2] I. Hwang, J. Kim, S. Chong, H. S. Choi, S. K. Hwang, J. Oh, *et al.*, "Impact of Channel Hot Electrons on Current Collapse in AlGaIn/GaN HEMTs," *IEEE Electron Device Letters*, vol. 34, pp. 1494-1496, 2013.
- [3] D. Jin and J. A. del Alamo, "Mechanisms responsible for dynamic ON-resistance in GaN high-voltage HEMTs," in *Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on*, 2012, pp. 333-336.
- [4] D. Jin and J. A. del Alamo, "Methodology for the study of dynamic ON-resistance in high-voltage GaN field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 60, pp. 3190-3196, 2013.
- [5] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of Dynamic On-Resistance in GaN Transistors: Under Soft- and Hard-Switching Conditions," in *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2011, pp. 1-4.
- [6] R. Gelagaev, P. Jacqmaer, and J. Driesen, "A fast voltage clamp circuit for the accurate measurement of the dynamic on-resistance of power transistors," *IEEE Transactions on Industrial Electronics*, vol. 62, pp. 1241-1250, 2015.
- [7] G. Cao, A. Ansari, and H. J. Kim, "A New Measurement Circuit to Evaluate Current Collapse Effect of GaN HEMTs Under Practical Conditions," *IEEE Transactions on Instrumentation and Measurement*, vol. 64, pp. 1977-1986, 2015.
- [8] N. Badawi, O. Hilt, E. Bahat-Treidel, J. Böcker, J. Würfl, and S. Dieckerhoff, "Investigation of the dynamic ON-state resistance of 600 V normally-off and normally-on GaN HEMTs," *IEEE Transactions on Industry Applications*, vol. 52, pp. 4955-4964, 2016.
- [9] K. Li, P. Evans, and M. Johnson, "GaN-HEMT dynamic ON-state resistance characterisation and modelling," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1-7.
- [10] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic RON Characterization and Circuit Design Considerations," *IEEE Transactions on Power Electronics*, vol. 32, pp. 5539-5549, 2017.
- [11] T. Yao and R. Ayyanar, "A Multifunctional Double Pulse Tester for Cascode GaN Devices," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 9023-9031, 2017.
- [12] Y. Cai, A. J. Forsyth, and R. Todd, "Impact of GaN HEMT dynamic on-state resistance on converter performance," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1689-1694.
- [13] O. C. Spro, D. Pefitsis, O. M. Midtgard, and T. Undeland, "Modelling and quantification of power losses due to dynamic on-state resistance of GaN E-mode HEMT," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2017, pp. 1-6.
- [14] T. Cappello, A. Santarelli, and C. Florian, "Dynamic $R_{\text{DS(on)}}$ Characterization Technique for the Evaluation

- of Thermal and Off-State Voltage Stress of GaN Switches," *IEEE Transactions on Power Electronics*, vol. PP, pp. 1-1, 2017.
- [15] J. Joh, N. Tipirneni, S. Pendharkar, and S. Krishnan, "Current collapse in GaN heterojunction field effect transistors for high-voltage switching applications," in *2014 IEEE International Reliability Physics Symposium*, 2014, pp. 6C.5.1-6C.5.4.
- [16] X. Huang, T. Liu, B. Li, F. C. Lee, and Q. Li, "Evaluation and applications of 600V/650V enhancement-mode GaN devices," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 113-118.
- [17] T. Yao and R. Ayyanar, "A Multi-functional Double Pulse Tester for Cascode GaN Devices," *IEEE Transactions on Industrial Electronics*, vol. PP, pp. 1-1, 2017.
- [18] X. Huang, Z. Liu, F. C. Lee, and Q. Li, "Characterization and Enhancement of High-Voltage Cascode GaN Devices," *IEEE Transactions on Electron Devices*, vol. 62, pp. 270-277, 2015.
- [19] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 707-719, 2016.
- [20] J. B. Witcher, "Methodology for switching characterization of power devices and modules," M.S thesis, Dept. Electrical Engineering, Eng, Virginia Polytechnic Institute and State Univ., Blacksburg, USA, 2003.
- [21] Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, *et al.*, "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 2534-2541.
- [22] N. Badawi and S. Dieckerhoff, "A new Method for Dynamic Ron Extraction of GaN Power HEMTs," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2015, pp. 1-6.
- [23] E. Marcault, D. Trémouilles, K. Isoird, F. Morancho, and M. Gavelle, "Dynamic of power-GaN-HEMT Electrical Parameters: Why DC characterization might be misleading," in *Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016 18th European Conference on, 2016, pp. 1-6.
- [24] L. Ren, Q. Shen, and C. Gong, "A voltage clamp circuit for the real-time measurement of the on-state voltage of power transistors," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1-7.
- [25] S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, H. Okita, T. Morita, *et al.*, "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 41-44.
- [26] J. Böcker, H. Just, O. Hilt, N. Badawi, J. Würfl, and S. Dieckerhoff, "Experimental analysis and modeling of GaN normally-off HFETs with trapping effects," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-10.