Impedance-based Analysis of DC link Control in Voltage Source Rectifiers

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***Abstract*— This paper analyzes the dynamics influences of the outer dc link control in the voltage source rectifiers based on the impedance model. The ac-dc interactions are firstly presented by means of full order small signal model in *dq* frame, which shows the input voltage and load condition are the two main factors. Impedance model is then derived and the effects caused by the dc link voltage control are discussed. Oscillations in low frequency range may appear due to the dc link voltage control. Three case studies are presented, and subsequently validated in experimental tests. The experimental results demonstrate the effectiveness of the impedance model and staility analysis.**

Keywords—impedance stability; dc link voltage control; voltage source rectifiers;

I. INTRODUCTION

Three-phase Pulse-Width-Modulation (PWM) voltage source rectifiers (VSRs) are increasingly being used in ac-dc power conversion for achieving high power factor and low harmonics [1]. Conventionally, the control of VSR is performed in *dq* frame to achieve a constant dc link voltage and fast ac current dynamics, consisting of the outer dc link voltage control loop and inner current control loop [2]-[4]. The dynamics of the control loops together with the power grid may cause oscillations, even instability. The interactions between the control loops and the power grid tend to introduce additional resonances in certain frequency range. To deal with this issue, the impedance modeling methods have been developed, which use the impedance ratio to show the stability of the overall system.

Lots of impedance-based analysis have been carried out for the grid-connected converter system [4]-[12], which can be regarded as only considering the effects of the inner current control loop. The stability issues are mainly focused on the inner current control with LCL filters [7]-[9], where the effects of current controller and digital time delay are thoroughly discussed. However, a few works have been reported to include the outer dc link voltage controller [5], [10]-[12]. The dc link control loop would introduce negative impedance in the low frequency range, which results in the unexpected oscillations near the fundamental frequency [4], [10].

Normally, the bandwidth(BW) of the dc link control loop is much lower than the inner current control, therefore, it is common to ignore the ac-dc interactions by neglecting the dc link dynamics in the analysis of current control. The design of the dc link voltage control loop is based on the active power balance with the energy stored in the dc capacitor [5], [13]. Nevertheless, the accuracy of this model is not clear, especially on the stability analysis and control parameters design of dc link control loop. In case of requiring fast dc link response, which means a high BW of dc link control, the dc link impacts can no longer be ignored. Due to the nonlinearity of the system, the ac dynamics would be influenced by the dc link, varying with the grid and load condition. The neglected ac-dc interactions may cause inaccurate stability prediction.

Moreover, the negative impedance found in [5] is caused by the linearization of *d*-axis current reference. By unifying the current reference with grid voltage, it would introduce a negative term after linearization, which further leads to negative input admittance. Thus, it can be eliminated by directly giving the current reference without grid voltage compensation. Yet, the contrary results are obtained in [10], [12], where the negative impedance still can be observed. It is explained as direct results of the constant power load dynamics of VSR. The in-depth mechanism is not clearly presented. Furthermore, only *d*-*d* channel is discussed and the coupling in *dq* frame and the ac-dc interactions are overlooked in [10], [12], which cannot reveal the relations between the negative impedance and the stability.

This paper investigates impedance shaping effects of the dc link voltage control, and further predict the stability of the dc link voltage control. Based on the full order small signal model, the ac-dc interactions are obtained, which are closely related to the input voltage and the load condition. Stability analysis of the VSR without grid variation is given as the sufficient condition of the impedance-based analysis. Furthermore, the impedance shaping effects of the dc link control is discussed. Three cases with different BW of the dc link voltage control are presented. It is shown that the negative impedance is caused by the energy stored in the ac inductor, which may interact with the grid impedance in order that generating resonances in the low frequency range. Experimental results are given to validate the effectiveness of the impedance model and the stability analysis.

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II. Modelling and Control of Voltage Source Rectifiers

A. System Description

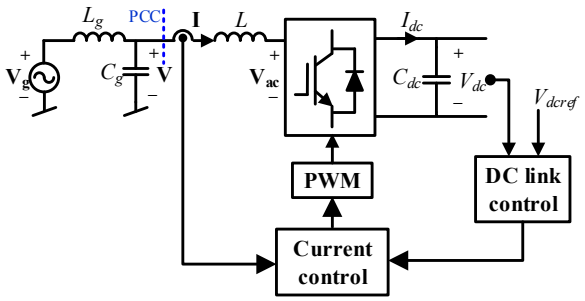


Fig. 1. Main circuit and control system of a three-phase VSR.

Fig. 1 shows the diagram of a three-phase VSR, where a input L-filter and a LC-type grid impedance is considered at the ac side. The dc link is connected through a capacitor to a dc load. The cascade controllers are implemented in the dq frame, where the dc link voltage control generates the d-axis reference of the current control. Both the dc link voltage control and the current control are realized with Proportional + Integral (PI) controller. Table I provides the main circuit parameters.

B. Small Signal Model

The small signal model can be represented by the transfer function matrices block diagram shown in Fig. 2, where $\hat{x}$ is the perturbation near the quiescent operation point x. In the plant of the VSR, $\mathbf{G_{p\text{-}dc}}$ is the transfer function matrix from duty cycle vector to dc link voltage, $\mathbf{G_{p\text{-}ac}}$ is the transfer function matrix from duty cycle vector to input current vector and $\mathbf{Y_{op}}$ is the open loop input admittance in ac side. In the control part, $\mathbf{G_{c\text{-}ac}}$ is the current controller and $G_{c\text{-}dc}$ is the dc link voltage controller.

The small signal model of the plant part can be further presented in Fig. 3, which represents the dynamics from the duty cycle to the outputs. $\mathbf{I}$, $\mathbf{G_{DQ}}$, Z_{dc} and $\mathbf{Y_{ac}}$ represent the

Table I Main circuit parameters

Electrical parameters		Value (p.u.)
Grid voltage (line to line)	V_g	400 V (1), 50 Hz (1)
Dc link voltage	V_{dc}	700 V (1.75)
Grid input current	P	7.5 kw (1)
	Q	0 var (0)
Grid impedance	L_g	3 mH (0.044)
	C_g	20 μF (0.134)
Input L-filter	L	5 mH (0.074)
Dc link capacitor	C_{dc}	3000 μF (20.106)
Swtching frequency	f_s	10 kHz (200)
Sampling time	T_s	100 μs (0.005)

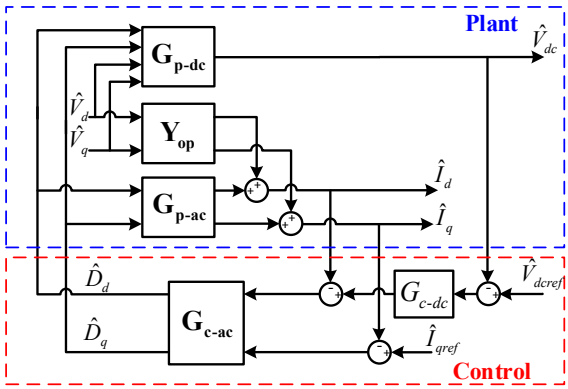
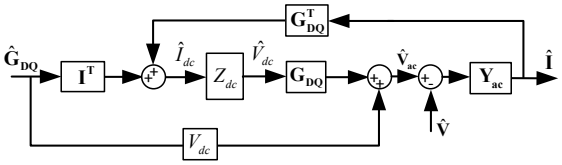


Fig. 2. Small signal model of VSR.

$$\mathbf{G_{p\text{-}ac}}=\begin{bmatrix} G_{dd} & G_{dq} \\ G_{qd} & G_{qq} \end{bmatrix}=\begin{bmatrix} -\frac{V_{dc}}{L}\dfrac{s+\frac{I_{dc}}{C_{dc}V_{dc}}}{s^2+\omega_1^2+\frac{D_d^2+D_q^2}{LC_{dc}}} & -\frac{V_{dc}}{L}\frac{\omega_1}{s}\dfrac{s+\frac{I_{dc}}{C_{dc}V_{dc}}}{s^2+\omega_1^2+\frac{D_d^2+D_q^2}{LC_{dc}}} \\ \dfrac{D_qI_d+\omega_1C_{dc}V_{dc}}{LC_{dc}}\dfrac{1}{s^2+\omega_1^2+\frac{D_d^2+D_q^2}{LC_{dc}}} & -\frac{V_{dc}}{L}\frac{1}{s}\dfrac{s^2+\frac{D_d^2}{LC_{dc}}}{s^2+\omega_1^2+\frac{D_d^2+D_q^2}{LC_{dc}}} \end{bmatrix} \tag{1}$$

$$\mathbf{G_{ac\text{-}dc}}=[G_d \;\; G_q]=\begin{bmatrix} \dfrac{LI_d}{C_{dc}V_{dc}}\dfrac{-s+\frac{V_d}{LI_d}}{s+\frac{I_{dc}}{C_{dc}V_{dc}}} & 0 \end{bmatrix} \tag{2}$$



$$\mathbf{G_{DQ}}=[D_d \;\; D_q] \quad \mathbf{I}=[I_d \;\; I_q]$$

$$Z_{dc}=\frac{1}{sC_{dc}} \quad \mathbf{Y_{ac}}=-\frac{1}{L}\begin{bmatrix} \frac{s}{s^2+\omega^2} & \frac{\omega}{s^2+\omega^2} \\ \frac{-\omega}{s^2+\omega^2} & \frac{s}{s^2+\omega^2} \end{bmatrix}$$

Fig. 3. Small signal model of voltage source rectifier with dc link.

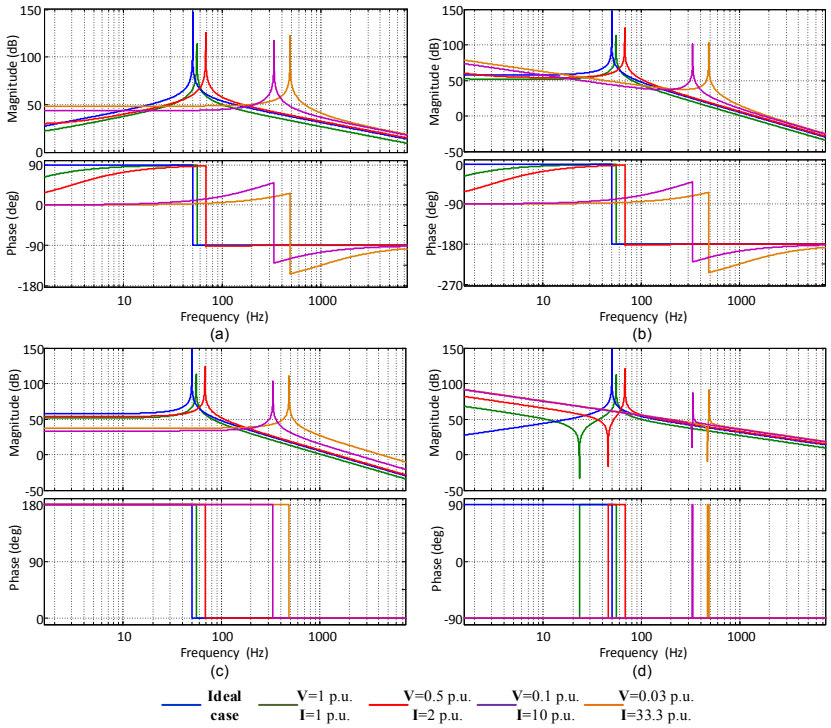


Fig. 5. Frequency response of the inner control loop plant including ac-dc interactions, $\mathbf{G_{p\text{-}ac}}$. (a) $G_{dd.}$ (b) $G_{dq.}$ (c) $G_{qd.}$ (d) G_{qq}

space vector of input current, the space vector of the duty cycle, dc capacitor plant and ac L-filter plant. It is noted that the ac-dc interactions are resulted from the admittance of the ac side $\mathbf{Y_{ac}}$ and the impedance of the dc side Z_{dc}, which build the relationship between the current flow and the voltage flow. Assuming the VSR is operating with unity power factor and the load is an ideal dc current source, the small signal model can be simplified as shown in Fig. 4, where $\mathbf{Y_{op}}$ is the open loop input admittance and $\mathbf{G_{ac\text{-}dc}}$ is the transfer function matrix from input current vector to dc link voltage.. The expression of $\mathbf{G_{p\text{-}ac}}$ and $\mathbf{G_{ac\text{-}dc}}$ are shown in (1) and (2).

From (2), it can be obtained that the pole in G_d, located at $-I_{dc}/C_{dc}V_{dc}$, is caused by the linearization of the energy stored in the dc link capacitor. Besides, the instantaneous power of the input L-filter introduces a zero at $-V_d/LI_d$, which is a right half plane (RHP) zero. It leads to the non-minimal-phase property of the dc link dynamics. Compared with the ac dynamics without dc link ($V_{dc}\mathbf{Y_{ac}}$), which is

$$\mathbf{G_{pL}} = -\frac{V_{dc}}{L(s^2+\omega_1^2)}\begin{bmatrix} s & \omega_1 \\ -\omega_1 & s \end{bmatrix} \tag{3}$$

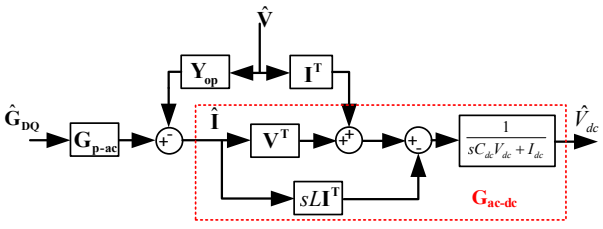


Fig. 4. Simplified small signal model of VSR with dc link.

the location of the complex-conjugate poles are related to the duty cycle and passive filters. Additionnally, the numerators are also changed which means the zeros are affected. Based on (2), $\hat{V}_{dc}$ is only related to $\hat{I}_d$, which agrees with the rule of active power balance [13]. Moreover, G_d has a right half plane zero (RHZ) which can describe the non-minimal-phase property of the dc link dynamics. This RHZ is introduced by the term $sL\mathbf{I}^{\mathbf{T}}$, which represents the variation of energy stored in the input L-filter. Although the average of the energy stored in the input L-filter in a fundamental cycle is zero, the input L-filter still has impact on the dc link dynamics.

To investigate the detail ac-dc interactions, Fig. 5 shows the frequency responses from the duty cycle $\hat{\mathbf{G}}_{\mathbf{DQ}}$ to the input current $\hat{\mathbf{I}}$ under different operation point. The active power is equal to 1 p.u. and the dc capacitor remain the same for all the operating point. It can be seen that the ac side dynamics is closed to the ideal case when the voltage is much higher than the current. With decreasing the ratio between the voltage and current, the frequency responses change a lot, where the resonance frequency move towards to higher frequency range and the magnitude responses of low frequency range are different. It proves that the ac-dc interactions play an important role in the low voltage with high current applications, where the inner control loop cannot be simplified to a L-filter plant. The dc link control plant shows the same trend based on the ac-dc interactions. With lower ratio between voltage and current, the frequency of the RHZ turn to be higher.

III. Impedance-based Stability Analysis of Dc Link Voltage Control

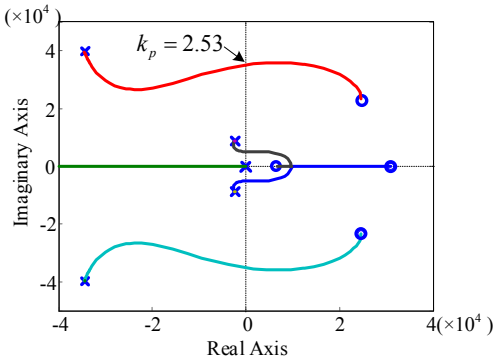


Fig. 6. Root loci of the VSRs.

To analyze the impact of the dc link voltage control on the input admittance, the inner loop is designed with 1 kHz BW with selecting the gain of the current controller as 18.8. The controller design follows the rule in [7]. The parameters for the following analysis are P=0.2 p.u., V_g=0.2 p.u., V_{dc} =0.75 p.u., L =0.267 p.u. C_{dc} =3.35 p.u..

A. Stability analysis of the VSR without grid variation

Base on the small signal model of VSR with considering the ac-dc interactions, Fig. 6 shows the root loci of the dc link voltage control with varying the proportional gain of the PI controller. It can be seen that proportional gain, k_p, of closed loop stable region is $k_p < 2.53$, which indicates the BW of dc link voltage control can be chosen to 160 Hz.

B. Impedance model of VSR

To calculate the input admittance of the VSR, the impact from the PCC voltage should be included. Fig. 7 shows the control block diagram of the cascade control loops in *dq* frame. $\mathbf{G_{del}}$ is the digital time delay effect, e.g. [14]

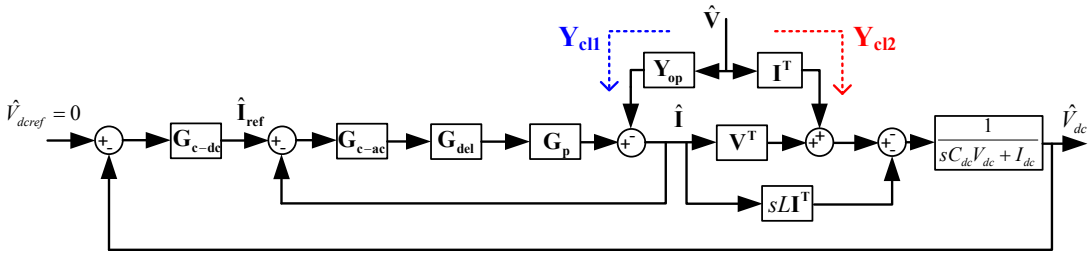


Fig. 7. Block diagram of the transfer function matrices of VSR with cascade control loops.

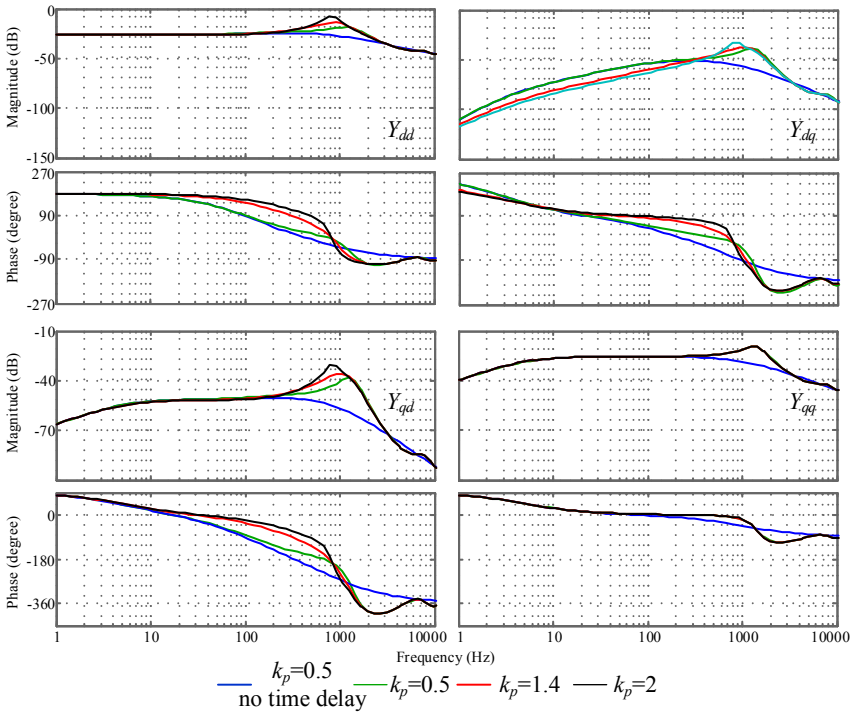


Fig. 8. Input admittance $\mathbf{Y_{cl}}$ of VSR in *dq* frame.

$$\mathbf{G_{del}} = \begin{bmatrix} G_{del} & 0 \\ 0 & G_{del} \end{bmatrix} = \begin{bmatrix} e^{-1.5T_s s} & 0 \\ 0 & e^{-1.5T_s s} \end{bmatrix} \quad (4)$$

The input admittance can be divided to two parts, one, $\mathbf{Y_{cl1}}$, is through the inner current control loop, the other, $\mathbf{Y_{cl2}}$, is through the outer dc link control loop. Unlike the methods in [7], the current reference of the inner loop is directly connected with the output of the outer loop control, which means the PCC voltage would not inject effects on the reference of inner loop. The total input admittance $\mathbf{Y_{cl}}$ of system in Fig. 7 is

$$\mathbf{Y_{cl}} = \mathbf{Y_{cl1}} + \mathbf{Y_{cl2}} = \begin{bmatrix} Y_{dd} & Y_{dq} \\ Y_{qd} & Y_{qq} \end{bmatrix} \quad (5)$$

To investigate the impedance shaping effects of the dc link voltage control, the VSR are analyzed with three sets of dc voltage controller in each. Both of them are in the stable region according to aforementioned closed loop stability analysis in Fig. 7. Table II provides the parameters of dc link voltage controller and current controller.

Table II Control parameters

Dc voltage controllers (k_p+k_i/s)	0.5+5/s, BW=30 Hz
	1.4+5/s, BW=85 Hz
	2+5/s, BW=120 Hz
Current controller	18.8+600/s, BW=1 kHz

Fig. 8 shows the bode plot of the input admittance $\mathbf{Y_{cl}}$, where three cases corresponding the three sets of the dc link voltage controller are compared. It can be observed that the negative impedance occurs merely in low frequency range in Y_{dd} without the digital time delay effects. When considering the digital time delay, high frequency range negative impedance appears. Moreover, with increasing the proportional gain k_p of the dc link voltage controller, the low frequency range of the negative impedance becomes wider, while the high frequency range moves to the left. The impedance model indicates that the low frequency range negative impedance is caused by the inherent dynamics within the VSR and its control loops, while the digital time delay effects lead to additional high frequency range negative impedance.

C. *Impedance-based stability analysis of VSR*

According to the generalized Nyquist stability criterion, the system stability can be predicted by the eigenvalues of the impedance ratio [15], which is derived as $\mathbf{T} = \mathbf{Z_{gdq}}\mathbf{Y_{cl}}$, where the $\mathbf{Z_{gdq}}$ is the grid impedance matrix in *dq* frame. The frequency response of the eigenvalues is plotted in this paper to explicate the stability of the system. The system is stable when both the gain margin (GM) and phase margin (PM) of all the eigenvalues are positive [16].

Fig. 9 shows the frequency responses for the eigenvalues with different BW of outer dc link controller. The GM and PM

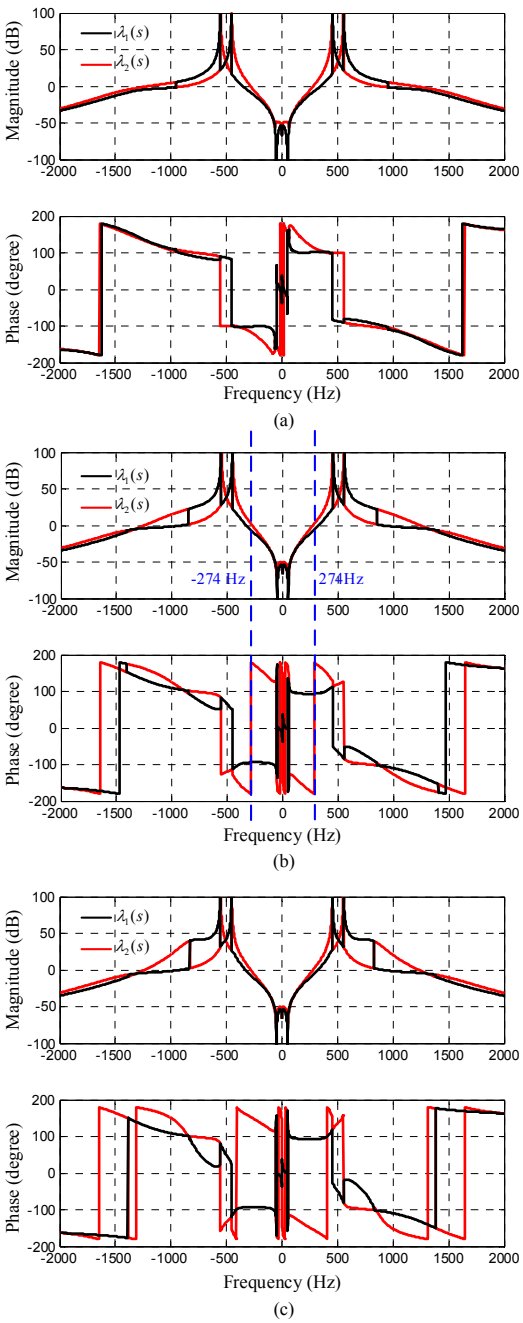


Fig. 9. Frequency response of the eigenvalues in the rectifier mode. (a). BW=30 Hz. (b). BW=85 Hz. (c). BW=120 Hz.

of both the eigenvalues are always positive, as shown in Fig. 9(a), which implies that the VSR system is stable. However, with increasing the BW of the dc link voltage control loop, the frequency responses vary. In Fig. 9(b), when increasing the BW to 85 Hz, one of the eigenvalues in black remains stable while the other in red shows instability. At the -274 Hz and 274 Hz, which is the phase crossover frequency, the GM is -0.4 dB. This indicates that the system is unstable but quite near the stable boundary, which implies that the system diverges slowly with resonances occurring nearby 274 Hz.

When the BW is increased to 120 Hz, as shown in Fig. 9(c), the system turns to be unstable because the GM of the eigenvalue in red is negative with -33 dB other than near 0 dB.

IV. Experimental Results

In order to verify the impedance and stability analysis, a test setup of the three phase VSR is built, where Chroma grid simulator is used for generating grid voltage, a danfoss frequency converter is used as the VSR and Cinergia electronic load is used as the dc link current source. The control system is implemented in the DS1007 dSPACE system. The electrical and inner current control parameters are the same used in impedance-based stability analysis

Fig. 10 shows the measured waveforms of PCC voltage(line to line, V_{AB}), phase A input current (I_A), and dc link voltage (V_{dc}) in the VSR. Three sets of dc control parameters, i.e. BW=30 Hz, 85 Hz and 120 Hz are tested. It can be seen in Fig. 10(a) that the system is stable when BW=30 Hz, which is consistent with the frequency domain analysis in Fig. 9(a). Compared with Fig. 9(b), harmonic oscillations occur in case of BW=85 Hz. To further confirm the stability prediction, the FFT results of I_A are given in Fig. 10(b), where two main harmonic components, i.e. 220 Hz and 320 Hz closely to the frequencies identified in Fig. 9(b) can be observed. In case of BW=120 Hz, the system is unstable with saturated. It is noted that all three control parameters is limited to the single VSR stability requirement, i.e. BW<160 Hz, and with increasing the BW of the dc control, the voltage and current are distorted. Thus, the experimental results verify the impedance shaping effects on the total input admittance from the dc link voltage control.

V. Conclusion

This paper presents the stability analysis of dc link voltage control in the VSRs based on the impedance method. The dc link dynamics would affect the inner ac current control plant in terms of the input voltage and load condition, which indicates the ac-dc interactions in the VSRs. Based on that, the input admittance of VSRs is calculated. The right half plane zero in dc link control would introduce negative impedance, which may result in oscillations in the low frequency range. Different BW of dc link voltage control are analyzed with impedance-based stability criterion, which are validated by the experimental results.

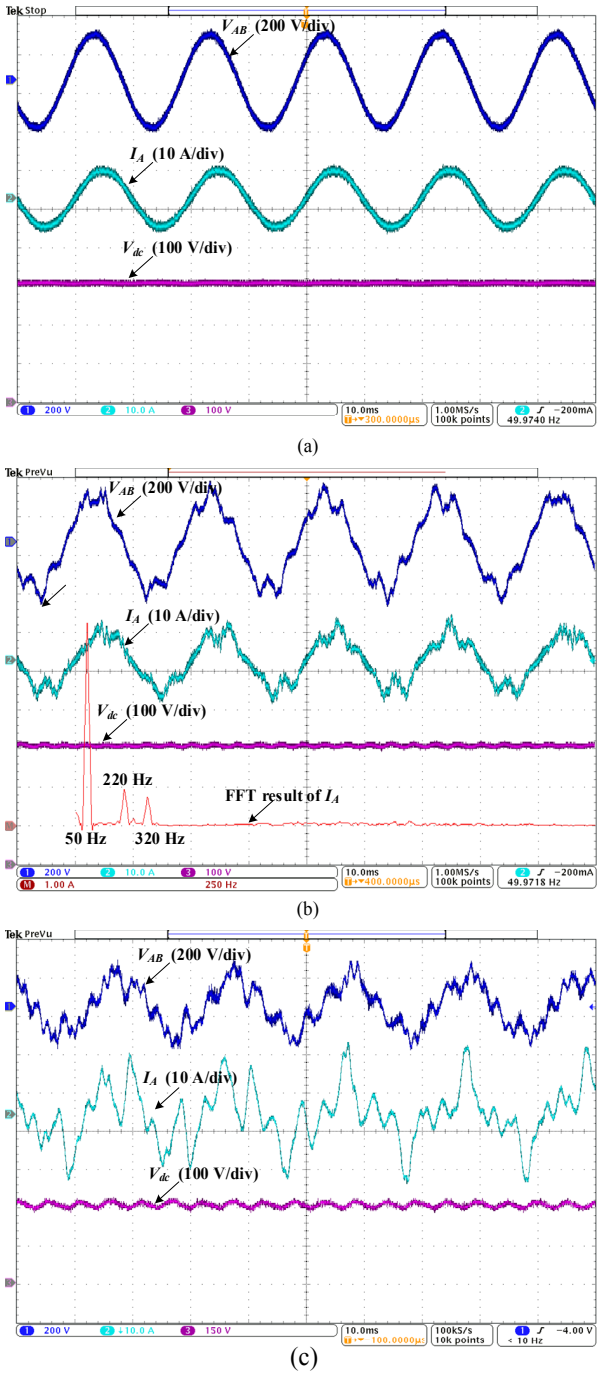


Fig. 10. Experimental waveforms for dc link control in VSRs. (a). BW=30 Hz (b). BW=85 Hz (c). BW=120 Hz.

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