Expanding the CCM Boundary of a Current-fed Switched Inverter

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***Abstract*—Current-Fed Switched Inverter (CFSI) is widely used due to its higher gain and inherent shoot-through protection. To account for the pulsating power output of the single phase CFSI, the passive storage elements (inductor and capacitor) of its boost stage contains a second harmonic component. As a result, the peak-to-peak ripple in the inductor current increases. This increased ripple forces the CFSI to have Discontinuous Conduction Mode (DCM) during light load condition. This distorts the AC output voltage of the CFSI. To avoid DCM, the peak-to-peak ripple in inductor current must be reduced. This paper presents a control based approach, in which second harmonic component of the inductor current is suppressed. This expands the boundary range of Continuous Conduction Mode (CCM) in a CFSI and improves its light load range. The proposed control scheme is validated for CFSI using a 500 W prototype, and it shows that the peak to peak ripple in the inductor current is reduced from 6.04 A to 2.76 A for a resistive load. This results the CCM boundary is extended by 54.3 % for a DC input of 35 V and AC output of 61 V (RMS).**

Keywords—Current-fed switched inverters, DCM, CCM, Second harmonic ripple, pulsating power.

I. INTRODUCTION

The boost-VSI (voltage source inverter) is a cascaded of a boost converter and a Voltage source inverter (VSI) and it is widely used to convert a DC input voltage to a higher AC output voltage. However, the major drawback of VSI is shoot-through which directly shorts the voltage stiff input, as the inverter is directly connected to DC-link of boost stage (Fig. 1). This drawback of converter is eliminated in Z-source inverter and its derivatives. They allow shoot-through of the inverter legs, which leads to better EMI noise immunity [1], [2]. The CFSI shown in Fig. 2, belongs to this class of converter [3], [4]. CFSI produces the similar characteristics as ZSI with lower passive components, and draws continuous input current. To further increase the gain of the converter, coupled inductor based CFSI is proposed in [5].

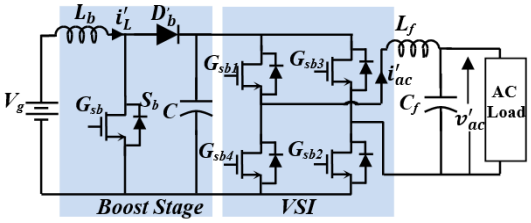

Fig. 1 Circuit diagram of Boost-VSI.

Referring to Fig. 1, in case of a Boost-VSI, the boost stage goes to DCM, when the diode D'_b stops conducting during turn off period of switch S_b [6], [7]. In this mode of operation, the DC-link capacitor supplies the current to the inverter and works as a normal VSI.

In case of CFSI, it works in CCM only when the instantaneous value of inductor current (i_L) is greater than the instantaneous value of inverter output current ($i_L > i_{ac}$) as shown in Fig. 3. During CCM, the current flows through the diode D_b, in the power interval, is the difference of i_L and i_{ac}. Due to this, the DC-link capacitor is connected at the input of the inverter (Ref to Fig. 2) and it behave as a normal VSI. However, CFSI exhibits DCM operation when current in D_a and D_b goes to zero. Diode D_b is first go to DCM, when i_L is equal or less than i_{ac} ($i_L \leq i_{ac}$). Therefore, DC-link capacitor floats and it is unable to supply the current to the inverter in the power state unlike boost-VSI. As a result, the voltage at the output terminal of the inverter differs from the DC-link capacitor voltage in the power state. Due to this disturbance, the AC output voltage gets distorted and leads to poor THD.

Due to pulsating power at the inverter output terminal, a double the line frequency ripple (*2f*-ripple) component appears in the inductor current (i_L) as shown in Fig. 3, [8]. The switching frequency ripple is also present in the inductor current. Due to these ripple components, peak-to-peak ripple in the inductor current increases and this leads to the condition of DCM in a CFSI.

The load at which DCM is invoked in a CFSI can be reduced in four ways: (a) By connecting a dummy load across the DC-link capacitor at the cost of reduced efficiency, (b) using an inductor with higher inductance value leads to reduce the switching frequency ripple and second harmonic ripple at the cost of degraded power density, (c) Increase the switching frequency of boost stage, reduces the switching frequency ripple only and, (d) control can be used to eliminate *2f* ripple in

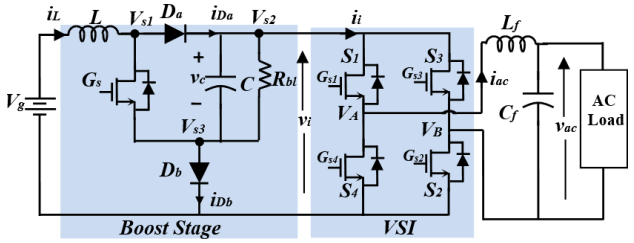

Fig. 2 Circuit diagram of Current Fed-Switched Inverter (CFSI).

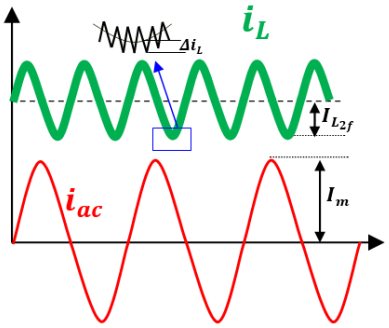

Fig. 3 Waveform of i_L and i_{ac} during CCM operation.

in the inductor current by suitably modifying the duty of converter [9]-[11].

In this paper, last method is opted to suppress the second harmonic current of the inductor. This reduces the peak-to-peak ripple of the inductor current and widens the CCM boundary of a CFSI. Thus, CFSI can operate relatively at lower load.

This paper is organized as follows: Firstly, operation of CFSI during CCM and DCM are discussed in section II. This section also derives the expression of critical load. Section III discusses the control technique to reduce peak-to-peak ripple in inductor current, which widen the CCM boundary range of a CFSI. In this section, controller is designed, which suppress the $2f$ ripple in inductor current. Designed controller is verified with the experimental and simulation results in section IV. Finally, section V concludes this paper.

II. Operation of CFSI in CCM and DCM

Similar to single phase H-bridge inverter, the unipolar PWM scheme of the CFSI includes zero and power state [3]. Shoot-through interval is inherently inserted in between the zero state to get the boost output voltage. The shoot-through interval is synchronized with the switch (S) of the boost stage. Shoot-through of inverter is equivalent to turning on either S_1 and S_4 together or S_3 and S_2 together.

During the shoot-through interval (DT_s), switch S of the boost stage is turned on with the synchronization of shoot-through (turning on S_1 and S_4) of inverter as shown in Fig. 4(a). Diode D_a and D_b is reversed biased by the capacitor voltage. The switching scheme is such that the inverter works in zero state in this duration [3]. During non-shoot through interval, inverter either works in zero interval (Fig. 4(b)) or power interval (Fig. 4(c)), which depends on the modulation index (m) of the inverter. In this interval, switch S is turned off, diodes D_a and D_b are forcibly turned on by the current. Therefore, DC-link voltage appears at the input of the inverter. Fig. 5 shows the waveform of switch node voltage and current during CCM operation.

If the inverter is in zero state during non-shoot through interval, all the inductor current flows through the diodes D_a and D_b as shown in Fig. 4(b). But in the power state of the inverter, part of the boost inductor current flows through the inverter and rest of the current flows through the capacitor and turned on the diode D_b as shown in Fig. 4(c). Therefore, boost capacitor charges through the difference of boost inductor current, and filter inductor current. The current from the diode D_a and D_b in the power state of the inverter are given as,

$$\left.\begin{aligned} i_{D_a} &= i_L(t) \\ i_{D_b} &= i_L(t) - i_{ac}(t) \end{aligned}\right\} \quad (1)$$

From the above equation, it is to be noted that the diode D_b stops conducting before the diode D_a. Fig. 6 shows the operation of CFSI, when it moves from CCM to DCM. The converter is operating in CCM mode initially, when the input inductor current is greater than inverter output current ($i_L > i_{ac}$) as shown in Fig. 4(c) and 6(b). At 0.5 sec, 60% of the load from the inverter is removed. It shows the instantaneous value of boost inductor current (i_L) is less than or equal to the inverter current ($i_L \leq i_{ac}$) for some duration as shown in Fig. 6(c). Therefore, in this duration, current through the diode D_b

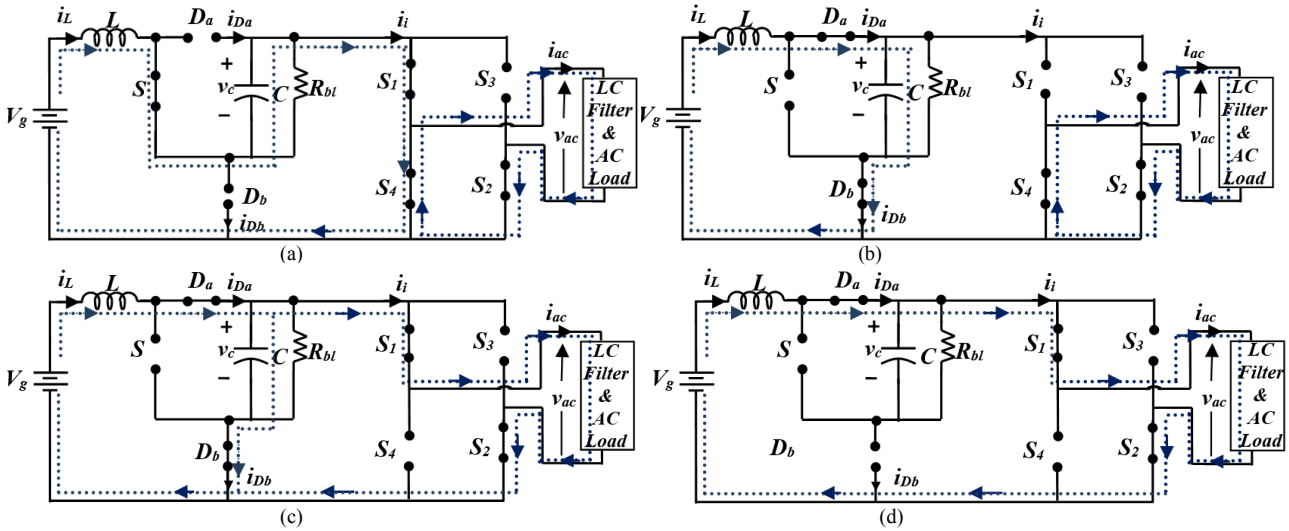

Fig. 4 Different modes of CFSI, (a) Shoot-through interval, (b) Zero state of inverter during non-shoot through interval, (c) Power state of the inverter during non-shoot through interval, and (d) Equivalent circuit of CFSI during DCM.

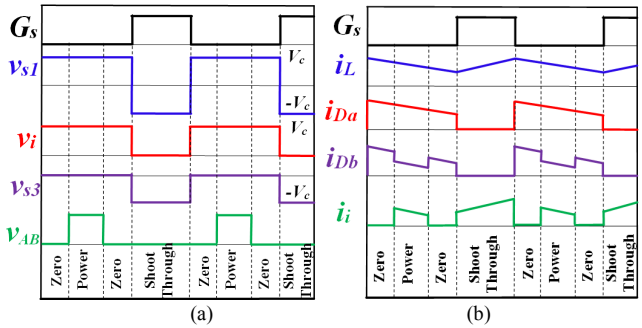

Fig. 5 Waveform of (a) Voltages and (b) Currents in a switching period during CCM operation.

becomes zero. Hence, as shown in Fig. 4(d), diode D_b is turned off. Thus, the inductor of boost-stage and filter inductor of the inverter are in series. Therefore, inductor current (i_L) is equal to the inverter current (i_{ac}) as shown in the shaded part of Fig. 6(c). In this mode, voltage at the inverter output terminal (V_{ab}) depends on the boost inductance and its current (i_L), which is relatively lesser than the DC-link voltage as shown in Fig. 6(c). This will distort the AC output voltage as shown in Fig. 6(a). From Fig. 3, the minimum current flowing through the diode D_b is given as,

$$\left(i_{D_b}\right)_{min} = \left(i_L(t)\right)_{min} - \left(i_{ac}(t)\right)_{max}$$

$$\left(i_{D_b}\right)_{min} = I_L - I_{L_{2f}} - \underbrace{\left(\frac{V_g + V_C}{2L} DT_s\right)}_{\Delta I_L} - I_m \qquad (2)$$

Here, D is the duty cycle (shoot-through period) of the boost stage. The average current of the boost inductor is relatively lesser for inductive load. Therefore, the condition of DCM is more severe in case of highly inductive load.

Let the fundamental voltage and current at the inverter output terminals are represented as, $v_{ac} = V_m \sin \omega t$ *and* $i_{ac} = I_m \sin(\omega t - \varphi)$, where V_m and I_m are the amplitudes of fundamental voltage and current, respectively, $\omega(=2\pi f)$ is the fundamental angular frequency and φ is the phase difference between v_{ac} and i_{ac}. It is assumed that LC (L_f-C_f) filter is filtering switching frequency component only. It doesn't affect component at frequency f. Hence, fundamental component of current in the filter inductor (L_f) is equal to the AC output current(i_{ac}).

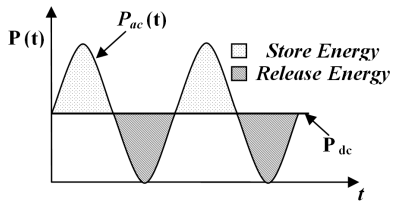

Fig. 7 Instantaneous power at the inverter output terminals.

Therefore, the power at the output terminal of the inverter is given as,

$$p_{ac}(t) = 0.5V_mI_m \cos\varphi - 0.5V_mI_m \cos(2\omega t - \varphi)$$

First term in above equation represents the real power or average power. And, second term represents the oscillating power. It oscillates above the average power at double the line frequency ($2f$) as shown in Fig. 7. This oscillating power is supplied by the passive storage components (L and C) of the boost stage. Passive storage components store energy in one half cycle and release in other. Due to this pulsating power, inductor current contains ripple at double the line frequency apart from switching frequency as shown in Fig. 3(a).

The converter is assumed to be lossless and operating in CCM mode. Therefore, the DC value of inductor current (I_L) is obtained by power balance. And, capacitor voltage is obtained by inductor volt-sec balance.

$$I_L = \frac{0.5V_mI_m \cos\varphi}{V_g} \quad and \quad V_c = \frac{V_g}{(1-2D)} \qquad (3)$$

Therefore, the minimum value of load (P_{min}) to operate CFSI in CCM is obtained by substituting the value of capacitor voltage, inductor current and magnitude of pulsating component ($I_{L_{2f}}$) in (2).

$$P_{min} = \left[I_{L_{2f}} + \frac{(1-D)DT_sV_m}{m \times L}\right] \times \left[\frac{(1-2D)V_m \cos\varphi}{0.5m\cos\varphi - (1-2D)}\right] \qquad (4)$$

Above equation shows that the minimum active power depends on the modulation index, second harmonic current of inductor and operating duty cycle. The magnitude of pulsating component ($I_{L_{2f}}$) can be calculated from the averaged AC model of the CFSI. After suppressing the second harmonic

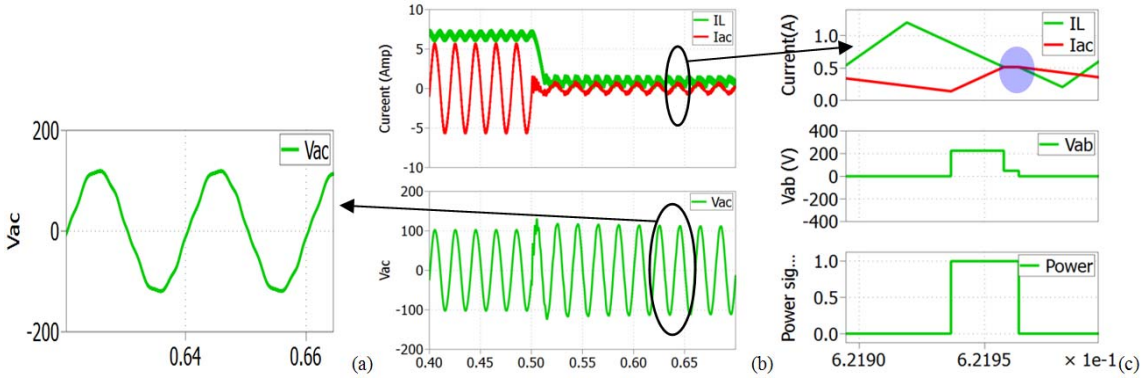

Fig. 6 Transition condition, when the converter moves from CCM to DCM. Horizontal axis represents time in Sec

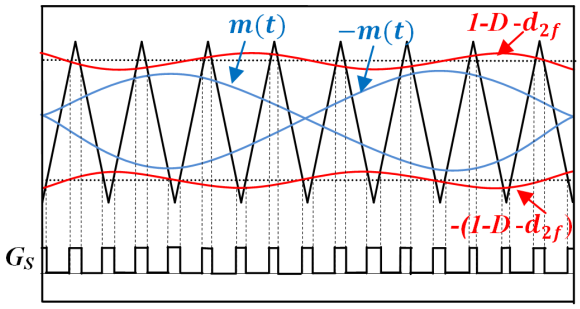

Fig. 8 Variation of shoot-through interval to suppress inductor *2f* component.

component ($I_{L_{2f}}$) to zero, the minimum value of diode D_b current is increased as seen from (2). Therefore, the minimum load requirement to keep the converter in CCM is improved as seen from (4). Next section discusses the control technique to suppress the Second Harmonic Component (SHC) of inductor current to zero.

III. Control Technique To Suppress Second Harmonic Component

The SHC of the inductor can be made zero by adding a small component (d_{2f}) of double the frequency in the duty cycle as shown in Fig. 8. It shows that the duty cycle is varying over a constant DC signal, which modulates the switching signal of the boost stage (and shoot through interval of inverter). Fig. 9 shows the closed loop block diagram to control the SHC of inductor current (shaded in blue) in CFSI. The DC and AC bus voltage are regulated by the DC voltage controller and AC voltage controller by controlling the duty cycle (D) and modulation index (m), respectively.

To suppress SHC, firstly inductor current is sensed by a current sensor and passed through the second order generalized integrator (SOGI) as shown in block diagram. SOGI is used to extract SHC of inductor current ($i_{L_{2f}}$). This SHC is compared with the reference signal and passed through the controller. Controller generates a double line frequency component (d_{2f}) according to reference signal. The reference signal is set to zero to suppress the SHC of the inductor current. The transfer function (TF) of SOGI tuned at double the line frequency ($2f$) is given below and plotted in Fig. 10. Bode plot of SOGI shows that it is tuned at 100 Hz so that it provides a

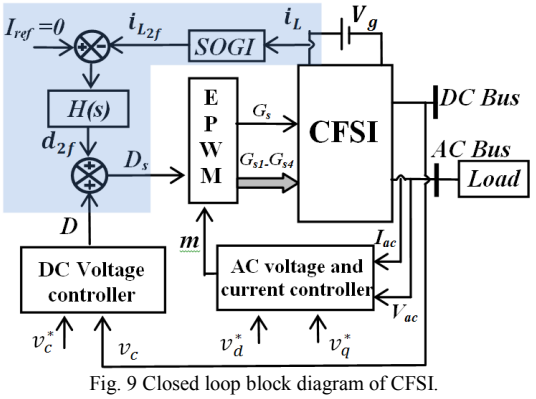

Fig. 9 Closed loop block diagram of CFSI.

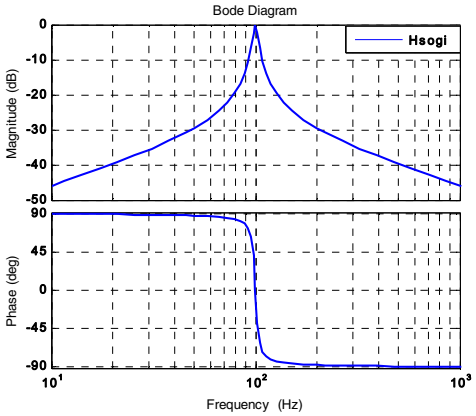

Fig. 10 Bode plot of Second order generalized integrator (SOGI).

gain of 0 dB and phase of 0 degree for 100 Hz component and, provides a significant attenuation to DC and other frequency components.

$$H_{SOGI}(s) = \frac{K_1 w_r s}{s^2 + K_1 w_r s + w_r^2}, w_r = 200\pi, K_1 = 0.05 \quad (5)$$

In order to obtain small component in duty cycle (d_{2f}), plant transfer function of CFSI is derived first. To do so, equivalent circuit of CFSI is derived. In the equivalent circuit, shoot-through of inverter is replaced by a switch and, current drawn by inverter is replace by a current source as shown in Fig. 11 (a). To do the analysis, some of the assumptions are carried out such as, (a) Semiconductor devices are ideal with zero on-state resistance and infinite off-state resistance, (b) Resistance and, forward voltage drop of diode during turn on is zero, (c) The turn-on and turn-off delays of semiconductor devices are assumed to be zero, (d) CFSI is working in CCM and (e) Bleeder resistance connected across DC-link is of infinite value.

In the PWM scheme of CFSI, S and S_T are turned ON simultaneously, as shown in Fig. 11(b). From this figure, capacitor voltage and inductor current can be written as,

$$v_L = L\frac{di_L(t)}{dt} = V_g - (r_l + r_c)i_L(t) + v_c(t)$$

$$i_c = C\frac{dv_c(t)}{dt} = -i_L(t)$$

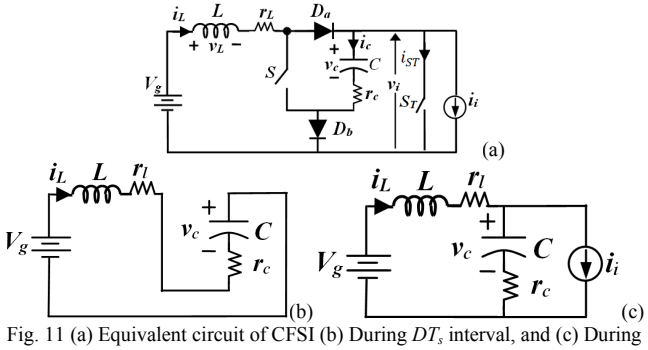

Fig. 11 (a) Equivalent circuit of CFSI (b) During DT_s interval, and (c) During $(1-D)T_s$ interval.

During *(1-D)T_S* interval, both the switches *S* and S_T are turned off simultaneously as shown in Fig. 11(c). From this figure, capacitor voltage and inductor current during *(1-D)T_S* interval can be written as,

$$v_L = L\frac{di_L(t)}{dt} = V_g - v_c(t) - (r_l + r_c)i_L(t) + r_c i_i(t)$$

$$i_c = C\frac{dv_c(t)}{dt} = i_L(t) - i_i(t)$$

Therefore, the average over one switching cycle is calculated using state-space average technique.

$$L\frac{d}{dt}\langle i_L(t)\rangle_{T_s} = V_g - \{1-2d(t)\}\langle v_c(t)\rangle_{T_s} - (r_l + r_c)\langle i_L(t)\rangle_{T_s} + r_c d'(t)\langle i_i(t)\rangle_{T_s}$$

$$C\frac{d}{dt}\langle v_c(t)\rangle_{T_s} = \{1-2d(t)\}\langle i_L(t)\rangle_{T_s} - \{1-d(t)\}\langle i_i(t)\rangle_{T_s}$$

Above average equations are perturbed to obtain the plant transfer function. $\hat{\imath}_L(t), \hat{\imath}_i(t), \hat{v}_c(t)$ and $\hat{d}(t)$are the small AC perturbation above the DC operating points I_L, I_i, V_c and *D*, respectively, which is given as,

$$\langle i_L(t)\rangle_{T_s} = I_L + \hat{\imath}_L(t),\ \langle i_i(t)\rangle_{T_s} = I_i + \hat{\imath}_i(t),$$

$$\langle v_c(t)\rangle_{T_s} = V_c + \hat{v}_c(t),\ \ d(t) = D + \hat{d}(t)$$

State space matrix is obtained after perturbation and linearizing the average circuit equations, which is given as,

$$\begin{bmatrix}\dot{\hat{\imath}}_L(t)\\ \dot{\hat{v}}_c(t)\end{bmatrix} = \begin{bmatrix}\frac{-(r_l+r_c)}{L} & \frac{-(1-2D)}{L}\\ \frac{(1-2D)}{C} & 0\end{bmatrix}\begin{bmatrix}\hat{\imath}_L(t)\\ \hat{v}_c(t)\end{bmatrix} + \begin{bmatrix}\frac{2V_c - I_i r_c}{L}\\ \frac{I_i - 2I_L}{C}\end{bmatrix}\hat{d}(t) + \begin{bmatrix}\frac{(1-D)r_c}{L}\\ \frac{-(1-D)}{C}\end{bmatrix}\hat{\imath}_i(t)$$

Above matrix is solved to obtain plant transfer function $G_{ip}(s)$, which is given as,

$$G_{ip}(s) = \left.\frac{\hat{\imath}_L(s)}{\hat{d}(s)}\right|_{\hat{\imath}_i(s)=0} = \frac{(2V_c - I_i r_c)Cs + I_i}{LCs^2 + (r_l + r_c)Cs + (1-2D)^2} \quad (6)$$

Plant *TF* has two poles and one right-half zero, which is plotted in Fig. 12. A controller, $(H(s))$ is to be designed based on the plant transfer function to obtain a desired phase and gain margin, which is given as,

$$H(s) = K\left(\frac{\frac{s}{w_z}+1}{s}\right), w_z = 162.22\,, K = 7.3$$

Loop gain and closed loop *TF* are also plotted in Fig. 12. At 100 Hz, gain and phase of Closed loop *TF* are 0 dB and 0 degree, respectively. It shows that the closed loop system is following the reference signal, which is set to zero in Fig. 9.

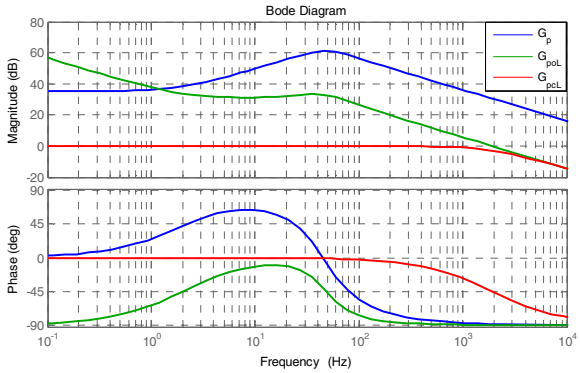

Fig. 12 Bode plot of plant transfer function, Loop gain and closed loop transfer function.

$$Loop\ gain\ TF:\ G_{poL}(s) = G_{ip}(s) \times H(s)$$

$$Closed\ loop\ TF: G_{pCL}(s) = \frac{G_{ip}(s)H(s)}{1 + G_{ip}(s)H(s)}$$

In the next section, controller is to be verified by the experiment and simulation results.

IV. Simulation And Experimental Results

CFSI converter is simulated in PLECES software to verify the above designed controller. The parameter used are V_g = 35 V, L/r_l =1.078 mH/ 470mΩ, *C*= 270 uF, R_{bl} (Bleeder resistor) = 15 kΩ, *m* = 0.56, *D* = .42. The inductive load of 250 W is connected at the power factor of 0.707. Fig. 13 shows the transition of CFSI from DCM to CCM by using above technique. Fig. 13 shows that, before point A, inductor current contains second harmonic component apart from DC and switching frequency component. The converter is operating in CCM mode ($i_L > i_{ac}$). At point A, compensation is applied. Therefore, the second harmonic component of inductor current is suppressed. After the compensation, inductor current contains only switching frequency component as shown in figure. At point B, 60% of the load is removed. It shows that in steady state the converter is still working in CCM mode because the second harmonic component is not present. Compensation is removed at point *C* to show that the circuit was in DCM if above technique was not used. It shows that the inductor current is less than or equal to the inverter current ($i_L \le i_{ac}$) and

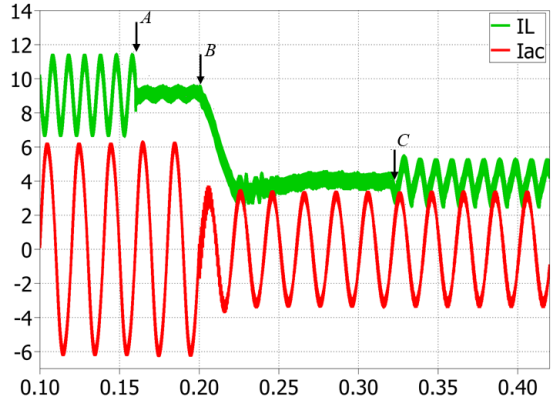

Fig. 13 Simulated waveform of inductor current during CCM and DCM condition. Horizontal axis represents time in sec.

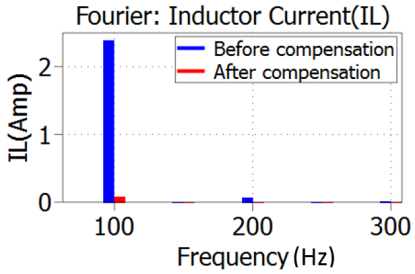

Fig. 14 Fourier spectrum of inductor current

converter goes to DCM. Fourier spectrum (Fig. 14) shows that the magnitude of second harmonic component in inductor current is suppressed from 2.2 A to 0.1 A.

A laboratory porotype of 500 W is developed to verify the above control technique. SiC Mosfet's (C2M0120160D) are used to operate the converter at a switching frequency of 75 kHz. Fig. 15(a) and 15(b) shows the experimental result before and after the compensation applied, respectively. Fig. 15(a) shows that the inductor current contains second harmonic component apart from switching frequency component. But after the compensation is activated, second harmonic component in inductor current is suppressed as shown in Fig. 15(b). Only the switching frequency component is present after

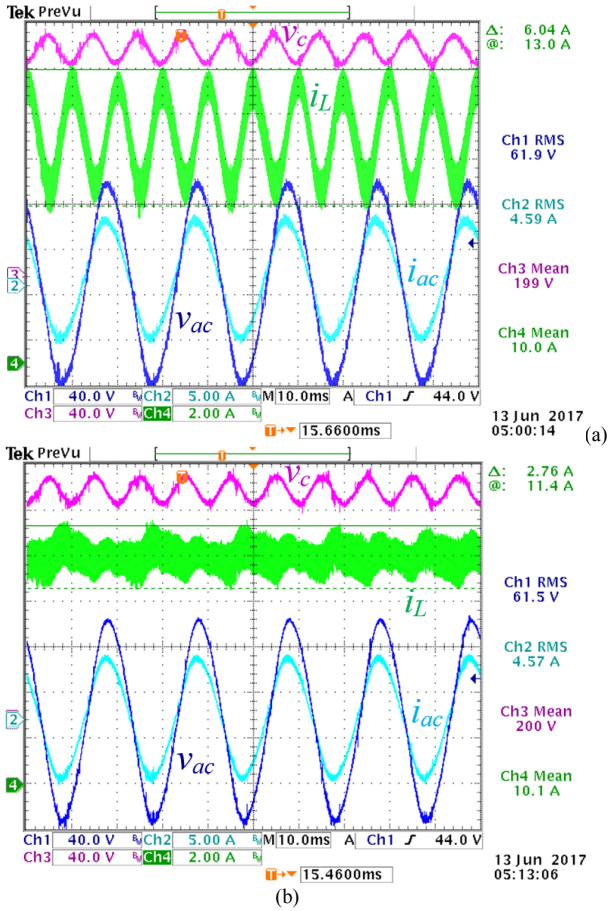

Fig. 15 Experimental waveform of CFSI (a) Before Compensation, and (b) After compensation.

the compensation. Waveform of inductor current shows that the peak to peak ripple is reduced from 6.04 A to 2.76 A. Using (4), value of P_{min} is calculated before and after compensation. It is found that the CCM boundary range of CFSI is increased by 54.3%.

V. Conclusion

The problem of DCM associated with CFSI during light load condition is discussed. The expression of minimum power is derived, which gives the lower (critical) boundary range to operate converter in CCM. The control technique is discussed, and controller is designed to suppress the second harmonic component in the inductor current. Simulation and experimental results verify the designed controller. Experimental results show that the peak-to-peak ripple is reduced from 6.04A to 2.76 A. This improve the CCM boundary range of CFSI by 54.3%.

Acknowledgment

This work was supported by the Department of Science and Technology, Government of India, under the Grant DST/RCUK/JVCCE/2015/04 (2) (G).

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