Analysis and Design of a Series Self-resonant Coil for Wireless Power Transfer

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***Abstract*—A planar coil structure that exhibits a series self-resonant behavior is developed for wireless power transfer systems which use magnetic resonant coupling. The proposed structure uses two thin, planar, spiral tracks separated by one layer of dielectric. By connecting to alternate ends of each track, the coil shows a series LC impedance, which is often necessary for voltage source inverters. An analytical model for the inductance, capacitance and resistance is used to develop a geometric design method that minimizes resistance given a set of application constraints. Experimental coils made with an FR4 PCB and an Teflon-ceramic PCB verify the proposed structure and modeling.**

I. Introduction

With the promise of cutting the last cord, wireless power transfer (WPT) using magnetic resonant coupling is gaining increasing popularity. Compared to the inductive WPT techniques used in commercial products today, resonant WPT can transfer power over a longer distance with higher spatial freedom. Experimental prototypes have shown power transfer across an air gap comparable to the radius of the transmission coil [1]–[3] with high efficiency, proving the viability of resonant WPT. Industrial consortia such as the AirFuel Alliance have specified standards that enable wide application in consumer electronics.

Despite the promises of high efficiency and long transfer distance, resonant WPT has significant challenges to overcome before broad adoption occurs. One of the critical challenges is the resonant coil design. Standard WPT coils use the coil inductance and a discrete, external capacitor to form the resonance. However, the resonant voltage applied to the capacitor may be very high and the high-frequency current may be problematic for lumped capacitors. Large arrays of film capacitors can reduce the voltage and current stresses of individual elements [4]. However, the array can be bulky and expensive, and may introduce undesirable interconnection impedance [5].

Another approach to building the resonance is using the intrinsic electric field of the coil to resonate with the magnetic field, forming a self-resonance. Depending on whether there is standing wave along the transmission line, the self-resonant coils are separated into two classes. The first class relies on the standing wave to form the resonance [2], [6]. In [2], the reported system uses two identical coils with 25 cm radius and can transfer 60 W over 2 m distance with 40 % efficiency.

However, at 20 cm away from the surface of the device coil, the calculated RMS magnitude of the electric field is E_{rms} = 1.4 kV/m and radiated power is 5 W [2]. Both the electric field and the radiated power are problematic for nearby components and humans.

In the second class, the length of the coil is much smaller than the wavelength, and thus has negligible standing wave along the coil. Instead, coils incorporate the parasitic capacitance between adjacent turns or parallel structures to resonate with the self-inductance [5], [7]–[13]. These coils can be modeled using simple LCR equivalent circuits.

Comprehensive research into coil parasitics is reported in the literature for various coil structures. The parasitics between adjacent turns for solid copper wire [7], Litz wire [8], copper tube [9], and planar PCB coil [10] have been widely studied. Based on the parasitic modeling, the self-resonant frequencies can be calculated or, equivalently, the geometry of the coils can be designed to achieve a target resonant frequency.

However, one key feature of the coils using the electric field between adjacent turns as the resonant field is that the electric field is exposed in the open air. Therefore, the stray capacitance is sensitive to nearby objects. More importantly, the exposed resonant electric field has the potential to interfere with, or damage, nearby electronic components.

Instead of using the stray capacitance between turns, reference [5], [11], [12] propose structures that confine the resonant electric field between two conductor layers inside a dielectric material, similar to a lumped capacitor. The stray capacitance is stable and the resonant electric field is safe for nearby components. Reference [11] is a helical coil built from a coaxial cable. By adding an auxiliary layer on the isolation layer and adjusting the length of the auxiliary layer, the stray capacitance is formed and tuned. Reference [12] is a double side PCB coil. The electric field is confined between the top and the bottom conductor layer. Reference [5] uses a C-shaped parallel plate capacitor.

The majority of self-resonant WPT coils described in literature to date exhibit a parallel resonance. Without additional filtering elements, parallel resonant coils are not suitable for use with voltage-source inverters in WPT systems. In [13], a self-resonant coil is reported with series LC impedance using a bifilar coil. However, the structure uses the capacitance between adjacent turns, resulting in exposed resonant electric field. Moreover, the design method of the inductance,

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capacitance, and ESR is missing in the literature.

This paper proposes a self-resonant coil with series LC impedance and contained electric field. The structure, working principle and complete LCR design method are presented in Section II. A geometrical design optimization that achieves specified inductance and capacitance while minimizing resistance is detailed in Section III. Analysis is verified with simulation and experimental measurements of prototype coils in Section IV. The conclusions are stated in Section V.

II. Self-Resonant Coil Structure and Analysis

A. Proposed Structure and Operation Principle

Fig. 1 shows an exploded view of the proposed coil structure. The coil consists of two identical planar spiral coils separated by one layer of dielectric material. The two copper spirals are designed to achieve the resonant inductance and inserted dielectric material helps form a parallel-plate capacitor between the two copper layers while fixing their position. When implemented, there is no air gap between the three layers. Terminals one and four are connected to the ac source (e.g., WPT inverter) while terminals two and four are left open.

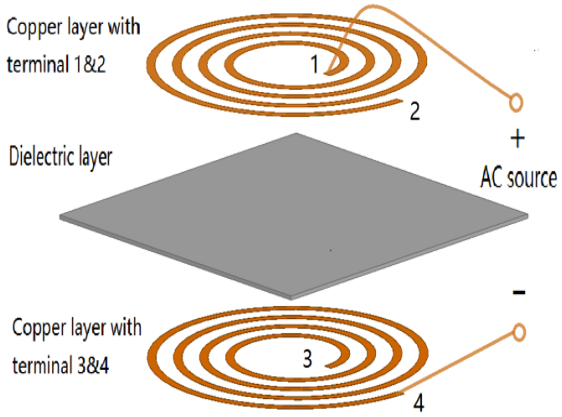


Fig. 1. Exploded view showing the structure of the proposed coil.

Due to complete separation of the two conduction layers by the dielectric, the coil is an open circuit for a DC source. When an AC source is applied, current flows from one terminal to the other crossing through the dielectric in a distributed gradient throughout the length of the coil. Though current is distributed over the length of the coil, every current path between the terminals traverses the entirety of the spiral once, and crosses the dielectric once, resulting in a series LC impedance.

The geometric parameters of the spiral track are shown in Fig. 2. w is the width of each turn, s is the distance from the inner radius of one turn to the inner radius of the adjacent turn, d_i is the inner radius, and d_o is the outer radius. Additionally, n is the number of turns in the spiral and h is the thickness of the dielectric layer.

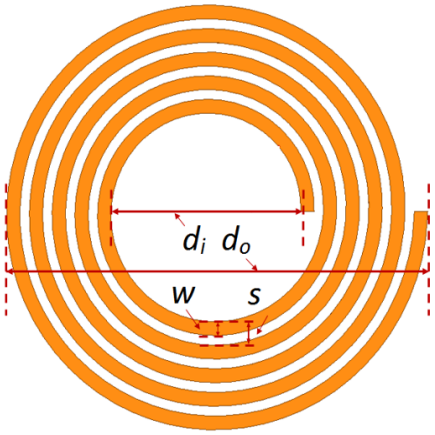


Fig. 2. Geometric parameters and shape of the proposed coil.

B. Analysis and Modeling

In order to examine the performance capabilities analytical models are developed based on results from the literature for the inductance, capacitance, and resistance in the following subsections.

1) Inductance: Compared to a single spiral coil, the current flow in the proposed self-resonant coil differs only in that it crosses vertically through the dielectric layer (i.e. in the plane of the page in Fig. 2). When the dielectric thickness is thin relative to the coil diameter, the current path in the proposed self-resonant coil and a simple planar spiral inductor are nearly the same. Therefore the two coils have the same inductance. As analyzed in [14], the inductance of a planar spiral coil is

$$L_s = \frac{\mu n^2 d_{avg}}{2}\left(\ln\frac{2.46}{k_u} + 0.2{k_u}^2\right) \tag{1}$$

where μ is the magnetic permeability, d_{avg} is the average diameter $d_{avg} = (d_o + d_i)/2$, $k_u = (d_o - d_i)/(d_o + d_i)$. Therefore the inductance equation is re-written as

$$L_s = \frac{\mu n^2 (d_i + d_o)}{4}\left(\ln\frac{2.46(d_i + d_o)}{d_o - di} + 0.2\left(\frac{d_o - d_i}{d_o + d_i}\right)^2\right) \tag{2}$$

From [14], this expression exhibits a typical error of 3% when compared to FEM analysis.

2) Capacitance: The electric field of the proposed structure is composed of two parts: the primary electric field located vertically between the two conductor layers and inside the dielectric, and the fringing field located between adjacent conductors. Fig. 3, reproduced from [10], shows the electric field of the double layer planar coil for an example case of conductor pitch.

The electric field with fringing effect has been widely researched in the literature [10], [15]. The work in [15] summarized various calculation formulae and verified them with simulation results, proposing an accurate model of the capacitance

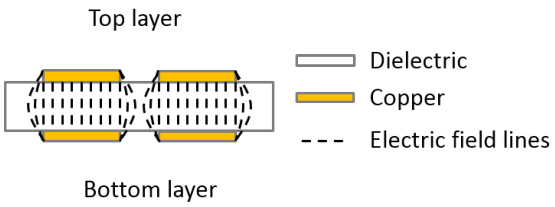


Fig. 3. Schematic showing the electric field of a double-layer PCB coil [10].

$$C_s = \frac{\varepsilon\varepsilon_0 l_0}{h}\left[w + \frac{h}{\pi}\ln\frac{2h}{\pi w} + \frac{h}{\pi}\ln\left(1 + \frac{2h}{\pi w} + 2\sqrt{\frac{t}{h} + \left(\frac{t}{h}\right)^2}\right)\right] \tag{3}$$

where ε is the dielectric constant, ε_0 is the permittivity of vacuum, h is the dielectric thickness, $l_0 = \pi n(d_o + d_i)/2$ is the total length of one spiral copper foil, and t is the thickness of the foil. Based on the design parameters, (4) is written as:

$$C_s = \frac{\varepsilon\varepsilon_0\pi w n(d_i + d_o)}{2h}\left[1 + \frac{h}{\pi w}\ln\frac{2h}{\pi w} + \frac{h}{\pi w}\ln\left(1 + \frac{2h}{\pi w} + 2\sqrt{\frac{t}{h} + \left(\frac{t}{h}\right)^2}\right)\right] \tag{4}$$

3) Resistance: The total loss of the proposed self-resonant coil consists of copper loss and dielectric loss. The copper loss is modeled as low-frequency loss due to DC resistance and additional high-frequency loss due to eddy currents in the conductors [5]. For a simple single layer spiral coil, the low frequency resistance is

$$R_{s,lf} = \frac{\rho_{copper}\int \vec{E}\cdot d\vec{l}}{\vec{E}\cdot d\vec{S}} = \frac{\rho_{copper}\pi n(d_i + w + n\cdot s)}{w\cdot t} \tag{5}$$

The loss when the simple spiral coil conducts I_0 current is

$$P_s = \frac{I_0^2\rho_{copper}\pi n(d_i + w + n\cdot s)}{w\cdot t} \tag{6}$$

The current in the series self-resonant coil is different from in a simple single layer inductor. At the terminals, the entire coil current flows through one of the spiral conductors, with zero in the opposite conductor. Assuming the capacitance is perfectly uniform across the length of the conductor, the current linearly transitions from the top to bottom spiral over the length of the coil. With I_0 as the total input current, the current at any position in the coil a distance l away from terminal 1 is

$$I_{1,l} = \frac{l}{l_0}I_0 \tag{7}$$

The total current of both sides add up to I_0. Therefore, the current on the other side at the same position is

$$I_{2,l} = \frac{l_0 - l}{l_0}I_0 \tag{8}$$

The power loss on the proposed self-resonant coil when conducting I_0 is

$$P_r = \int_0^{l_0}(I_{1,l}^2 + I_{2,l}^2)\frac{\rho_{copper}}{w\cdot t_c}\cdot dl \tag{9}$$

where t_c is the thickness of the copper layer. After simplification, it is found with same current the loss on the resonant coil is 2/3 of a simple spiral coil. Therefore

$$R_{r,lf} = \frac{2}{3}R_{s,lf} \tag{10}$$

In addition to dc resistance, the time-varying magnetic field causes the eddy current loss in the copper foil. Since the magnetic field in the self-resonant coil and the single planar inductor are the same, the self-resonant coil has twice the eddy current loss of a single planar coil because it has two layers of conductor exposed to the magnetic field. The eddy current loss in a single spiral planar inductor $R_{ac,s}$ has been studied in [16] and is given by

$$R_{s,e} = \frac{\rho_{copper}l_0}{w\delta(1 - e^{-\frac{t}{\delta}})} - R_{s,lf} \tag{11}$$

The total copper ESR of the self-resonant coil is

$$R_{r,copper} = 2R_{s,e} + \frac{2}{3}R_{s,lf} \tag{12}$$

$$R_{r,copper} = \frac{\rho_{copper}l_0}{w}\left(\frac{2}{\delta(1 - e^{-\frac{t}{\delta}})} - \frac{4}{3t}\right) \tag{13}$$

where δ is the skin depth at working frequency f

$$\delta = \sqrt{\frac{\rho_{copper}}{\pi\mu f}} \tag{14}$$

The dielectric loss is calculated based on the loss tangent D_k of the dielectric material

$$R_c = \frac{D_k}{2\pi f C_s} \tag{15}$$

Finally, the total equivalent series resistance (ESR) of the coil is

$$R_s = \frac{\rho_{copper}l_0}{w}\left(\frac{2}{\delta(1 - e^{-\frac{t}{\delta}})} - \frac{4}{3t}\right) + \frac{D_k}{2\pi f C_s} \tag{16}$$

III. Coil Design for Minimum Resistance

Using the equations for inductance, capacitance and ESR in (2), (4), and (16), respectively, it is of interest to examine optimization of the coil geometry to achieve a designed L_s and C_s while minimizing R_s for a given application.

A. Design Process

The dielectric constant D_k, the copper thickness t_c and the dielectric thickness h are fixed for a given laminate material. Because D_k is fixed, and assuming the design achieves the target capacitance $C_s = C_0$, the dielectric loss in (15) is constant, and thus the optimization goal is solely to minimize $R_{r,copper}$. The maximum outer diameter d_o is usually fixed due to the constrained device size in-application. Therefore, the coil design is determined by d_i, n and w. For desired inductance L_0 and capacitance C_0, the optimization problem is

$$\min R_{r,copper}(d_i, n, w) \quad s.t. \begin{cases} L_s(d_i, n, w) = L_0 \\ C_s(d_i, n, w) = C_0 \end{cases} \tag{17}$$

The three design parameters d_i, n and w are constrained by the two equations of L_0 and C_0 shown in (17). Another requirement is that the n needs to be an integer. The most straightforward way of finding the optimal geometry design with lowest ESR is through iterative calculation of all possible integer values of n and selection of the lowest ESR design. To bound this iteration, the feasible range of n is examined. From (2) the number of turns n is:

$$n = 2\sqrt{\frac{L_0}{\mu\left(d_i + d_o\right)\left(\ln\frac{2.46(d_i+d_o)}{d_o-d_i} + 0.2\left(\frac{d_o-d_i}{d_o+d_i}\right)^2\right)}} \tag{18}$$

Note that, in (18), only d_i is a design parameter, as d_o and L_0 are fixed by application requirements. As such, this equation is rewritten using a spiral fill factor $\alpha = d_i/d_o$, where $0 < \alpha < 1$, and normalized number of turns $n_0 = n/\sqrt{\frac{L_0}{d_0}}$

$$n_0 = \frac{2}{\sqrt{\mu\left(\alpha+1\right)\left(\ln\frac{2.46(1+\alpha)}{1-\alpha} + 0.2\left(\frac{1-\alpha}{1+\alpha}\right)^2\right)}} \tag{19}$$

The relation between n_0 and α is shown in Fig. 4.

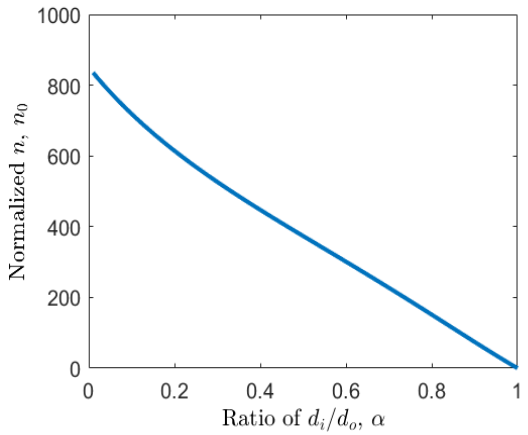


Fig. 4. Relation of n_0 with α, with α ranging from 0 to 1.

Fig. 4 shows n_0 decreases monotonically as α increases. For any target L_0, the maximum n occurs when the inner diameter $d_i \approx 0$ or, equivalently, $\alpha = 0$. Under this condition (19) simplifies to

$$n_{max} = 2\sqrt{\frac{L_0}{\mu d_o\left(\ln 2.46 + 0.2\right)}} \tag{20}$$

The minimum n approaches zero when $d_i \approx d_o$. Therefore, the practical minimum number of turns, as constrained by L_0, is one. However, n is also constrained by the required capacitance C_0. As the inner diameter increases, the remaining copper area decreases until even completely filling the winding area with copper does not result in sufficient plate area to produce C_0.

$$d_{i,max} \approx \sqrt{\left(d_o^2 - \frac{4hC_0}{\varepsilon\varepsilon_0\pi}\right)} \tag{21}$$

which neglects fringing capacitance to simplify the expression. The largest inner diameter $d_{i,max}$ directly determines the minimum n_{min}, as shown in Fig. 4. Accordingly, the minimum n_{min} is calculated combining (21) and (18), with $k_{u,min} = (d_o - d_{i,max})/(d_o + d_{i,max})$

$$n_{min} = 2\sqrt{\frac{L_0}{\mu\left(d_{i,max} + d_o\right)\left(\ln\frac{2.46}{k_{u,min}} + 0.2k_{u,min}^2\right)}} \tag{22}$$

Once the range of n is known, w and d_i are solved by combining the inductance and capacitance equations (2) (4) and the ESR is calculated using equation (16) for each feasible integer value $n_{min} < n < n_{max}$. The iteration process is shown in Fig. 5.

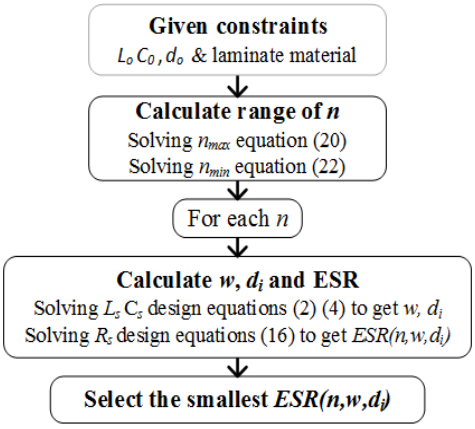


Fig. 5. Optimal design process.

From intuition, the minimal n will result in the shortest conductor length. Assuming the fringing capacitance is small compared with the primary capacitance, a shorter conductor length requires a larger conductor width to achieve an equivalent conductor area and thus to maintain C_0. In this case, the design with the minimum number of turns n_{min} will have

the minimum copper loss as both shorter and wider trace reduces $R_{r,copper}$ according to (13). However, in some extreme situations, e.g. when h is much larger than w and the required C_0 is small, the fringing field dominates the capacitance and n_{min} may not minimize $R_{r,copper}$. To maintain generality, an iterative approach which considers all n within the feasible range $n_{min} < n < n_{max}$ is used for all design cases.

B. An Example of the Geometric Optimization Design

An example set of 6.78 MHz WPT coil design constraints is listed in Table I. The geometric parameters to be optimized are the number of turns n, the width of trace w and the inner diameter d_i. Using the design method in Fig. 5, the results are shown in Fig. 6.

TABLE I
EXAMPLE COIL DESIGN CONSTRAINTS

Parameters	Value
L_0	3.12 μH
C_0	176.5 pF
d_0	10 cm
ε	3
h	0.508 mm
t_c	1 oz
D_k	0.0001

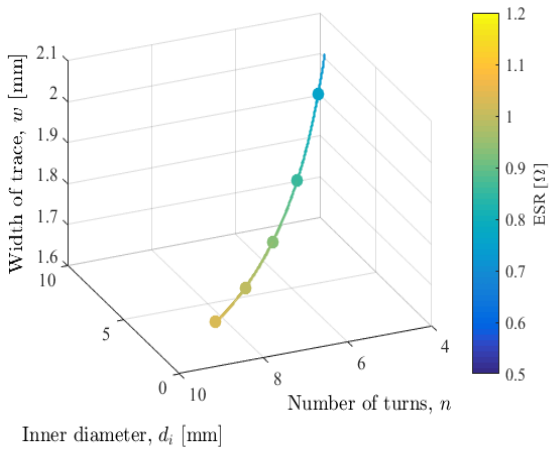


Fig. 6. ESR with different n, w, d_i, the the dot on the curve is the iterated point with integer n.

The inner diameter d_i with respect to n is shown in Fig. 7. The monotonic increasing of d_i with the decreasing of n is as expected. The calculated n_{max} and n_{min} are 9.5 and 4.4, respectively. Because both n_{max} and n_{min} are boundary limits, only coils with integer values of n in the range $5 \leq n \leq 9$ can achieve the design constraints on L_0 and C_0 simultaneously.

The calculated results show the ESR of the optimized geometry is 0.75 Ω with $n = 5$. In contrast, the ESR of the worst geometry is 1.03 Ω with $n = 9$. The ESR is

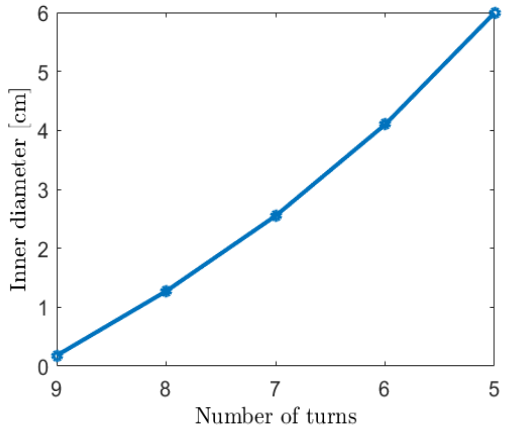


Fig. 7. Inner diameter with different n.

reduced by 27 % compared with the worst design which still meets the target inductance and capacitance. Fig. 8 shows the length and width of the trace as n is varied. In this design case the minimal n results in shortest conductor length and widest conductor width, minimizing $R_{r,copper}$, and therefore producing the optimal design. A comparison of the optimal design with n = 5 with a non-optimal design with n = 8 is shown in Fig. 9.

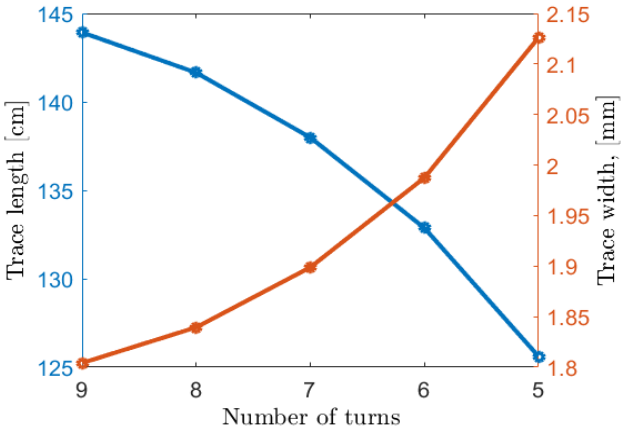
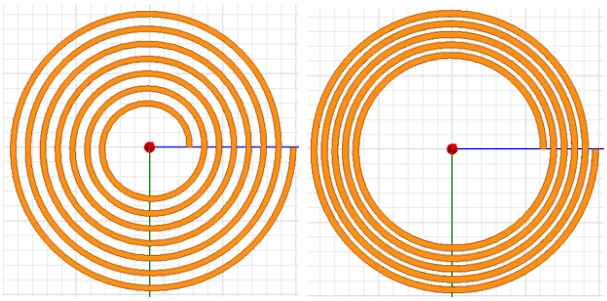


Fig. 8. Length and width of trace with different n design for same inductance and capacitance.

IV. PROTOTYPE TESTING AND VERIFICATION

A. Electric Field Simulation

For the proposed self-resonant coil, the energy of the resonant electric field is located inside the dielectric instead of exposed to nearby components or human. Ansys HFSS simulation is used to verify the field location. The simulated coil has five turns and operates at the resonant frequency. Fig. 10 shows a cross-section view where the red region is the resonant electric field. It is confined inside the dielectric



(a) (b)

Fig. 9. Images of the non-optimal coil with n = 8 (a) and optimal coil with n = 5 (b)

layer. As the coil is approximately central-symmetric, the field distribution for other cross-sections is similar.

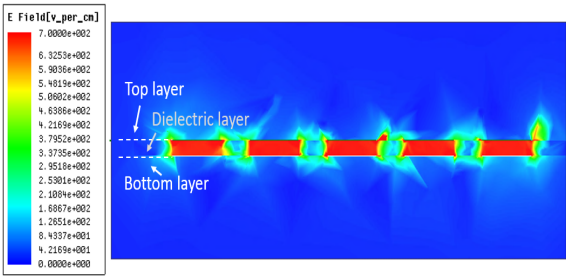


Fig. 10. Cross-section view of the E-field distribution of the proposed coil.

B. Experimental Coil Tests

A set of coils with different shapes are built to verify the proposed coil and design equations. Coils use a standard FR4 PCB as both the substrate and dielectric material. Six different geometries and their parameters are listed in Table II. Fig. 11 shows the picture of the experimental coils. The coil uses the two inner layers of the PCB resulting in a dielectric thickness of 0.71 mm. The coil uses one inner layer and the adjacent outer layer resulting in a thickness of 0.33 mm.

TABLE II
GEOMETRIC PARAMETERS OF THE FABRICATED SELF-RESONANT COILS WITH FR4

Coil	Dielectric thickness h (mm)	Inner diameter d_i (mm)	Outer diameter d_o (mm)	Number of turns n	Trace width w (mm)
1	0.33	20	140	3	9.9
2	0.33	21.2	100	4	6.6
3	0.71	34.2	100	5	4.5
4	0.33	20	74	7	1.6
5	0.33	20	74	6	2.8
6	0.71	31	74	7	2.2

The coils are tested using an Agilent 4294A impedance analyzer and 42941A impedance probe kit. One example measurement curve is shown in Fig. 12. As shown, the

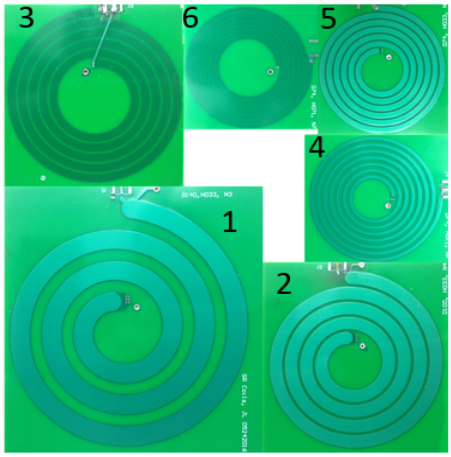


Fig. 11. Picture showing the fabricated FR4 coils.

coil is capacitive below 6.457 MHz, and inductive above 6.457 MHz. At 6.457 MHz the impedance is minimized, and the phase is nearly zero, which means the coil exhibits a series LC resonance. The series LC impedance is also verified by connecting the coil to a voltage source inverter (VSI) working at 6.78 MHz. Fig. 13 shows the input voltage and current of the coil.

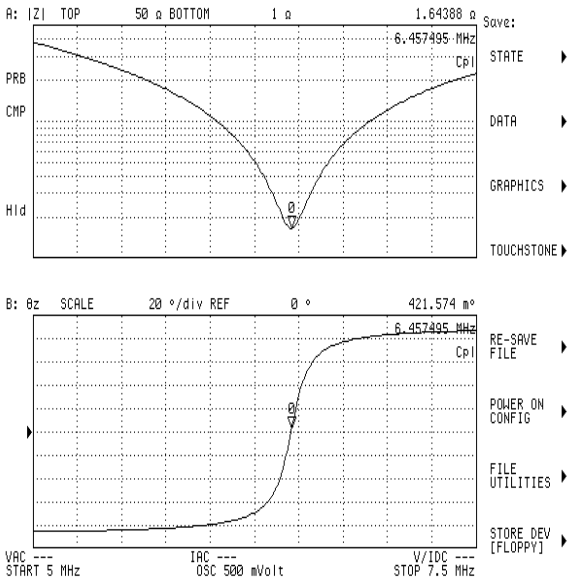


Fig. 12. The impedance and phase curve of one fabricated coil.

The measured LCR parameters of each coil are compared with calculation values, which are shown in Fig. 14. The calculated values match with the measurements, proving the accuracy of the design equations. However, the quality factors of those coils are low (around 40). The high dielectric loss of the FR4, $D_{k,FR4}$ = 0.02, limits the achievable ESR of the

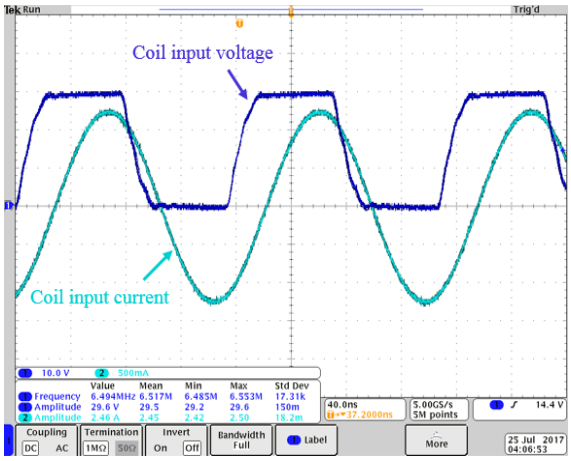


Fig. 13. Input voltage and current of the fabricated coil when connected with a VSI working in a WPT system.

coils.

To improve quality factor, a RO3003 Teflon-ceramic laminate is used for an additional prototype. The loss tangent of RO3003 is 0.001 at 10 GHz [17].

However, there is no data on the loss tangent at 6.78 MHz. In the calculation, the loss tangent is approximated to be zero as the minimal loss tangent produces a negligible increase in ESR compared to the copper loss. The calculated values of the RO3003 coil are L = 3.12 µH, C = 176.5 pF, ESR = 0.75 Ω, and Q = 177. The tested values are L = 3.13 µH, C = 173.8 pF, ESR = 0.72 Ω and Q = 185, showing good accuracy. Fig. 15 shows the picture of the RO3003 coil.

V. Conclusion

By separating two planar spiral foil inductors with a dielectric layer, and connecting in a manner such that the current has to flow through the dielectric, the proposed coil exhibits a series LC impedance. The series working principle is verified by impedance measurements and by testing with a voltage source inverter in a WPT system. Complete LCR modeling and design methods are proposed and verified by experimental measurements of prototype coils. Based on the design equations, a geometrical optimization that achieves specified inductance and capacitance while minimizing resistance is detailed.

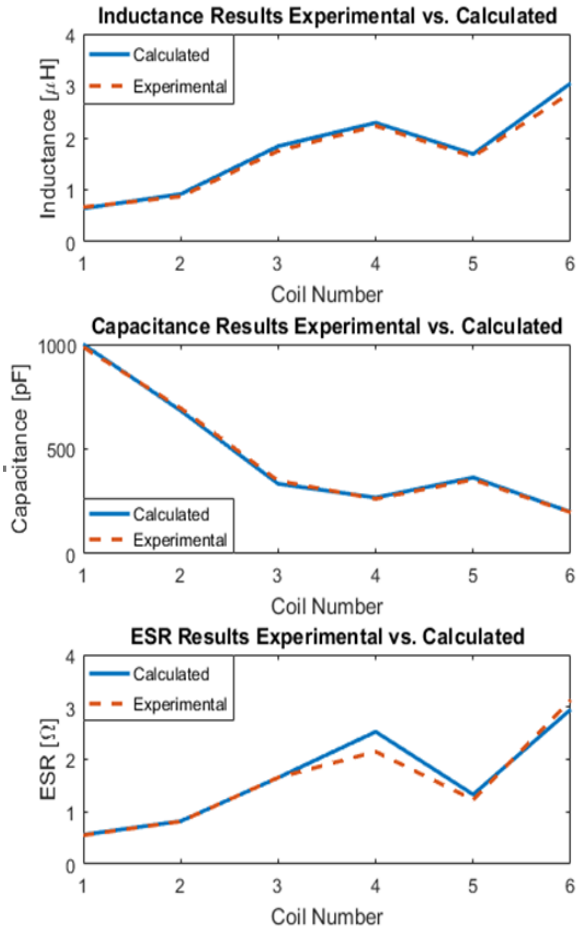


Fig. 14. LCR parameters comparison of the tested results and the calculated results.

Fig. 15. Self-resonant coil built with RO3003 for further reduced loss.

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