High Current Switching Capacitor Converter for On-Package VR

Stefano Saggini†,Shuai Jiang*, Mario Ursino†, Chenhao Nan*, Roberto Rizzolatti†

*Google Inc.
1220 N. Mathilda Ave, Sunnyvale, CA 94089

†DPIA - University of Udine
Via delle Scienze 208, 33100 Udine, Italy

Email: shuaij@google.com, stefano.saggini@uniud.it, ursino.mario@spes.uniud.it, rizzolatti.roberto@spes.uniud.it, chenhaon@google.com

***Abstract*—Digital ASIC devices are widely used in networking and computing applications. This kind of devices are implemented with a short channel technology requiring high peak currents for high complexity systems and a low supply voltage. Digital ASICs are powered by an external Voltage Regulator with specifications similar to modern microprocessors' power supply (VRMs). In order to reduce the number of power pins and to reduce the Power Distribution Network (PDN) issue, Intel's® 4th generation CoreTM [1] integrates Voltage Regulators, moreover many on-package conversion systems [2], [5] are present in literature. In this paper a conversion solution based on switched resonant tank is presented, yielding currents up to 300 A, on 0.8 V in an area of 10 cm^2 with a resonant-driving technique.**

I. Introduction

TODAY DIGITAL ASICS, implemented in short channel technology, require low voltage and high current power supply with a critical PDN design and a huge number of supply voltage pins. Modern Intel processors integrate voltage regulators in order to overcome these limitations, improving also the system efficiency and increasing the available peak power. Unfortunately, fully integrated voltage regulator modules (FIVR) requires a considerable design effort, therefore conversion implemented directly on the package can be a good compromise for ASIC applications. Switched capacitor (SC) DC-DC converters have become increasingly convenient for high-density conversion [6] because of the relatively high energy-density of capacitors compared to inductors [6], [17]. Moreover, they can be potentially integrated in scaled CMOS technologies [7], [10]. The on-package conversion system proposed in this paper is based on a fixed-ratio switching capacitor structure, as reported in Fig 1. The resonant converter is composed of two phases connected in parallel operating with a 180 phase shift, where each phase is composed of 20 elementary cells.

The area required for the conversion system is about 20 mm $\times$ 50 mm and can supply up to 300 A. With a 2:1 switching capacitor conversion the input supply voltage of the ASIC is doubled and the input pins are potentially halved. In order to improve the system efficiency and together to reduce the output impedance of the converter, the switched capacitor

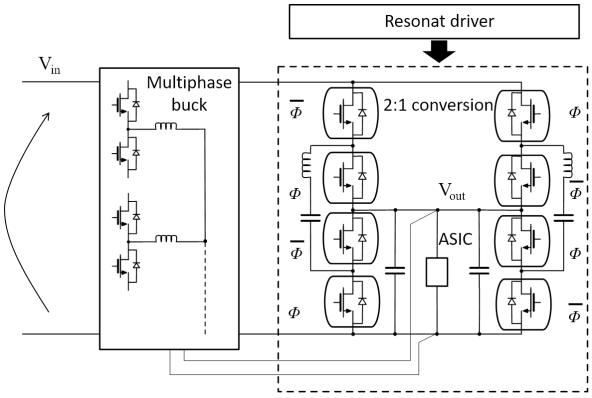

Fig. 1: Representation of the main architecture of the converter.

circuits are driven at the resonant frequency of the flying capacitor, operating as a resonant switching converter. To minimize the output impedance many switches are connected in parallel, making driving losses a crucial issue, especially at light load. In order to overcome this limitation, a new driving technique is presented and tested, where a single resonant structure is used to commute all the elementary cells in a phase, allowing to recycle gate charge energy.

The paper is organized as follows: in session II the switching capacitor circuit characteristics, the operation principle and the total output impedance are reported; in session III the resonant driving architecture is discussed, while in session IV and V experimental results and conclusions are presented.

II. Converter architecture

Each power switch reported in Fig. 1 is composed by the parallel of 20 devices organized in cells, each one with the structure reported in Fig 2. In every elementary cell, a block of three capacitors is switched at fixed frequency; hence the total number of capacitors is 60 per phase. Commuting the capacitor block near its resonant frequency ensures a sinusoidal current excitation, that is rectified to the output through the same cell structure. Charge balance among C_p terminals ensures

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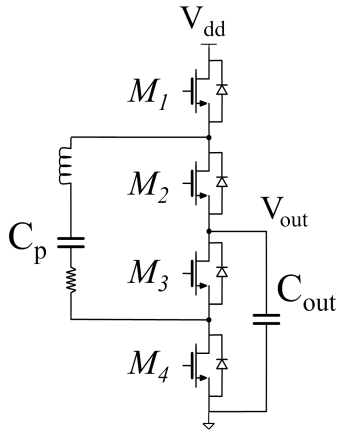

Fig. 2: Elementary switched-capacitor cell schematic.

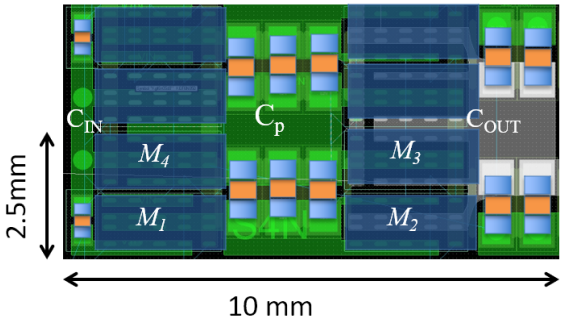

Fig. 3: Elementary switched-capacitor cell layout.

$V_{out} = V_{in}/2$ in steady state. Output voltage is filtered by output capacitors placed at the output of every cell, as reported in Fig. 3. As the converter is operated at resonant frequency, every switch commutation is at zero-current.

One of the most important performance indicator for the converter is the output impedance; in the closed-loop architecture reported in Fig. 1, without using load line regulation, it can be expressed as:

$$Z_{out}^{CL}(f) = \frac{Z_{out}^{OL}(f)}{1 + G_{loop}(f)} \tag{1}$$

where $Z_{out}^{OL}(f)$ is the open-loop impedance and $G_{loop}(f)$ is the loop transfer function of the full regulated system of Fig. 1, that includes the series of the buck converter together with the SC and the controller. Output impedance in the open-loop condition can be evaluated using equation (2) [18], this estimation is consistent when the impedances of the input and output capacitors are negligible:

$$Z_{out}^{OL}(0) = \frac{\pi^2 R_{cell}}{8} \tag{2}$$

where R_{cell} is the total resistance due to the series of the MOS on-resistance and the total ESR of the structure.

One of the contribution of this work is to measure the real shape of the output impedance $Z_{out}^{OL}(f)$ of the converter in the open-loop configuration, enabling the possibility for the correct selection of the regulator parameters. The equivalent small-signal model of the unregulated converter is reported in Fig. 4, where the small-signal input voltage is zero.

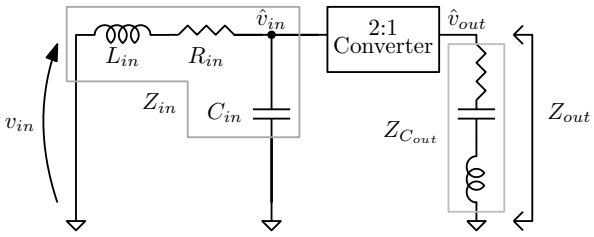

Fig. 4: Equivalent small signal model of the converter.

While equation (2) is compact and yields, under certain conditions, a fast estimation of the open-loop value of the impedance at low frequencies, the behavior of $Z_{out}^{OL}(f)$ is far more complex and its calculation was proven to require the study of a periodically time-varying system. As the analytical approach is not in this paper's purpose, the evaluation is carried out at different frequencies through the direct injection of a regulated load current. The converter structure (without the first stage) is composed of the input impedance Z_{in}, the 2:1 conversion cells and the output capacitance $Z_{C_{out}}$. Circuit-level simulation of Fig. 5 shows three main frequency intervals where $Z_{out}^{OL}(f)$ changes accordingly with the small signal model of Fig. 4. Impedance at low frequencies is dominated by $R_{in}/4$, that is the total resistance between the first stage and the output, divided by the squared converter transformation ratio. After the resonance between the input line impedance L_{in} and the input capacitance C_{in}, the output impedance becomes dominated by the SC-converter cell impedance, approaching the value of (2). Regulated-system's closed-loop crossover frequency is usually set inside this interval. At high frequency the converter influence decreases and C_{out} is the only contributor to Z_{out}.

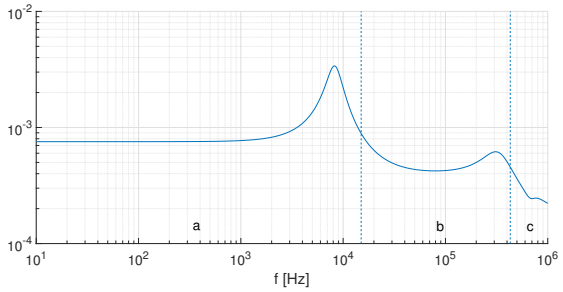

Fig. 5: Open-loop output impedance simulation. $Z_{out}^{OL}(f) \simeq Z_{in}/4$ (a); $Z_{out}^{OL}(f) \simeq \frac{\pi^2 R_{cell}}{8}$ (b); $Z_{out}^{OL}(f) \simeq Z_{C_{out}}$ (c).

As each phase can be considered a converter, even if made by the parallel of many components, consideration issues on current sharing are limited and the problem must be solved imposing device matching constraints.

III. Driver Architecture

The most noticeable drawback of the solution is the driving power loss, caused by the large number of devices connected

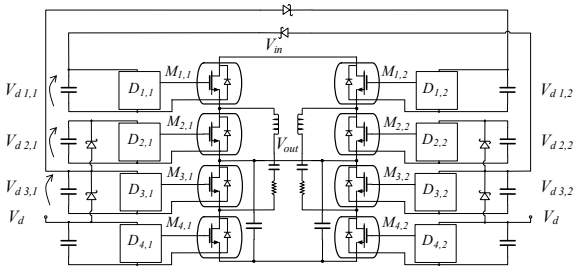

Fig. 6: Driver architecture for the 2:1 converter.

in parallel. The top-level view of the driver architecture is reported in Fig 6, where each group of paralleled switches $M_{x,y}$ is driven by a dedicated driver with a floating supply, obtained with a multilevel bootstrap capacitor system. In order to increase the system efficiency, the resonant driver topology of Fig. 7 is adopted. The architecture is based on a multilevel half bridge with a clamping capacitor C_c. As shown in Fig. 8, The central node V_a commutates into three different levels: 0, $V_{dd}/2$ and V_{dd} with a fixed timing sequence. Each FET of the driver is activated with a commercial IC with independent high side and low side input. Obviously, a suitable form for this driving architecture is an fully integrated driver with only an external capacitor C_c.

The structure exploits the calibrated strip inductance form the drivers to the parallel connection of the transistor as resonance inductor, and the total C_{iss} of the paralleled switches as resonance capacitor. At t_0 the V_a node commutates to $V_{dd}/2$, starting a resonant voltage transient between the L_{str} and the total C_{iss} capacitance. During this interval, V_{gs} can be expressed as

$$V_{GS}(t) = V_{dd}(1 - \cos(\omega_{cc}(t - t_0))) \tag{3}$$

where ω_{cc} is the resonance frequency of the network during the phase from $(t_0 - t_1)$

$$\omega_{cc} = \sqrt{\frac{1}{L_{str} N C_{iss}}} \tag{4}$$

and N is the number of devices connected in parallel.

The duration of this phase is fixed to to one half of the resonance period, allowing the zero-current commutation of the drivers' switches and reaching the voltage supply of the driver V_{dd} at the end of the phase. Considering $V_{gs}(t_1) = V_{dd}$, during the interval $(t_1 - t_2)$ V_{gs} remains stable and equal to V_{dd}. To turn off the switch the driver commutates the output to $V_{dd}/2$ at t_2 by using the same switching configuration of phase $(t_0 - t_1)$. In this interval, the voltage V_{gs} has an opposite commutation respect to the $(t_0 - t_1)$ interval; as before, this interval lasts half of the resonance period. During the intervals $(t_0 - t_1)$ and $(t_2 - t_3)$ the current I_{Lres} has a sinusoidal shape with opposite signs as reported in Fig. 8. Using the same switch configuration in the two intervals the gate charge extracted form the driver supply during $(t_0 - t_1)$ is restored in $(t_2 - t_3)$.

Thanks to the resonant operation, power losses of this driver are limited to the conduction losses associated with the gate current pulses. The total resistance on the driver path is

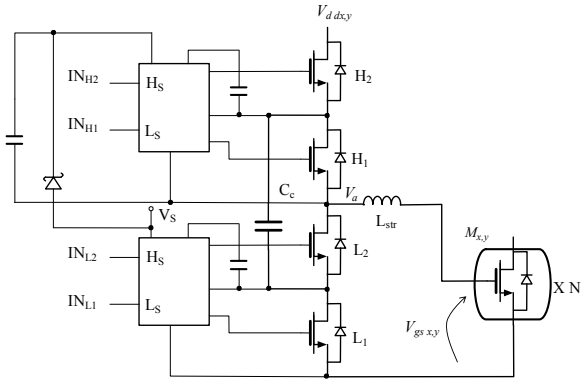

Fig. 7: Single driver circuit.

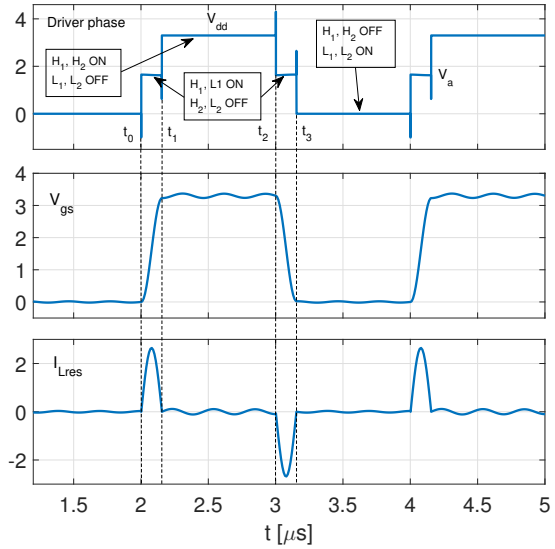

Fig. 8: Circuit-level simulation of the driver operation.

composed of the parasitic resistance of C_C, the R_{dsON} of the FETs $H_{1,2}$ and $L_{1,2}$ of Fig.7, the gate resistance of the power FETs and finally the strip resistance.

$$R_{driving} = ESR_{C_c} + 2R_{dsON} + R_{strip} \tag{5}$$

Considering the waveforms reported in Fig. 8, the inductor peak current can be approximated as:

$$\max|I_L| = \frac{Q_g}{T_{cc}} \pi N \tag{6}$$

Where Q_g represents the gate charge of a single FET, N is the number of FETs connected in parallel and T_{cc} is the resonance period of the driving structure. The total losses of the driver can be derived easily from (5) and (6).

$$\begin{aligned} P_{loss} &= \left(\frac{Q_g}{T_{cc}} \pi N\right)^2 \frac{R_{driving}}{2} \frac{T_{cc}}{T_{sw}} \\ &= \frac{R_{driving}}{2} \frac{f_{cc}}{T_{sw}} {Q_g}^2 \ \pi^2 \ N^2 \end{aligned} \tag{7}$$

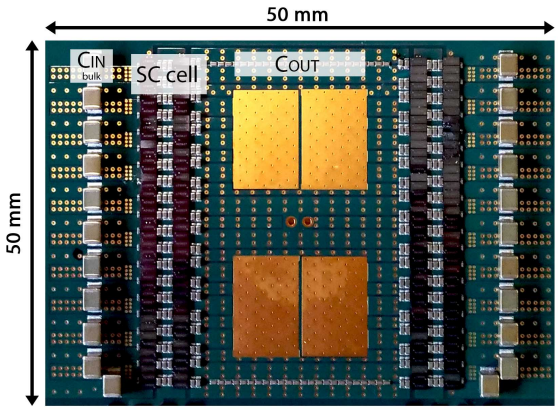

Fig. 9: Power stage on the PCB prototype.

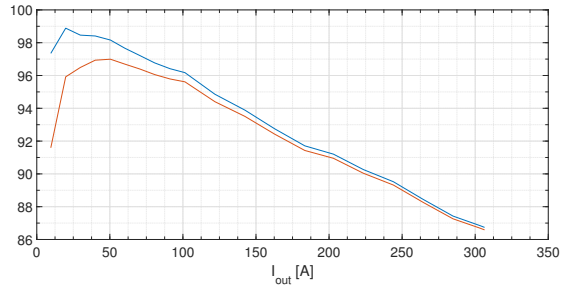

Fig. 10: Measured converter efficiency with driving losses (red) and without driving losses (blue).

IV. Experimental Results

A 10-layers prototype PCB was built in order to demonstrate the effectiveness of the solution. Table I summarizes the main specifications of the prototype. The first stage was implemented through a multi-phase VRM buck.

TABLE I: Converter and PCB specifications

$V_{in,nom}$	1.6 V
$V_{out,nom}$	0.8 V
$I_{out,max}$	300 A
f_{sw}	500 kHz
PCB power area	50 × 50 mm
PCB copper width	75 μm
MOSFETs (power + driving)	Intersil KGF20N05D (160 + 32)
Switched capacitors	Murata GRM155Z80E226M (120)

Prototype efficiency was measured with precision current shunt resistors and it's reported in Fig. 10. The power converter, neglecting driving losses, has a 98.8 % measured peak efficiency. With an overall driving current of only 150 mA at 3.3 V (0.495 W), measured total peak efficiency is 97 %. Without the resonant driver, driving losses would be as high as:

$$P_{driving}^{standard} = Q_{gate} V_{drive}^2 f_{sw} N_{mos_tot} \simeq 1.74W \quad (8)$$

Driving waveforms can be observed in Fig. 11, where gate-source voltages are reported the pair of switches H1, H2 of Figure 7. Voltage measured on a single switched-capacitor cell is shown in Fig. 12 with 100 A output current.

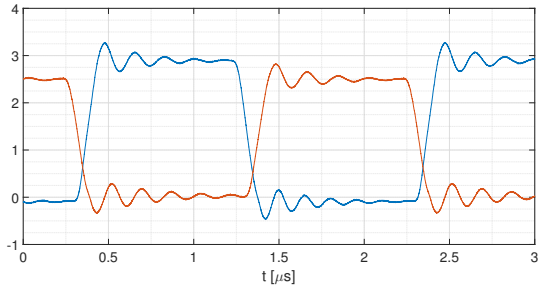

Fig. 11: Measured V_{gs} voltage of MOSFET columns H1 (blue) and H2 (red) as in Figure 8.

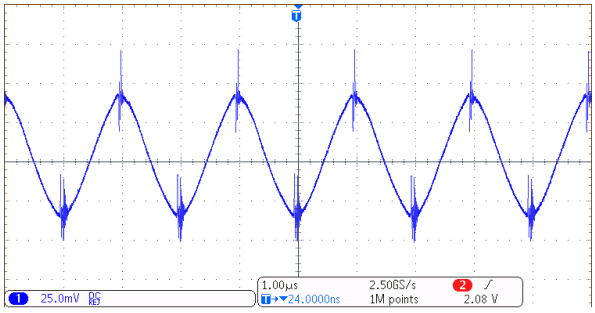

Fig. 12: Switched capacitor voltage at 100 A output current.

The active-load tool (DLT100AGEVB, ON Semiconductor) allowed to directly measure the output open-loop impedance in wide frequency range, validating the theoretical model discussed in section II. The results are reported in Fig. 13: considering the middle frequency range, where Z_{out} depends on the converter's SC impedance, a minimum value of $|Z_{out,min}| \simeq 411\ \mu\Omega$ is measured, coherently with the value calculated with (2) and with the circuit-level simulation.

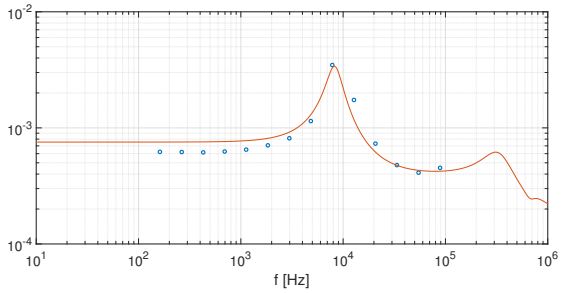

Fig. 13: Open-loop output impedance $|Z_{out}^{open}(f)|$ simulated (red line) and measured with active load tool (blue dots).

V. Conclusions

In this paper is proposed a in package conversion system based on resonant switched capacitors for high current (up to 400 A) low voltage (0.8 V) digital ASICs, in an area of 10 cm^2. Experimental results confirm the effectiveness of the solution with a 98.8 % peak efficiency and a very small driving current (150 mA at 3.3 V) that makes the new proposed resonant driver the correct choice for this type of converter. The direct

measurement of the output impedance validates the theoretical model for the SC-converter and allows consistent selection of the regulator's parameters.

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