Modeling and Control of Sigma Converter for 48V Voltage Regulator Application

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Abstract— For the new-generation of server voltage regulators modules (VRMs), companies are employing the use of 48V bus to improve system efficiency and to reduce the cost of datacenters. For 48V to 1V VRM, a quasi-parallel topology, the sigma converter, is shown to have 93.4% maximum efficiency and 420W/in3 power-density. In order to design the sigma converter to meet the VRM requirements, the large-signal performance as well as the small-signal behavior of the converter must be studied. In this paper, the small-signal model is examined, a voltage-mode control design is provided, and hardware measurements are presented.

Keywords—48V voltage-regulator, sigma converter, small-signal model, voltage-mode control

I. INTRODUCTION

With the desire for higher performance devices and more compact designs, many of the storage and computing needs of portable electronics are being relocated to data centers via cloud services. Inside these data centers are racks of motherboards each housing multiple high-performance multi-core processors. Traditional server architectures support a 12V bus to distribute power to the VRMs supplying power to the processors. However with the increasing power consumption the processors, the loss due to the 12V bus became excessive and degrades the efficiency of the overall system.

In an effort to reduce the loss and increase the efficiency of datacenters, companies are looking toward the 48V bus for server applications [1]. The 48V bus has been in use by the telecom industry but the power regulation specification for server application is much more stringent. A considerable amount of research is being conducted for the 48V VRM but only a couple of commercial product are available [2]-[6]. A 48V to 1V, 80A sigma converter with a power density of 420W/in^3 and a maximum efficiency of 93.4% is demonstrated by M. Ahmed et. al. [7]. However, it is unclear how the system will perform under the conditions required for server VR. Modeling of the sigma converter was previously done by P. Lai and J. Sun in [8] but their modeling approach for the DC transformer (DCX) is outdated the accuracy of the model is questionable for various types of converters that could be used for the DCX. In this paper, a more accurate model is proposed for the sigma converter proposed in [7] for VR application.

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II. SMALL SIGNAL MODEL OF THE SIGMA CONVERTER

The 48V to 1V, 80A sigma converter proposed in [7] is composed of a fixed-frequency LLC converter running at resonant frequency, and a buck converter connected in a quasi-parallel configuration; the inputs of the converters are connected in series and the output are connected in parallel as shown in Fig. 1. The small signal model of this sigma converter can be obtained by connecting the models of the buck and LLC converters in the sigma configuration if all input and output behaviors of the converters are preserved by the models.

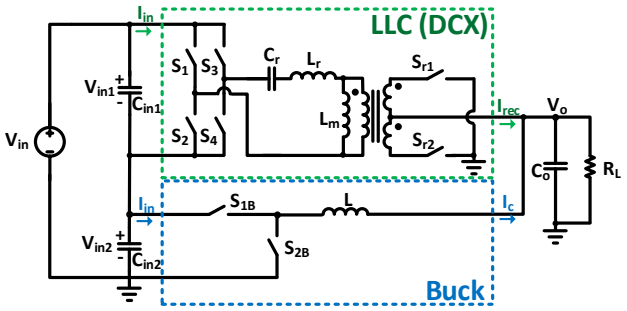

Fig. 1. Sigma converter.

The existing small-signal model of the LLC converter is too complicated for the purpose of this sigma converter [9]. In this sigma converter, the operation of the LLC is fixed at the resonant frequency. Under this condition, the LLC equivalent circuit model with simplified resonant capacitor branch, shown in Fig. 2, can be further simplified. With fixed frequency operation, the frequency variation terms (ω_s) no longer exist. At resonant frequency, (1) simplifies to zero and (2) simplifies to (3). With these conditions and only retaining the input and output behaviors of the converter, the LLC equivalent circuit model simplifies to the model shown in Fig. 3.

The buck converter small-signal equivalent circuit model is shown in Fig. 4 [10]. By combining the simplified LLC and the buck equivalent circuit models in the sigma configuration, the small-signal equivalent circuit model of the sigma converter is obtained and shown in Fig. 5. This model is used

to analyze the behavior and performance of the sigma converter.

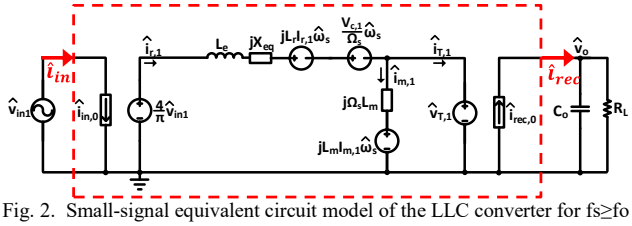

Fig. 2. Small-signal equivalent circuit model of the LLC converter for fs≥fo with simplified resonant capacitor branch [9].

$$X_{eq} = L_r\Omega_s\left(1 - \frac{\Omega_o^2}{\Omega_s^2}\right) \tag{1}$$

$$L_e = L_r\left(1 + \frac{\Omega_o^2}{\Omega_s^2}\right) \tag{2}$$

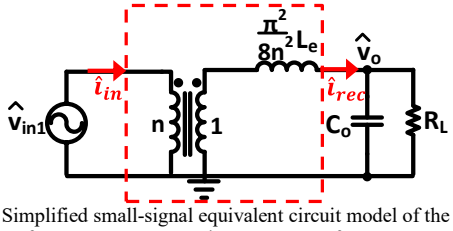

Fig. 3. Simplified small-signal equivalent circuit model of the fixed-frequency LLC operating at resonant frequency.

$$L_e = 2L_r \tag{3}$$

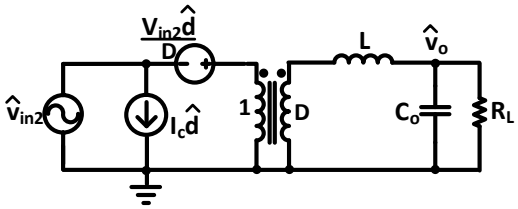

Fig. 4. Small-signal equivalent circuit model of the buck converter [10].

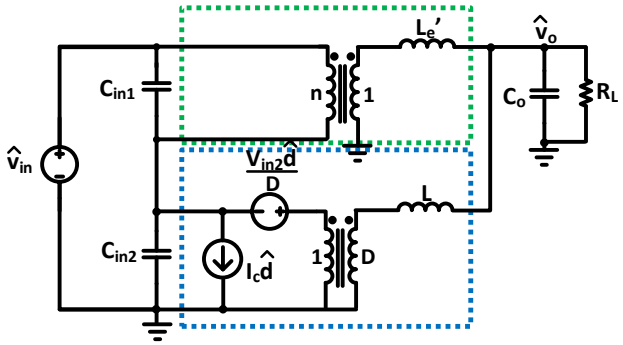

Fig. 5. Small-signal equivalent circuit model of the sigma converter.

A. Output Impedance

Evaluating the model shown in Fig. 5 for the open-loop output impedance (Z_o), the model simplifies to the circuit shown in Fig. 6 where the transfer function is given by (4) with variables given by (5)-(10) under the conditions $L>>L_e$' and $n^2C_{in}>>C_o$. The bode plot of Z_o is shown in Fig. 7 where V_{in}=48V, V_{in1}=40V, V_{in2}=8V, V_o=1V, D=0.125, n=40, C_{in1}=4u, C_{in2}=20uF, L_r=190nH, L=190nH, R_L=12.5mΩ, and C_o=3.6mF. From Fig. 7, it can be observed a sigma converter can naturally achieve low output impedance since both C_{in} and C_o help in reducing the impedance at different frequency ranges.

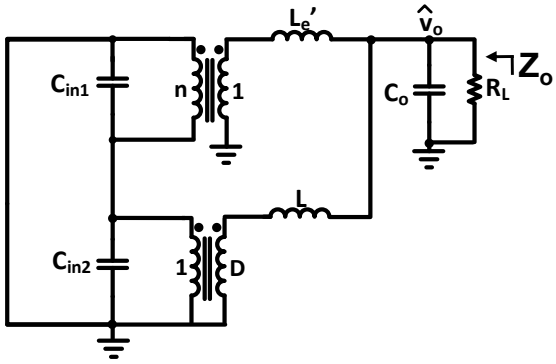

Fig. 6. Small-signal equivalent circuit model of the sigma converter open-loop output impedance.

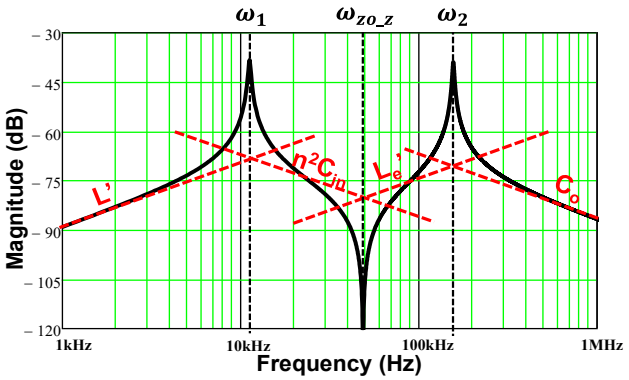

Fig. 7. Bode plot of modeled Z_o.

$$Z_o(s) \cong \frac{L's\left(1 + \frac{s^2}{\omega_{zo_z}^2}\right)}{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)} \tag{4}$$

$$C_{in} = C_{in1} + C_{in2} \tag{5}$$

$$L' = \frac{L}{(1+nD)^2} \tag{6}$$

$$L_e' = \frac{\pi^2 L_r}{4n^2} \tag{7}$$

$$\omega_{zo\_z} = \sqrt{\frac{1}{L_e'(n^2C_{in})}} \tag{8}$$

$$\omega_1 = \sqrt{\frac{1}{L'(n^2C_{in})}} \quad Q_1 = R_L\sqrt{\frac{n^2C_{in}}{L'}} \tag{9}$$

$$\omega_2 = \sqrt{\frac{1}{L_e'C_o}} \quad Q_2 = R_L\sqrt{\frac{C_o}{L_e'}} \tag{10}$$

At low frequencies, the impact of the buck and the LLC converters on Z_o can be observed through L'. As the frequency range increases, a low-frequency double-pole is formed at ω_1 with the impact of the input capacitors and the LLC converter,

observed through n^2C_{in}. When the frequency range further increases, a double-zero is formed at ω_{zo_z} with the impact of the LLC converter, observed through L_e'. At high frequency a high-frequency double-pole is formed at ω_2 with the impact of the output capacitor (C_o).

In a realistic design, the parasitic resistances of the converter impact the behavior of the system and need to be taken into consideration. As shown in Fig. 8, parasitic resistances of the LLC primary-side switching devices (R_{ds_on}), primary-side winding (R_{pri}), secondary-side switching devices ($R_{ds\_on\_sr}$), secondary-side winding (R_{sec}), the buck high-side switching device ($R_{ds\_on\_1B}$), low-side switching device ($R_{ds\_on\_2B}$), and the inductor (R_{DCR}) need to be included in the model. Using the average modeling concept, the parasitic resistances of the LLC can be simplified to R_{llc} and the parasitic resistances of the buck converter can be simplified into R_{buck} as shown in Fig. 9.

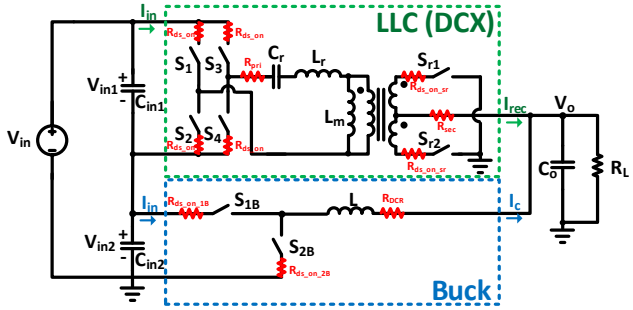

Fig. 8. Sigma converter with parasitic resistances.

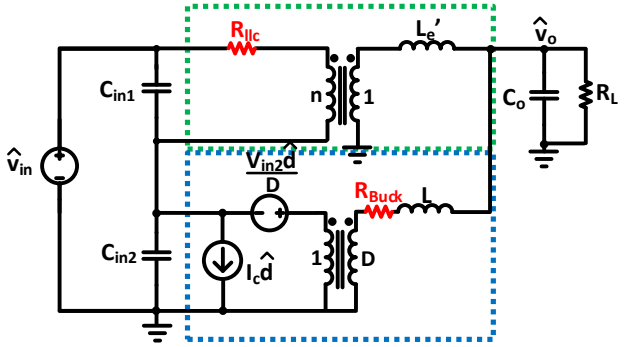

Fig. 9. Small-signal equivalent circuit model of the sigma converter with parasitic resistances.

Evaluating the model in Fig. 9 for Z_o with parasitic resistances, the model simplifies to the circuit shown in Fig. 10 where the transfer function is given by (11) with variables given by (5)-(7) and (12)-(16) under the conditions L>>L_e' and n^2C_{in}>>C_o. The bode plot of Z_o with parasitic resistance is shown in Fig. 11 where V_{in}=48V, V_{in1}=40V, V_{in2}=8V, V_o=1V, D=0.125, n=40, C_{in1}=4u, C_{in2}=20uF, L_r=190nH, L=190nH, R_L=12.5mΩ, C_o=3.6mF, R_{llc}=1.433Ω, and R_{Buck}=5mΩ. The Simplis simulated result is also shown in Fig. 11; the model matches well with simulation. From Fig. 11, it can be observed the parasitic resistances increase the DC gain, moving the low frequency zero higher, reduce the Q factor of the low-frequency double-pole, separating and recombining the double-zero and high-frequency double-pole resulting in a single-zero and single-pole. Even with the increase in impedance at low-frequencies, the sigma converter still has very small output impedance overall.

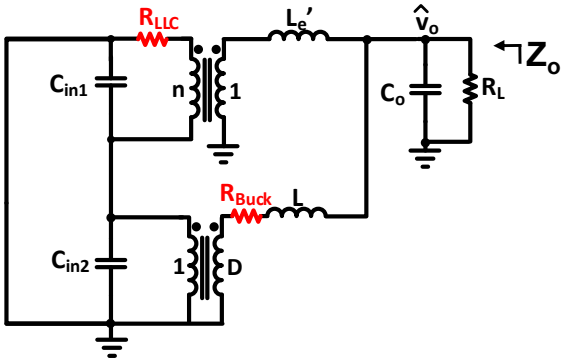

Fig. 10. Small-signal equivalent circuit model of the sigma converter open-loop output impedance with parasitic resistances.

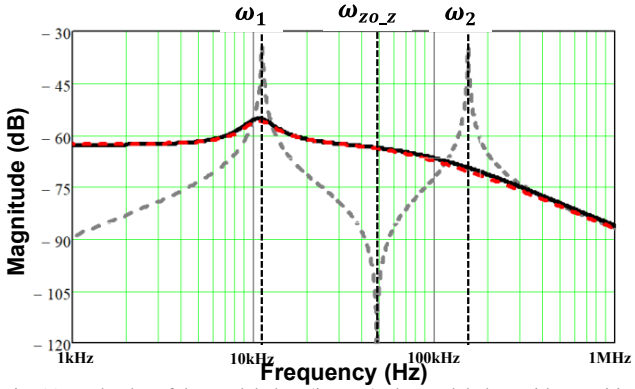

Fig. 11. Bode plot of the modeled Z_o (in gray), the modeled Z_o with parasitic resistances (in black), and the Simplis simulated Z_o with parasitic resistances (in red).

$$Z_o(s) \cong \frac{Z_{o_{DC}}\left(1+\frac{L's}{Z_{o_{DC}}}\right)\left(1+\frac{s}{\omega'_{zo\_z}}\right)}{\left(1+\frac{s}{Q'_1\omega'_1}+\frac{s^2}{\omega'^2_1}\right)\left(1+\frac{s}{\omega'_2}\right)} \quad (11)$$

$$Z_{o_{DC}} = \frac{R_{LLC}D^2 + R_{Buck}}{(1+nD)^2} \quad (12)$$

$$\omega'_{zo\_z} = \frac{1}{C_{in}R_{LLC}} \quad (13)$$

$$\omega'_1 = \sqrt{\frac{1+\frac{R_{Buck}}{R_L}}{L'(n^2C_{in})}} \quad (14)$$

$$Q'_1 = \frac{R_L}{1+\frac{n^2C_{in}R_{Buck}R_L}{L}}\sqrt{\frac{n^2C_{in}\left(1+\frac{R_{Buck}}{R_L(1+nD)^2}\right)}{L'}} \quad (15)$$

$$\omega'_2 = \sqrt{\frac{1+\frac{R_{LLC}}{R_Ln^2}}{L_e'C_o}} \quad (16)$$

B. *Control-to-Output Voltage*

Evaluating the model in Fig. 5 for the control-to-output voltage (G_{vd}), the model simplifies to the circuit shown in Fig. 12 where the transfer function is given by (17) with variables

given by (5)-(7), (9), (10), and (18)-(24) under the conditions $L>>L_e'$ and $n^2C_{in}>>C_o$. When considering the effect of parasitic resistances, the model is modified as shown in Fig. 13 where the transfer function is given by (21) with variables given by (5)-(7), (14)-(16), and (21)-(23) under the conditions $L>>L_e'$ and $n^2C_{in}>>C_o$.

The bode plots of G_{vd} with and without parasitic are shown in Fig. 14 where V_{in}=48V, V_{in1}=40V, V_{in2}=8V, V_o=1V, D=0.125, n=40, C_{in1}=4u, C_{in2}=20uF, L_r=190nH, L=190nH, R_L=12.5mΩ, C_o=3.4mF, R_{llc}=1.433Ω, R_{Buck}=5mΩ, and I_o=15A. In Fig. 14, it can be observed the parasitic resistance in the sigma converter will reduce the Q values of the double-poles and double-zero. Also shown in Fig. 14, the model matches well with the Simplis simulation.

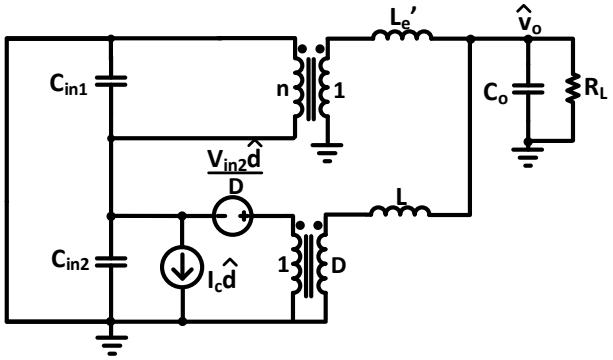

Fig. 12. Small-signal equivalent circuit model of the sigma converter open-loop control-to-output voltage.

$$G_{vd}(s) \cong \frac{G_{vd\_DC}\left(1+\frac{s}{Q_{vd\_z}\omega_{vd\_z}}+\frac{s^2}{\omega_{vd\_z}^2}\right)}{\left(1+\frac{s}{Q_1\omega_1}+\frac{s^2}{\omega_1^2}\right)\left(1+\frac{s}{Q_2\omega_2}+\frac{s^2}{\omega_2^2}\right)} \tag{17}$$

$$G_{vd\_DC} = \frac{V_{in2}}{1+nD} \tag{18}$$

$$\omega_{vd\_z} = \sqrt{\frac{1+nD}{L_e'(n^2C_{in})}} \tag{19}$$

$$Q_{vd\_z} = \frac{V_{in2}}{I_C n^2(1+nD)L'}\sqrt{\frac{L_e'C_{in}}{1+nD}} \tag{20}$$

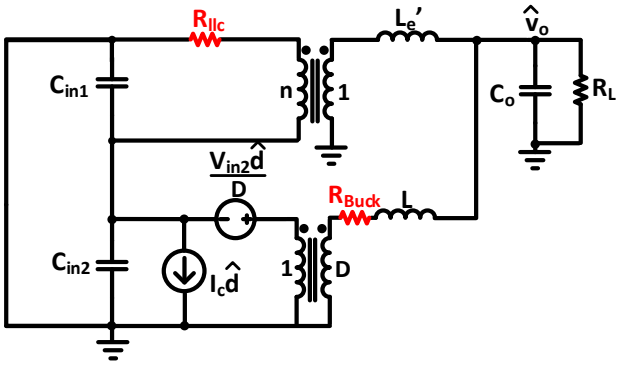

Fig. 13. Small-signal equivalent circuit model of the sigma converter open-loop control-to-output voltage with parasitic resistance.

$$G_{vd}(s) \cong \frac{G_{vd\_DC}'\left(1+\frac{s}{\omega'_{vd\_z}}\right)}{\left(1+\frac{s}{Q_1'\omega'_1}+\frac{s^2}{\omega'^2_1}\right)\left(1+\frac{s}{\omega'_2}\right)} \tag{21}$$

$$G_{vd\_DC}' = \frac{V_{in2}-R_{LLC}-R_{buck}}{1+nD} \tag{22}$$

$$\omega_{vd\_z}' = \frac{1+nD}{C_{in}R_{LLC}} \tag{23}$$

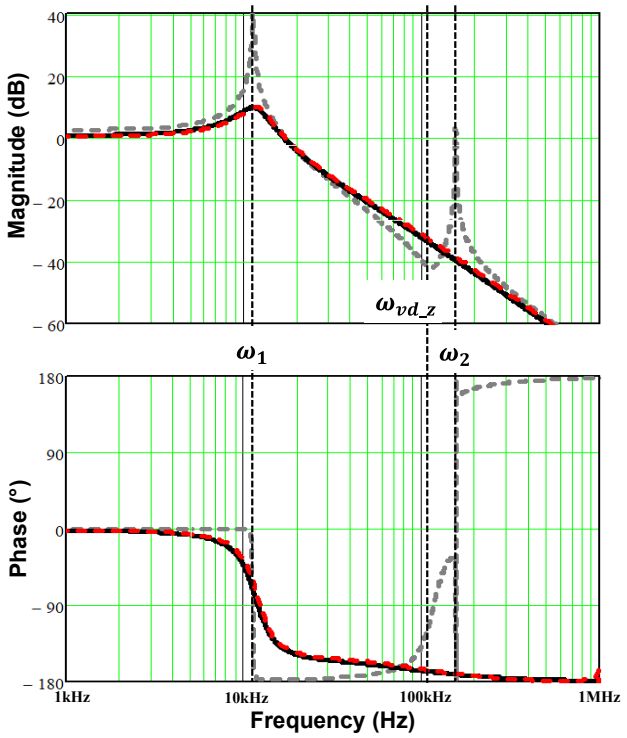

Fig. 14. Bode plot of the modeled G_{vd} (in gray), the modeled G_{vd} with parasitic resistance (in black), and the simulated Gvd with parasitic resistance (in red).

III. Sigma Converter with Voltage-Mode Control

A voltage-mode control can be designed for the sigma converter. Since the LLC is running at fixed frequency, only the buck switches are affected by the control as shown in Fig. 15. The loop gain (T_v) of the closed-loop converter is then given by (24), where H_v is the compensator transfer function. Using T_v, the closed loop output impedance (Z_{oc}) can be obtained, providing insight on the transient performance of the converter when load transient occurs.

Based on the behavior of G_{vd} with parasitic resistance, a type-III compensator is chosen to compensate the double-pole effect at ω_1. The compensator is designed with an integrator at DC, two zeros placed near ω_1, and two high-frequency poles beyond the bandwidth. The bode plots of the modeled and simulated H_v and T_v are shown in Fig. 16, and Z_{oc} is shown in Fig. 17.

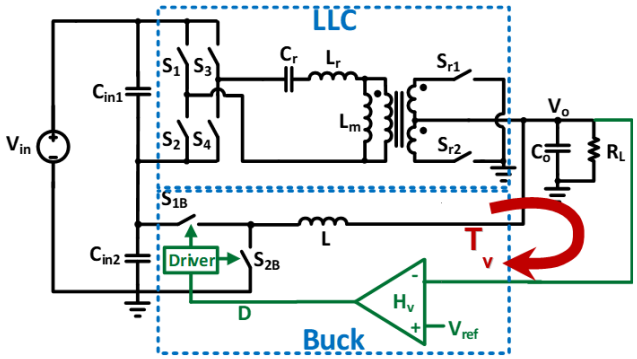

Fig. 15. Sigma converter with compensator $H_v(s)$.

$$T_v = G_{vd}(s) * H_v(s) \tag{24}$$

$$Z_{oc} = \frac{Z_o}{1 + T_v} \tag{25}$$

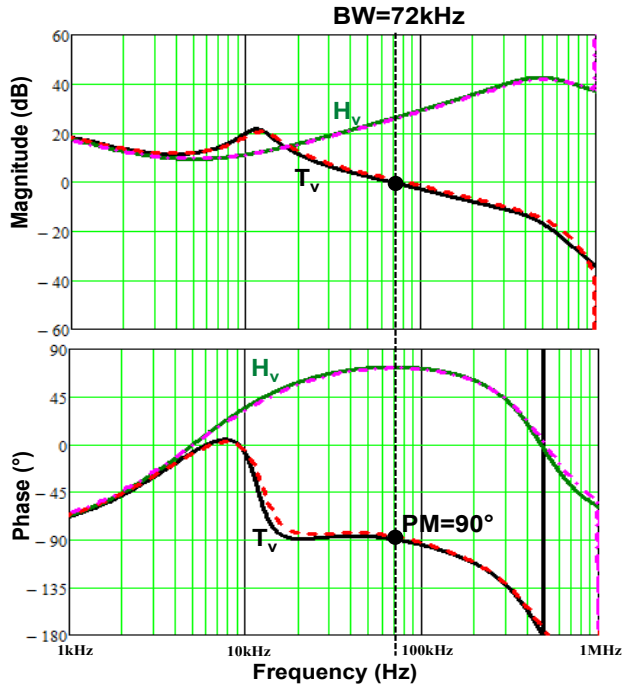

Fig. 16. Bode plot of the modeled T_v (in black), the simulated T_v (in red), the modeled H_v (in green), and the simulated H_v (in purple).

As mentioned before, the sigma converter can naturally achieve low output impedance due to the C_{in} and C_o working together to reduce impedance at different frequency ranges. As a result, high-bandwidth design is not necessary but will further reduce output-impedance and improve transient performance. For the voltage-mode controlled sigma converter design, the simulated transient performance of the closed-loop system is shown in Fig. 18 with V_{in}=48V, V_{in1}=40V, V_{in2}=14V, V_o=1V, D=0.125, n=40, C_{in1}=4u, C_{in2}=20uF, L_r=190nH, L=190nH, C_o=3.4mF, R_{llc}=1.433Ω, R_{Buck}=5mΩ, I_o=20-80A and di_o/dt=100A/us. From Fig. 18, the designed sigma converter has an undershoot of 20mV and an overshoot of 31mV.

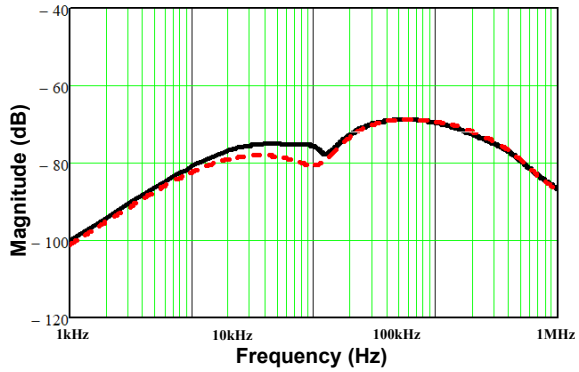

Fig. 17. Bode plot of the modeled Z_{oc} (in black) and the simulated Z_{oc} (in red).

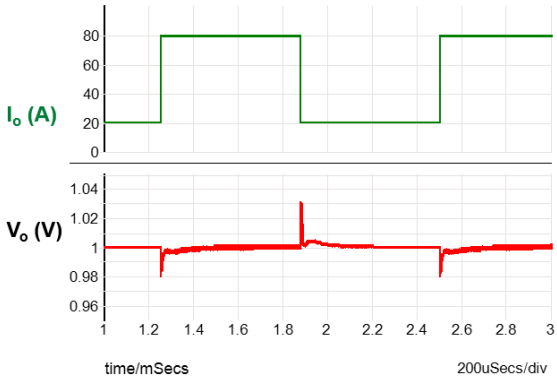

Fig. 18. Simplis simulation of the transient performance with V_{in}=48V.

IV. Experimental Results

A 48V to 1V, 80A sigma converter hardware was designed and built where V_{in}=42-60V; V_o=0.8-1V; I_{o_max}=80A; LLC operating at 1MHz with L_r=190nH, C_r=120nF, L_m=36uH; and voltage-mode controlled buck operating at 600kHz with L=190nH. The controls for both the LLC and the buck converter are implemented using a 60MHz micro-controller (MCU) with the start-up sequence from [11]. The transient performance of the sigma converter is shown in Fig. 19. From Fig. 19, the output voltage overshoot and undershoots are 30mV, matching well with the simulation results in Fig. 18.

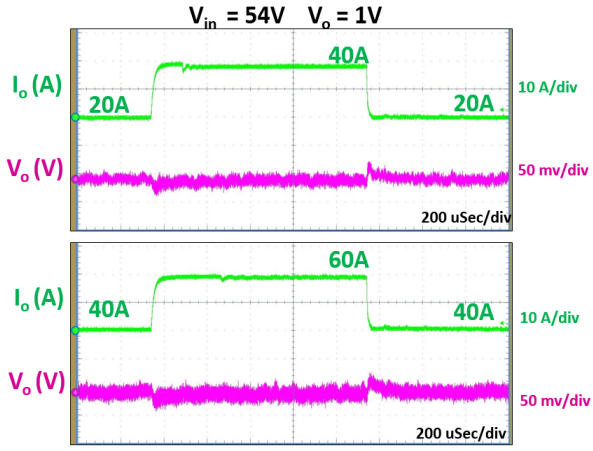

Fig. 19. Sigma converter transient performance waveforms with various load current and V_{in}=54V.

V. Conclusion and Future Work

In this paper, the behavior of the sigma converter is examined for the VR application using the proposed small signal model. The sigma converter naturally has a low output impedance due to the contribution of both the input and output capacitors in reducing the impedance at different frequency ranges. As a result, undershoot and overshoot less than 50mV is observed when load transient occurs.

Future works include the model and analysis of sigma converter with current-mode control methods for VRM application.

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