Performance Optimization of A 1.2kV SiC High Density Half Bridge Power Module in 3D Package

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***Abstract*—Wide bandgap power semiconductor devices show significantly superior performance than Si power devices, power module solutions are being investigated trying to improve system-level performance by applying SiC and GaN power devices in various applications. This paper introduces the design of a 1.2kV high density SiC half bridge intelligent power module based on 3-dimensional package concept, also addressed is the performance optimization of the proposed power module design. In the designed module, SiC MOSFETs and corresponding gate driver circuits in half bridge are interconnected vertically with high interconnection density and low power loop profile. Ultra-low parasitic inductance, 1.3nH, is introduced from DC+ to DC-. Isolation function blocks and bootstrap power supplies are also integrated in the 3D package. An ultra-thin dielectric substrate, with good thermal and breakdown performance, is applied to further decrease the power module weight and volume. The entire 3-dimentional 1.2kV SiC power module are within 35mm × 15mm × 7mm space. Through optimization, the design can achieve 8ns turn-on transient with limited switching loss at up to 700V / 60A. Thermal performance of the designed module is also evaluated through simulations.**

Keywords—SiC, High Density, Intelligent Power Module, Ultra-low Parasitics, Fast Switching, 3D Package

I. INTRODUCTION

Wide Bandgap (WBG) power semiconductor devices, with superior properties than Si devices including higher voltage, higher frequency and higher temperature, enables power conversion design with boosted efficiency, compact physical structure and operation capability under harsh environment [1][2]. According to demands from industries, such as automobiles, telecommunications, aerospace and consumer electronics, next-generation power conversion systems, i.e. inverters and converters, must be much smaller in volume, weight, and cost [3].

Investigations in power module design is undergoing to facilitate advanced utilization of wide bandgap power devices and corresponding performance improvement of power conversion systems [4], such as high temperature capability [5], and high frequency operation [6]. Double sided planar power module [7][8], as a potential WBG power module approach, significantly reduces commutation inductance by eliminating bonding wires for interconnection, and also has better thermal performance due to double-side cooling. The approach also motives the emerging of 3D power module concept, which has better space utilization and great potential for high density power conversion systems. 3D packaging concept is primarily available and pursued in low voltage/current power supply market [9]. As more and more emerging materials[10] and design concept available, 3D packaging is gradually moving forward for high power high voltage applications [11].

This paper introduces a 1.2kV high density SiC half bridge Intelligent Power Module (IPM) in a 3D package design. In this design, high side SiC MOSFET and low side SiC MOSFET are interconnected vertically, together with corresponding gate driver circuits and isolation function blocks. A ultra-low parasitic inductance is achieved with the design, followed by fast switching transients of SiC MOSFETs. In Section II, the physical structure design and corresponding electrical circuits are introduced with details, fabrication details of the designed module will also be included. Section III analyzes detailed parasitic parameters extraced from Q3D simulations to verify potential application in high frequency operation of the design. Section IV features characterization of the designed module and implementation of further performance optimizations. In Section V, thermal simulations of the designed module are discussed. Conclusions are summarized in Section VI.

II. 1.2KV SIC IPM IN 3D PACKAGE

A. 3D Package Design of 1.2kV SiC Half Bridge IPM

In the designed module, a recently developed epoxy-resin based dielectric is applied as substrates. The thickness of dielectric layers are 80μm, with copper plates on both sides. It has comparable thermal conductance with alumina based DBC substrates, and has >4kV breakdown voltage with 1nA leakage at room temperature.

The physical structure of the 3D package design is as shown in Fig. 1. High side and low side SiC MOSFETs are located at two separate layers in the model, with corresponding gate driver circuits and isolation function blocks. Bootstrap

power supply are also integrated in the module. The link between high side MOSFET layer and low side one is the switching node at the middle as shown. The corresponding circuit is as shown in Fig. 2.

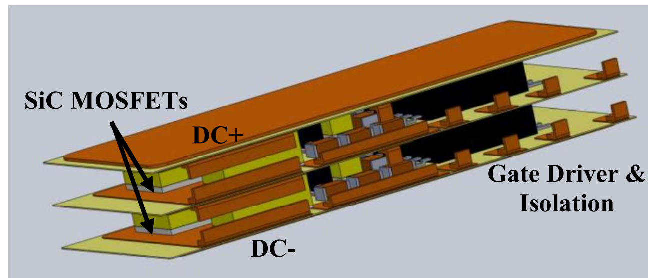


Fig. 1. 3D Packaging Design of 1.2kV SiC Half Bridge IPM.

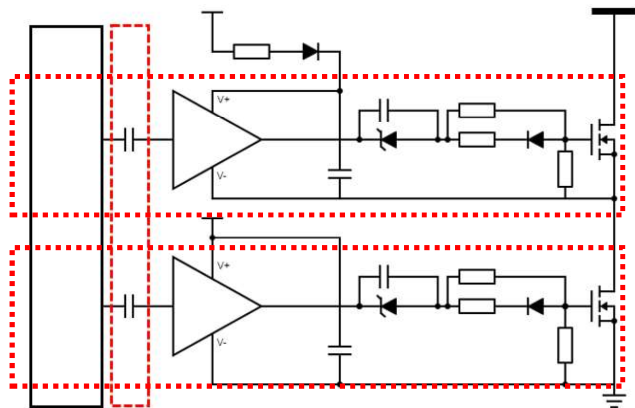


Fig. 2. Circuit schematic corresponding to 3D packaging design

The schematic is divided into highside MOSFET block and lowside MOSFET block, and the main power loop is as shown on both Fig. 1 and Fig. 2. Gate loop of each MOSFET is located on each layer, also as shown in Fig. 2. To eliminate gate loop commutation inductance, bonding wires on the gate terminals are avoided by flipping SiC MOSFET on each layer, so that the gate of MOSFET is connected with gate driver pin through Cu trace on the substrate. Also, since on bonding wires are applied on drain and source terminals of each device, and the ultra-thin substrate is applied, the gate loop is also short with limited parasitics.

B. Fabrications and Assembly

The proposed 3D structure complicates fabrication processes, since multiple layers requires die attachment reflow profiles. MoCu spacers are applied between SiC MOSFETs and its substrates to match the height difference with other components on the same level, at the same time to provide between thermal conduction and mechancial stress management.

Copper etching process are applied on every substrates with circuit interconnection layouts. All the terminals are left on one single side of the module, to promise double-side cooling feature during PCB board level applications, as shown in Fig. 3.

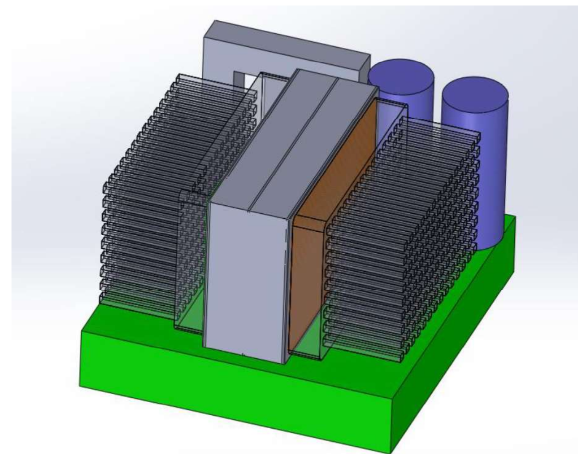


Fig. 3. 1.2kV SiC Half Bridge IPM with 3D packaging during PCB level power conversion application.

The more detailed description of fabrication and assembly processes can be found in [12]. The assemblied 1.2kV SiC half bridge IPM with 3D packaging design is as shown in Fig. 4, the overall size of the assembled IPM is within 35mm × 15mm × 7mm.

Fig. 4. Assemblied 3D 1.2kV SiC half bridge IPM.

III. PARASITIC PARAMETERS

Q3D is applied to extract parasitic parameters in the designed 3D power module. Since the gate driver is very close to gate terminals of MOSFETs, the gate loop parasitics is very limited. The analysis focuses on parasitic parameters extraction on the power loop. The simplified model of power stage in the 3D module is as shown in Fig. 5. The current path going through both high side and low side SiC MOSFETs are as shown.

Fig. 5. Power stage model for parasitic parameter analysis

Through simulation, the detailed parasitics is as shown in Table. I. The overall parasitic inductance in the power loop is limited to 1.3nH under DC condition. This promises limited ringing and overshoot of voltage during switching transient, even at fast switching condition. The ultra-low parasitic inductance ensure the potential application in high frequency operation of the designed 3D SiC power module.

TABLE I. PARASITICS EXTRACTION ON THE POWER LOOP

Location	Inductance / nH	Resistance / mΩ
DC+ → DC-	**1.3034**	**0.443**
High-side MOSFET Drain	0.4390	0.188
High Side MOSFET Source	0.1994	0.102
Low-side MOSFET Drain	0.4932	0.157
Low-side MOSFET Source	0.2327	0.149

To better explicit ultra-low parasitics on the power loop, each parasitic element at different location of the half bridge is also extracted as shown in Table I.

IV. CHARACTERISTICS AND OPTIMIZATION

Static characterizations of the designed module with ultra-thin dielectric substrate show that the module works with no degradation of SiC MOSFET performance, as indicated in [8]. Double pulse tests (DPT) are employed to verify switching performance of the designed module. External gate drivers with different configurations are applied as comparison.

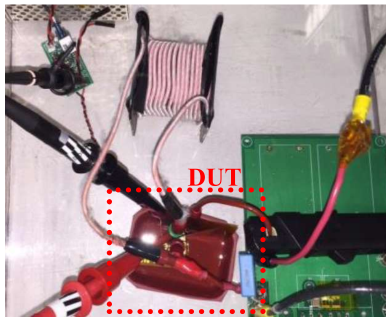
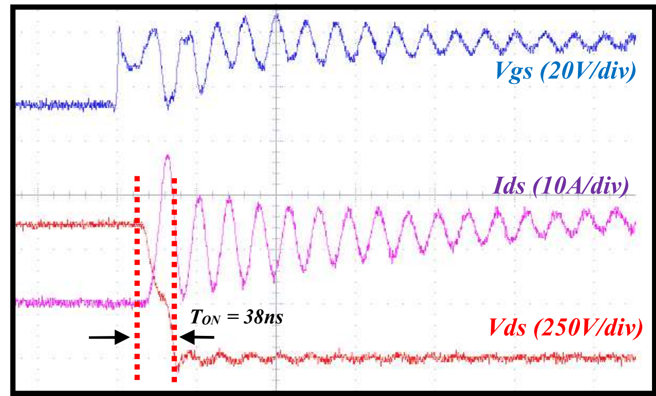


Fig. 6. DPT setup with external gate driver directly on the module under test

One of the test setup is as shown in Fig. 6. Kelvin connection is applied at gate and source of the device under test (DUT), the gate loop is long and directly applied on the module. Gate resistors are 5.0Ohm for turn-on and 2.5Ohm for turn-off switching transients. Assembled 3D SiC IPM is encapsulated by silicone gel during tests. The test results at 600V and 800V are as shown in Fig. 7 and Fig. 8.

At 600Vdc and 20A condition, the designed module enables turn-on time around 38ns, and turn-off time around 30ns, corresponding dV/dt is 15.8V/ns for turn-on and 20V/ns for turn-off. At 800Vdc and 40A condition, the designed 1.2kV 3D SiC power module achieves 16.7V/ns for turn-on transient and 25V/ns for the turn-off.



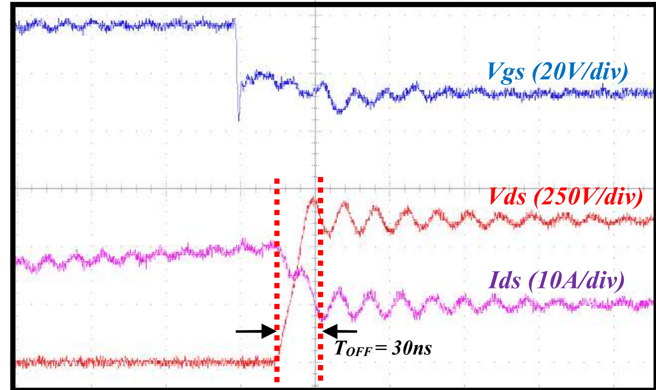
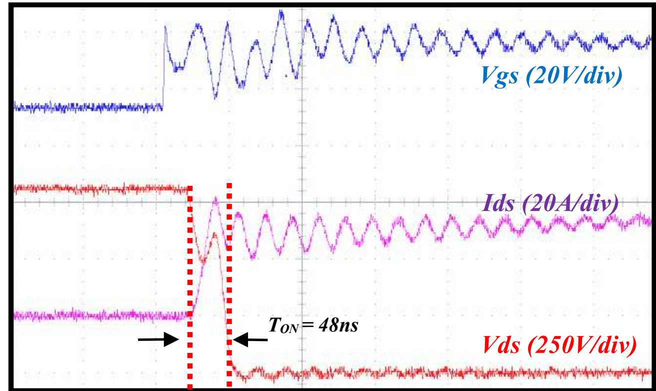


Fig. 7. Turn-on (up) and turn-off (down) switching transients at 20A, 600Vdc.



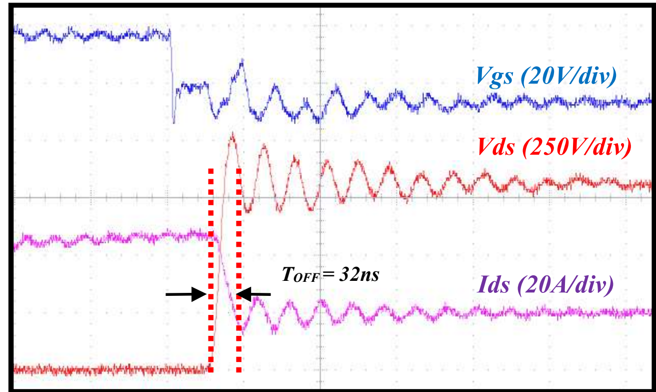


Fig. 8 Turn-on (up) and turn-off (down) transients at 40A, 800Vdc.

The turn-on and turn-off losses at 800Vdc with 40A are also measured. It shows that switching loss is 0.63mJ for turn-on transient and 0.23mJ for turn-off transient.

It is also obvious that the ringing during switching in the DPT setup is significant, due to extra external long gate loop. To better evaluate switching perfomance, another DPT setup is employed as shown in Fig. 9. Coaxial connection are employed between driver and gate of SiC MOSFET to reduce gate loop parasitic inductance.

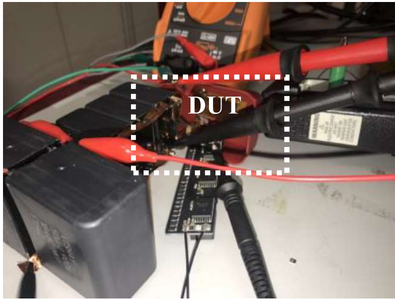


Fig. 9. DPT test setup with coaxial connection between gate and external driver.

An optimization approach is applied on the module to further improve switching performance. A 1000V ceramic decoupling capacitor is embedded in the 3D module, with one terminal connected with DC+ point at up-most substrate and the other connected wth DC- point at down-most substrate. The optimized 3D module with embedded decoupling capacitor is as shown in Fig. 10, with corresponding circuit schematic.

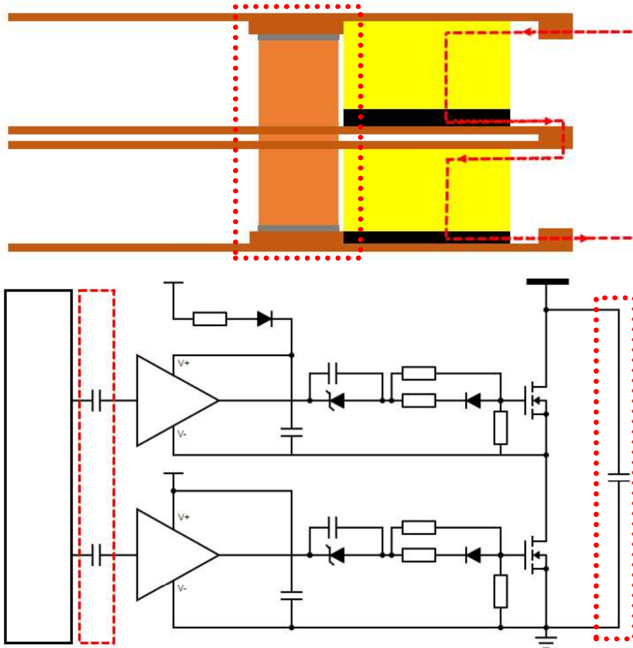


Fig. 10. Power stage integrated with embedded decoupling capacitor between DC+ and DC-.

The switching waveforms are as shown in Fig. 11 and Fig. 12. Fast turn-on and turn-off transients are implemented after the optimization with embedded ceramic decoupling capacitor at DC voltage up to 600V/40A and 700V/60A.

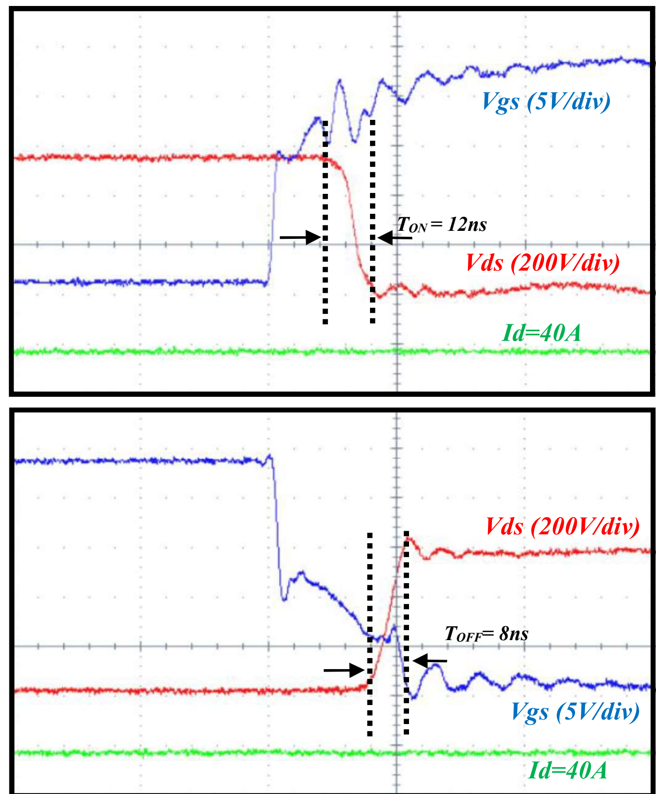


Fig. 10 Turn-on (up) and turn-off (down) transient at 40A, 600Vdc.

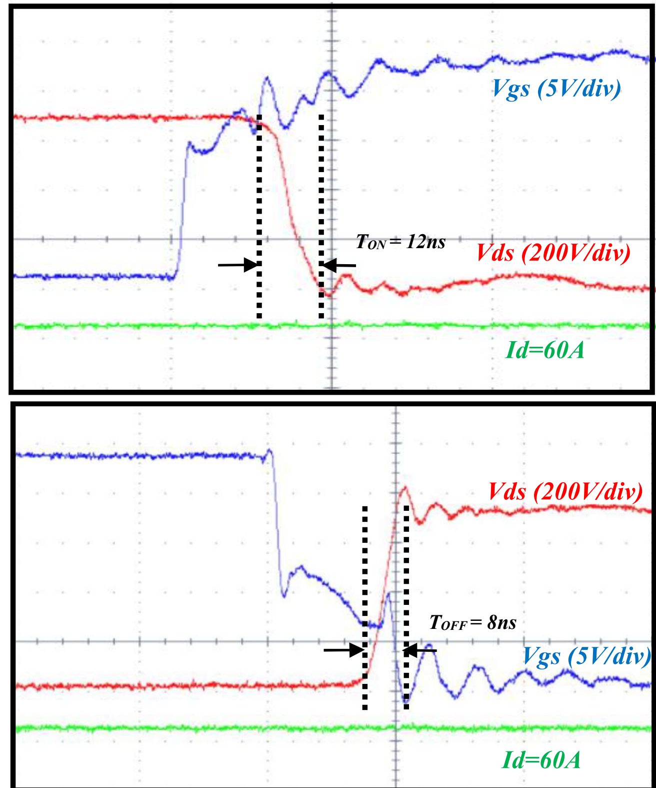


Fig. 11. Turn-on (up) and turn-off (down) transient at 60A, 700Vdc.

According to switching waveforms of 1.2kV SiC 3D half bridge IPM, it can be seen that through optimization, fast switching with limited voltage overshoot is achieved. For both cases, including 600V/40A and 700V/60A switching, turn-on transient is 12ns while turn-off one is 8ns. Corresponding dV/dt during turn-on at 600V is 50V/ns, and 75V/ns for turn-off. For 700V DC voltage, dV/dt during turn-on is 58.3V/ns, and 87.5V/ns for turn-off. The voltage overshoot in both cases are all limited to 40V, with implementation of optimization on the 3D 1.2kV SiC half bridge IPM.

V. THERMAL SIMULATIONS AND DISCUSSIONS

In the 1.2kV 3D half bridge SiC IPM, 80µm dielectric is applied as substrate instead of alumina in traditional DBC. The thermal conductivity of the ultra-thin dielectric is 8W/mK. Since SiC MOSFETs are stacked in the 3D packaging, for continues operation of the module during application, thermal design also need to be addressed carefully [13].

To evaluate thermal performance of the 1.2kV SiC 3D module, different models are applied for comparison, including planar module structure with DBC as substrates, planar module with ultra-thin flexible dielectric as substrate, and the designed IPM with stacked dies, as shown in Fig. 12.

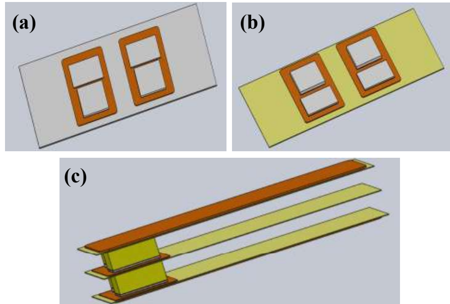


Fig. 12 Models for Thermal Performance Evaluation, (a) planar module with DBC substrate, (b) planar module with ultra-thin dielectric substrate, (c) 1.2kV 3D half bridge IPM.

All the substrate size is the same except thickness, the designed module is for 1200V applications, so DBC with 5mil Cu and 10mil ceramic is applied as shown in Fig. 12(a). The planar module with ultra-thin dielectric applied 80µm dielectric with 70µm Cu on one side and 210µm Cu on the backside, as shown in Fig. 12(b). As shown in Fig. 12(c), the substrate size is as same as model (b). In model (a), different ceramic material is applied on the DBC substrate, including alumina and aluminum nitride, and ultra-thin dielectric as comparison.

The same boundary conditions are applied on different models. In real case, module bottom is attached to baseplates and heatsinks. Considering maximum temperature on module bottom is around 80oC, and assuming different heat dissipation technologies can be substituted by convection coefficient applied on module bottom, it was found that 3000W/m2K can get temperature distribution close to real case, as shown in Fig.13. Simulation results shown that the 80µm dielectric provides same thermal performance compared with alumina based DBC substrate for 1.2kV applications.

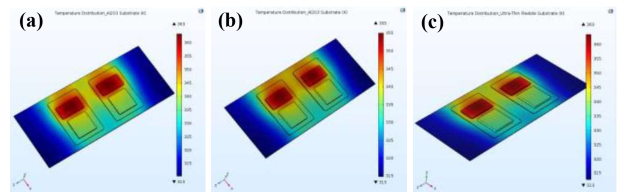


Fig. 13. Thermal Simulations on Planar modules with bottom convection coefficient 3000W/m^{2}K, (a) alumina DBC, (b) AlN DBC, (c) ultra-thin Dielectric.

Different convection coefficients, from 3000W/m2K to 6000W/m2K, are applied on both side of substrates on the 1.2kV SiC half bridge 3D IPM, as shown in Fig. 14.

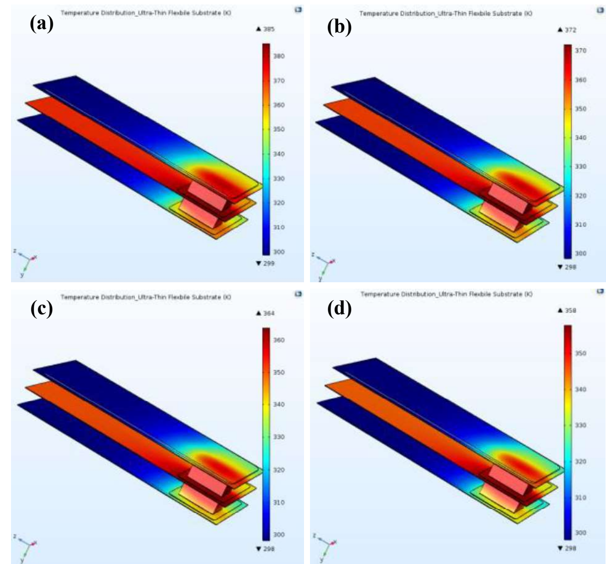


Fig. 14 Temperature Distribution on 1.2kV SiC half bridge 3D IPM with Different Bottom Convection Coefficient, (a) 3000W/m^{2}K, (b) 4000W/m^{2}K, (c) 5000W/m^{2}K, (d) 6000W/m^{2}K.

As bottom convection coefficient increases, junction temperature of the designed SiC PSiP half bridge IPM decreases. When convection coefficient is 3000W/m2K, the junction temperature is 385K, 22K higher than planar module with the same substrate due to thermal field overlapping from stacked highside and lowside SiC MOSFETs. When convection coefficient on both sides of the SiC IPM is doubled, the junction temperature can be even lower than that in planar modules with AlN DBC substrates. The proposed 3D 1.2kV SiC half bridge IPM, requires specifically designed heatsink to have comparable junction temperature with planar modules.

VI. CONCLUSIONS

The works propose design of a 1.2kV SiC half bridge Intelligent Power Module in 3D package. By interconnecting high side and low side SiC MOSFETs in the half bridge, the overall parasitic inductance in the power loop is limited to 1.3nH. Gate loop parasitics is also eliminated by flip-connecting SiC MOSFETs, so that the gate terminal can be directly connected with gate driver with minim distance. Characterizations in double pulse tests show that the switching losses of the designed power module in 3D package can 0.63mJ and 0.23mJ for turn-on and turn-off transients.

Further optimization is implemented by embedded decoupling ceramic capacitor in the 3D module. Through the optimization, switching transients for 600V/40A and 700V/60A are limited to 12ns turn-on and 8ns turn-off for SiC MOSFETs. Ringing on Vdc are significantly suppressed, with less than 40V voltage overshoot introduced during switching.

Thermal simulations are applied to address thermal performance evaluation of the designed IPM in 3D package, compared with traditional planar power module. Corresponding suggestions for specific thermal design of the 3D power module are provided. This work provides potential for further investigations on 3D power module concepts for ultra-high power density power conversion systems.

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