A Passivity-Based Decentralized Control Strategy for Current-Controlled Inverters in AC Microgrids

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***Abstract*—As a conventional stability analysis method of AC microgrid, the impedance based method needs a comprehensive impedance model of all the subsystems. It may fall short when the AC microgrid is interfaced by large number of converters with different parameters, or the microgrid has a time-varying structure, both of which would make the system modeling extremely complicated. This paper proposed a passivity margin criterion for AC microgrid, which decentralizes the stability target to each individual converter. The system will be stable with satisfactory margin as long as each converter is designed in accordance with the criterion, regardless of the system variations. A passivity realization approach for current-controlled LCL-type inverter is derived. The conclusions are verified on an OPAL-RT based Hardware-in-the-Loop platform.**

***Keywords*—AC microgrid; stability; impedance-based method; current-controlled inverter; passivity**

I. INTRODUCTION

Microgrid is a systematic organization of the distributed energy resources (DERs) and distributed energy storage devices (DESDs). LCL-type inverters are widely employed as the interface between DERs/DESDs and the grid [1]. A general configuration of AC microgrid is depicted in Fig.1. The converters in AC microgrid are either current-controlled or voltage controlled, which are also classified as grid feeding and grid-forming (supporting) converters, respectively [2]. The focus of this paper is the current-controlled LCL-type inverter in AC microgrid.

Among the many issues for AC microgrid, stability is one of the most important. There are mainly two types of instability issues in AC power electronics systems based on different timescales. One is induced by the slow power control loops [3], grid synchronization loops [4], or constant power loads [5], which often happens in very low frequency range with a typical timescale of tens or hundreds of milliseconds [6]. Another is often caused by the interactions among the multi-converter systems' fast inner current loops, higher order filters, or grid impedance [7]-[8], which often occurs in a higher frequency range with a typical timescale of less than a few milliseconds [6]. This paper focuses on the second type of instability issue.

Impedance-based method is a state-of-the-art method for stability analysis in AC microgrids. Only the terminal impedances of the two subsystems are required, and the stability analysis can be performed with the impedance ratio [8]-[9]. However, since a comprehensive model of the entire system is always required, the impedance ratio solution may fall short with the complex scenarios in AC microgrid. For instance, the converters may join or quit the microgrid in a plug-and-play manner due to the flexibility and uncertainty of DERs, which will result in a time-varying system structure [10]. In addition, when the AC microgrid is scaled up and involves lots of paralleled converters with different parameters, the modeling of the entire system is still possible but extremely complicated. Apart from the microgrid side problems, it is also hard to obtain the accurate information of the time-varying grid impedance, which further complicates the analysis.

A decentralized control to avoid the entire AC microgrid system modeling is required. Fortunately, the passivity concept offers the possibility to realize this target. Passive systems have two very useful characteristics: 1. a passive system is inherently stable; 2. the parallel and feedback interconnections of any passive systems are still passive [10]-[11]. Hence the passivity-based control (PBC) is highly applicable to the control of AC microgrids, which are basically interfaced by interconnected converters. As long as each converter is a passive subsystem, and the grid impedance is a RLC network (which is certainly passive), the entire AC microgrid will be stable.

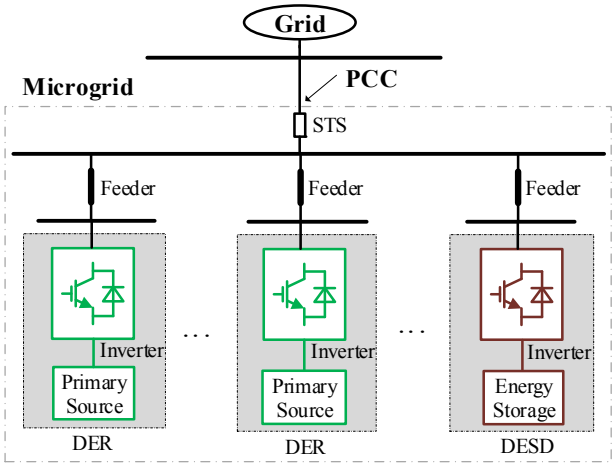


Fig.1. AC microgrid achiteture.

Based on the passivity concept, a passivity margin criterion is proposed in this paper. As a common design approach, it decentralizes the stability target to each individual converter in the microgrid and guarantees a satisfactory stability margin. Furthermore, an analogy between the passivity margin criterion and impedance-ratio criterion is derived.

In [10], a passivity realization method for DC microgrid based on voltage feed-forward is introduced. In [12], a capacitor voltage feedback based active damping is proposed to achieve passivity for converter-side current control of grid-tied inverters. The negative real part cancellation effect for paralleled converters with different parameters under certain conditions is studied in [13], but it can hardly be a general design guideline. In [14], a discrete derivative controller based passivity realization method is proposed. However, substantial mathematical analysis is required for the parameters tuning. Furthermore, none of [12]-[14] discussed the passivity margin.

Lead-lag controller and virtual resistor damping have been proposed to improve system stability in the literature [15]-[17]. Based on the passivity margin criterion, this paper proposed a novel passivity-oriented design approach with the lag controller to make the system passive and the virtual resistor damping to further improve the passivity margin, which is easy to understand and simple to implement. Finally, the theoretical analysis is verified on an OPAL-RT platform.

II. PASSIVITY MARGIN CRITERION

Passive systems are a class of dynamical systems in which the rate of the energy flows into the system is no less than the increase in storage. The difference between the energy supplied to the system and the stored energy is called the dissipated energy. The stability of a passive system is inherently guaranteed because the energy dissipation process always drives the system back to a point of equilibrium [11]. Another useful characteristic for passive systems is that the parallel and feedback interconnections of any passive systems are still passive [10]-[11]. This result is highly applicable to the control of microgrid, which are basically interfaced by interconnected power electronics converters. If each subsystem is designed to be passive, the passivity and stability of the entire system can be ensured. Furthermore, since the connection or disconnection of each converter won't change the passivity feature of the entire system, the system stability can be guaranteed under this condition, which is quite suitable for the plug-and-play requirement of the microgrid.

A circuit is passive if and only if its admittance Y seen from the terminal satisfies $\mathrm{Re}\{Y(j\omega)\} \geq 0$ for all ω, i.e., its phase $\arg\{Y(j\omega)\} \in [-90°, 90°]$ [11]. The passivity region for the admittance is depicted in Fig.2. Although stability is inherent in passive systems, the stability margin may not be acceptable. The LC resonant circuit is a straightforward example. It is a passive and stable system, but there is no passivity margin since it is an undamped system. From the frequency response point of view, the $Y(j\omega)$ of the circuit totally lies on the imaginary axis of the complex plane since it has a zero real part. If the admittance could be kept away from the boundary i.e., the imaginary axis, the stability margin of the system could be improved.

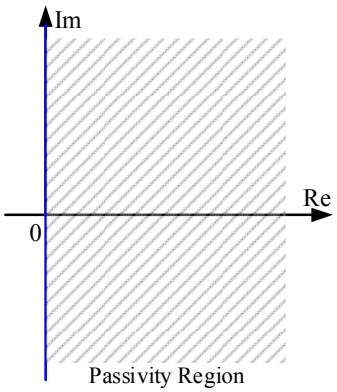


Fig.2. Passivity region for $Y(j\omega)$.

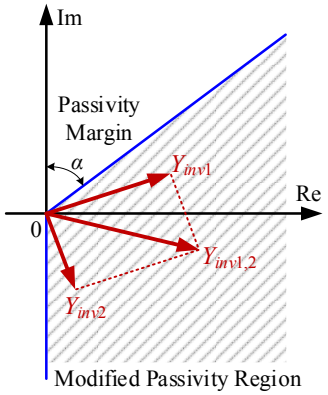


Fig.3. Modified passivity region for $Y(j\omega)$.

A. Passivity Margin Criterion

Based on this analysis, a modified passivity region is proposed for the AC microgrid, as shown in Fig.3. The upper part of the right half plane (RHP) is modified with a phase margin of α, while the lower part of RHP is unchanged. The explanation is provided as below. For LCL type grid-tied converter, the filter capacitor could be considered as a short circuit at high frequency range. Therefore, from a physical perspective the output admittance Y_{inv} is only the grid side inductor, which makes the admittance's phase −90°, and thus the lower part of the region is unalterable. This conclusion could also be drawn from the expression of Y_{inv}, which is provided in (5). When s is very large, $Y_{inv}(s) \approx 1/sL_2$.

If the admittances of all the converters in AC microgrid are designed to be within the proposed passivity region in Fig.3, a higher stability margin can be achieved. In addition, if each subsystem satisfies the passivity margin criterion, so does the entire interconnected system. Take parallel connection for example. If both of Y_{inv1} and Y_{inv2} lie within the modified passivity region, the combined admittance $Y_{inv1,2} = Y_{inv1} + Y_{inv2}$ will be between Y_{inv1} and Y_{inv2} according to the parallelogram law for complex number addition, hence it also lies within this region, as shown in Fig.3. The proof is similar for series connection [10].

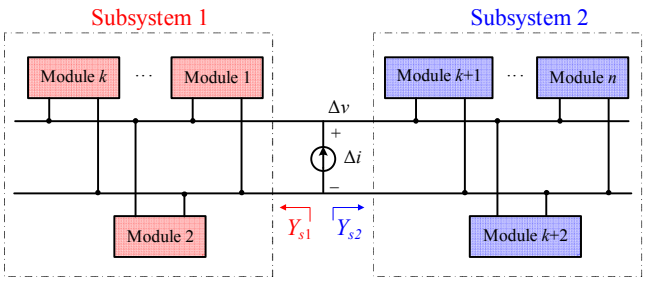


Fig.4. Impedance-ratio criterion for stability analysis of AC microgrid.

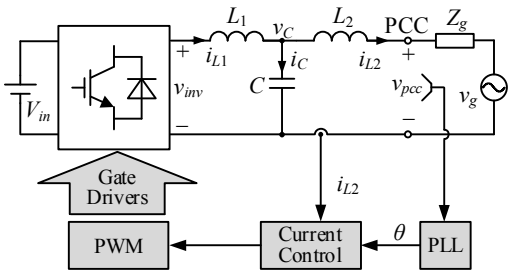


Fig.5. A current controlled grid-tied inverter system.

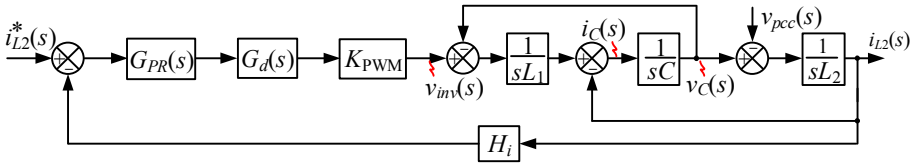


Fig.6. Grid-side current control diagram of a LCL-type current controlled grid-tied inverter.

B. *Analogy Between Passivity Margin Criterion and Impedance-Ratio Criterion*

Next, an analogy between the proposed passivity margin criterion and impedance-ratio criterion is provided. As shown in Fig.4, the AC microgrid is divided into 2 subsystems. Subsystem 1 contains all the Bus Current Controlled Converter (BCCC) in the microgrid, whereas subsystem 2 contains all the Bus Voltage Controlled Converters (BVCC). Note that a weak grid is a special case of BVCC [9]. It will be introduced in the later sections that the system under study in this paper is actually paralleled current controlled inverters (BCCC) interfaced with the non-ideal grid (BVCC).

$Y_{s1}(s)$ and $Y_{s2}(s)$ are the admittances of the two subsystems, and both $Y_{s1}(s)$ and $Y_{s2}(s)$ satisfy the passivity margin criterion, i.e. $\arg\{Y_{s1}(j\omega)\}, \arg\{Y_{s2}(j\omega)\} \in [-90°, 90°-\alpha]$. For a small-signal current injection Δi at the point of coupling, the consequent voltage ripple Δv can be obtained as (1), which indicates the relationship between each admittance and the impedance ratio.

$$\frac{\Delta v(s)}{\Delta i(s)} = \frac{1}{Y_{s1}(s)+Y_{s2}(s)} = \frac{Z_{s2}(s)}{1+Z_{s2}(s)/Z_{s1}(s)} \tag{1}$$

where $Z_{s1}(s)$ and $Z_{s2}(s)$ are the corresponding impedance of $Y_{s1}(s)$ and $Y_{s2}(s)$.

The impedance ratio $Z_{s2}(s)/Z_{s1}(s)$ could be considered as the equivalent loop gain of the system. Therefore, the system stability can be determined by studying this impedance ratio. The sufficient and necessary condition for the system stability is that this impedance ratio satisfies the Nyquist stability criterion [9]. The phase of $Z_{s2}(s)/Z_{s1}(s)$ can be derived in (2).

$$\begin{aligned}\arg\{Z_{s2}(s)/Z_{s1}(s)\} &= \arg\{Z_{s2}(s)\} - \arg\{Z_{s1}(s)\} \\ &= \arg\{1/Y_{s2}(s)\} - \arg\{1/Y_{s1}(s)\} \\ &= \arg\{Y_{s1}(s)\} - \arg\{Y_{s2}(s)\}\end{aligned} \tag{2}$$

Recall that $\arg\{Y_{s1}(j\omega)\}, \arg\{Y_{s2}(j\omega)\} \in [-90°, 90°-\alpha]$, hence $\arg\{Z_{s2}(s)/Z_{s1}(s)\}$ should be $[-180°+\alpha, 180°-\alpha]$, this is exactly the impedance ratio criterion as derived in [8]-[9]. Apparently, the passivity margin criterion is the sufficient yet unnecessary condition for impedance-ratio criterion. The main difference is that passivity margin criterion is a requirement for the admittance of each individual converter, whereas the impedance-ratio criterion involves two subsystems. A major disadvantage of passivity-based method is that it will leads to a more conservative controller design. So there is a trade-off between the stability objective and the conservativeness of the controller design.

III. PASSIVITY REALIZATION FOR AC MICROGRID

Based on the passivity design guideline described in Section II, a passivity realization approach for LCL-type grid-tied converters is introduced here.

A. *System Modeling*

A current-controlled grid-tied inverter system is depicted in Fig.5. The converter could either be a single-phase inverter, or a balanced three-phase inverter under the stationary $\alpha-\beta$ frame. The grid-side current control diagram are provided in Fig.6. As mentioned in Section I, this paper is focused on the higher frequency stability issues. And the PLL bandwidth used in this paper is designed to be low enough that no low-frequency oscillation will not occur [4]. $G_{PR}(s)$ is the current controller, as provided in (3). $G_d(s)$ is the digital control delay, it is normally modeled as a $1.5T_s$ delay [17], where T_s is the sampling period. K_{PWM} is the transfer function of the PWM converter,

and H_i is the grid-side current sensor gain.

$$G_{PR}(s) = k_p + \frac{2k_r\omega_i s}{s^2 + 2\omega_i s + \omega_o^2} \tag{3}$$

$$G_d(s) = e^{-1.5sT_s} \tag{4}$$

The impedance-based representation of the inverter-grid system is depicted in Fig.7. The expression of the inverter admittance can be derived as in (5).

$$Y_{inv}(s) = \frac{s^2 L_1 C_f + 1}{s^3 L_1 L_2 C_f + s(L_1 + L_2) + G_{PR}(s) K_{\mathrm{PWM}} G_d(s) H_i} \tag{5}$$

A 6kW DER inverter is taken as example here, of which the parameters are provided in Table I & II in the Appendix.

The Bode plot of $Y_{inv}(s)$ is shown in Fig.8. $Y_{inv}(s)$ first exhibits an inductive feature, then there is a phase jump from approximately −90° to 90° at fundamental frequency f_o = 60Hz, which is induced by the PR controller. Recalling from the last section, the phase of $Y_{inv}(s)$ should be kept away from 90° for satisfactory passivity margin. However, PR controller is introduced to achieve zero steady-state error for fundamental component, and normally it will not destabilize the system. Furthermore, only the high frequency harmonic stability issue is of interest in this paper as mentioned before, hence the phase jump at f_o does not matter. After f_o, the phase of $Y_{inv}(s)$ decreases until at f_{LC}, which is the resonant frequency of L_1 and C_f, another 180° phase jump occurs due to the L_1C_f resonance. Due to the digital control delay, the phase of $Y_{inv}(s)$ will be greater than 90°, which suggests that it is non-passive.

An analytical expression of the non-passive region for $Y_{inv}(s)$ can be obtained from (5). The R part of the PR controller $G_{PR}(s)$ is designed for zero steady-state error at fundamental frequency, therefore it has little influence at higher frequency range [14]. To simplify the calculation, use k_p instead of the expression in (3). By substituting s with $j\omega$, the real part of $Y_{inv}(s)$ can be derived as

$$\begin{aligned} &\mathrm{Re}\{Y_{inv}(j\omega)\} = \frac{(-\omega^2 L_1 C_f + 1) k_p K_{\mathrm{PWM}} H_i \cos(1.5\omega T_s)}{A^2 + B^2} \\ &A = k_p K_{\mathrm{PWM}} H_i \cos(1.5\omega T_s) \\ &B = \omega^3 L_1 L_2 C_f - \omega(L_1 + L_2) + k_p K_{\mathrm{PWM}} H_i \sin(1.5\omega T_s) \end{aligned} \tag{6}$$

The expression of $\mathrm{Re}\{Y_{inv}(j\omega)\}$ suggests that the negative real part is determined by both the digital delay and the L_1C_f resonance. As a general conclusion, the system is non-passive between f_{LC} and $f_s/6$, where f_s is the sampling frequency. Fig.8 is an example with f_{LC} below $f_s/6$.

B. Passvity-Based Controller Design

To get rid of the non-passivity region, an intuitive idea is to

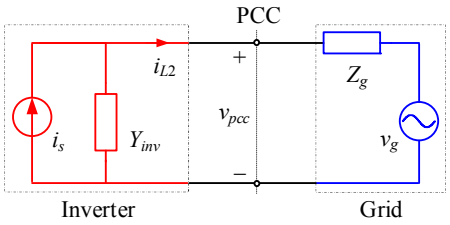


Fig.7. Impedance-based model of the grid-tied inverter system.

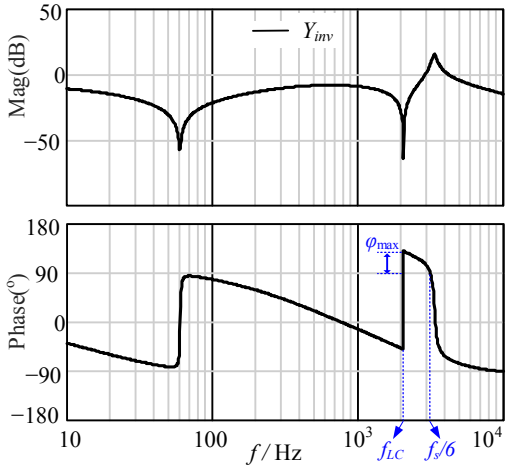


Fig.8. The admittance characteristic of a typical current controlled inverter.

make a phase drop of $Y_{inv}(s)$ between f_{LC} and $f_s/6$. This could be achieved by integrating a lag element $G_{lag}(s)$ in series with the PR controller. The implementation is very easy in the DSP, with no requirement for additional sensors. The expression of a first-order lag-controller is given as

$$G_{lag}(s) = k_{lag} \frac{1 + \tau_1 s}{1 + \alpha\tau_1 s} \tag{7}$$

where k_{lag}, τ_1, α are the parameters for the lag compensator. Note that for a lag compensator, $\alpha > 1$. The maximum phase lag $\varphi_{\max}$ that can be realized, and the frequency at which $\varphi_{\max}$ occurs are given by

$$\sin\varphi_{\max} = \frac{\alpha - 1}{\alpha + 1}, \quad f_{\max} = \frac{1}{2\pi\tau_1\sqrt{\alpha}} \tag{8}$$

To eliminate the non-passivity region, i.e., to limit the phase-frequency curve of $Y_{inv}(s)$ to [−90°, 90°], a good choice of $f_{\max}$ would be $f_{\max} = f_{LC}$, and $\varphi_{\max}$ is designed as the phase drop $Y_{inv}(s)$ required to be 90° at f_{LC}. In this way, τ_1, α can be determined. The phase drop should not be too large, because an excessive phase drop would make the lower part of $Y_{inv}(s)$ non-passive due to the 180° phase jump at f_{LC}.

$$Y_{inv\_lag}(s)=\frac{s^2L_1C_f+1}{s^3L_1L_2C_f+s(L_1+L_2)+G_{PR}(s)G_{lag}(s)K_{\mathrm{PWM}}G_d(s)H_i} \tag{9}$$

$$Y_{inv\_cmb}(s)=\frac{s^2L_1C_f+sC_fH_{ic}G_{lead}(s)K_{\mathrm{PWM}}G_d(s)+1}{s^3L_1L_2C_f+s^2L_2C_fH_{ic}G_{lead}(s)K_{\mathrm{PWM}}G_d(s)+s(L_1+L_2)+G_{PR}(s)G_{lag}(s)K_{\mathrm{PWM}}G_d(s)H_i} \tag{10}$$

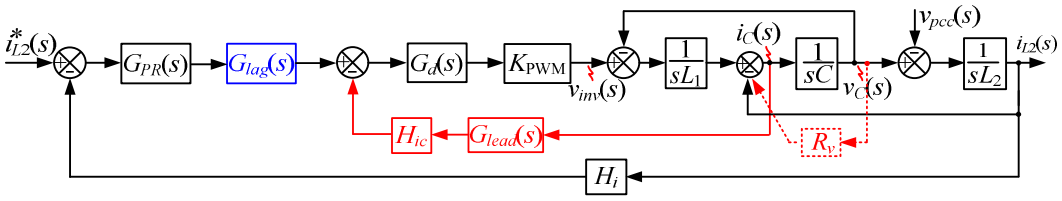


Fig.9. Control diagram with passivity-based controllers.

So far the design of k_{lag} has not been discussed. Although the required compensation for eliminating the non-passivity region of $Y_{inv}(s)$ is assumed to be an ideal phase drop, the lag-controller also inevitably introduces a magnitude attenuation at higher frequency range, which would greatly decrease the bandwidth of the current loop. Hence, $k_{lag} > 1$ is required to compensate this magnitude attenuation. On the other side, due to the phase drop introduced by $G_{lag}(s)$, this bandwidth also needs to decrease a certain extent to ensure enough phase margin for the current loop gain. The selection of k_{lag} is a trade-off between stability and dynamic performance.

For the 6kW DER inverter example, the lag-controller parameters are designed as $\alpha = 4.0$, $\tau_1 = 3.95\times10^{-5}$, $k_{lag} = 1.2$, which is provided in Table I. The expression of the lag-controller compensated inverter admittance $Y_{inv\_lag}(s)$ is given in (9). And its Bode plot is depicted Fig.10. The phase of $Y_{inv\_lag}(s)$ is limited to [−90°, 90°] with the lag-controller.

Now a passive inverter output admittance is obtained. However, since the L_1C_f resonance still exists, there will always be a 180° phase jump at f_{LC}, which suggest that it will never satisfy the passivity margin criterion. A straightforward idea is to damp the L_1C_f resonance.

If a virtual resistor R_v could be introduced in parallel with the capacitor, the L_1C_f resonance could be damped. Fig.9 depicts the realization of the virtual resistor by sampling the capacitor current and feeding it back to the lag controller output via a gain of H_{ic}. The expression of the inverter output admittance could be derived as $Y_{inv\_cmb}(s)$ in (10). Note that due to the delay, the intended virtual resistor is actually a frequency-dependent impedance, as given in (11), which has a negative resistance beyond $f_s/6$ and could destabilize the system [17].

$$R_v(s)=\frac{L_1}{C_fK_{\mathrm{PWM}}H_{ic}}e^{1.5sT_s} \tag{11}$$

To compensate the delay effect, a lead-controller $G_{lead}(s)$ is introduced to extend the positive resistance range.

$$G_{lead}(s)=k_{lead}\frac{1+\beta\tau_2 s}{1+\tau_2 s} \tag{12}$$

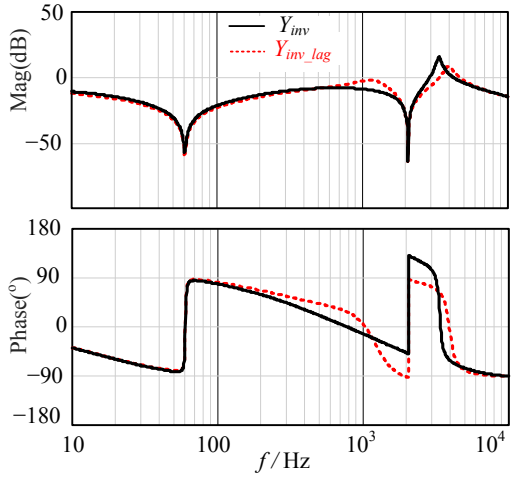


Fig.10. $Y_{inv}(s)$ with lag controller.

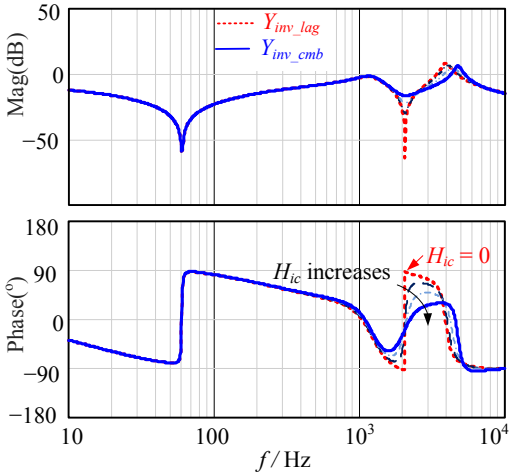


Fig.11. $Y_{inv}(s)$ with lag controller and virtual resistor.

The lead-controller has similar feature as the lag-controller. This time let $f_{max} = f_s/6$, and φ_{max} should compensate the phase delay caused by $G_d(s)$ at $f_s/6$. Consequently, the value of β and τ_2 can be determined. The tuning of k_{lead} and H_{ic} can be discussed as a whole. Without delay, the value of H_{ic} is inversely proportional to R_v [17]. Larger H_{ic} implies better damping effect, as shown in Fig.11. However, since $G_{lead}(s)$ can only cancel the digital delay up to $f_s/6$, an excessive H_{ic} would make the system non-passive at higher frequency. Using the H_{ic} and $G_{lead}(s)$ parameters provided in Table II, the Bode plot of Y_{inv_cmb} satisfies the passivity margin criterion with a phase margin of about 50°, as shown in Fig.11.

IV. Real-Time Simulation Verification

The OPAL-RT based hardware-in-the-loop (HIL) method has been proved to be a powerful tool for the verification of complex and large scale power electronics systems [18]-[20]. The HIL platform is depicted in Fig.12. The AC microgrid is modeled in the real-time simulator (OP5607), and the control algorithms are implemented in the TI TMS320F28377S DSPs. The Analog Out are the sampled electrical signals from the inverters, which are sent to the DSPs on the interface board to perform the control algorithms. Accordingly, the PWMs are generated and sent back to the inverters in the simulator. The electrical waveforms are monitored through the oscilloscope.

The AC microgrid test system is given in Fig.13, which consists of two 6kW DER inverters and one 3kW DESD inverters. The parameters of the inverters are provided in Table I in the Appendix. Each of them are connected with the PCC through feeders. The grid impedance is modeled at the PCC to describe the non-ideal grid condition. Generally, the grid and feeder impedance contain both inductance and resistance [7]. However, pure inductance L_g and L_{li} (i=1, 2, 3) are considered for a worst case scenario, since the damping effect of the resistances can help stabilizing the system.

The passivity-based controllers for the DER inverters and DESD inverter are designed according to the guideline proposed in this paper, as given in Table II in the Appendix.

Fig.14 shows the waveforms of grid injection current i_{L2} and PCC voltage v_{pcc} for a single inverter case, all in per-unit, where the base values are V_b= 110V, P_b= 6kW, I_b= P_b/V_b. As shown in Fig.14(a), before the lag-controller switches in, severe oscillation occurs. The lag-controller stabilizes the system. However, the oscillation decay takes more than half fundamental period. In Fig.14(b), with an additional active damping, the oscillation decays a lot faster. Thereby, system stability is further improved.

Fig.15 shows the grid current i_g and PCC voltage v_{pcc} of AC microgrid. As shown in Fig.15(a), when a DER and a DESD converter switch to the combined PBC, the oscillation can be attenuated noticeably. Nevertheless, the system is still unstable. Under this condition, although two of the converters are passive subsystems, the entire system is still non-passive. As shown in Fig.15(b), when all of the three converters are implemented with PBC, the oscillation decays rapidly. The results prove that the passivity margin criterion is an effective guideline for improving AC microgrid stability.

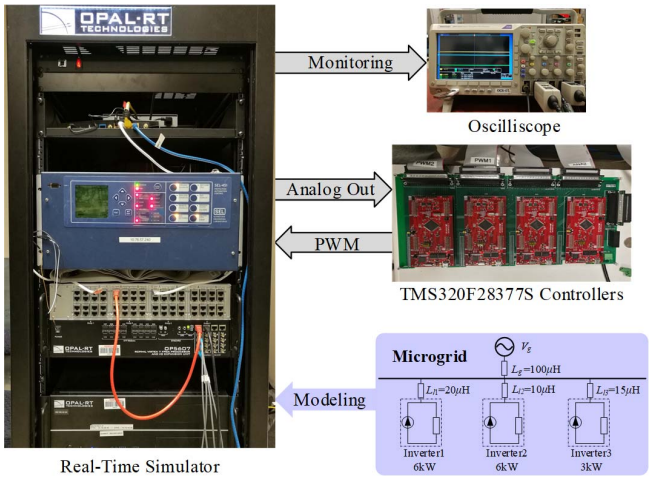


Fig.12. Hardware-in-the-loop system.

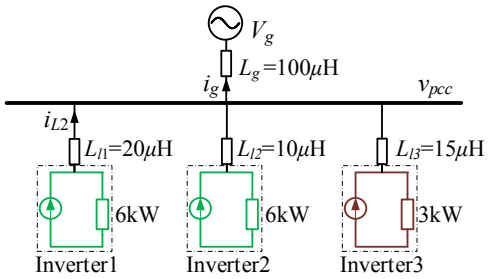


Fig.13. AC microgrid test system.

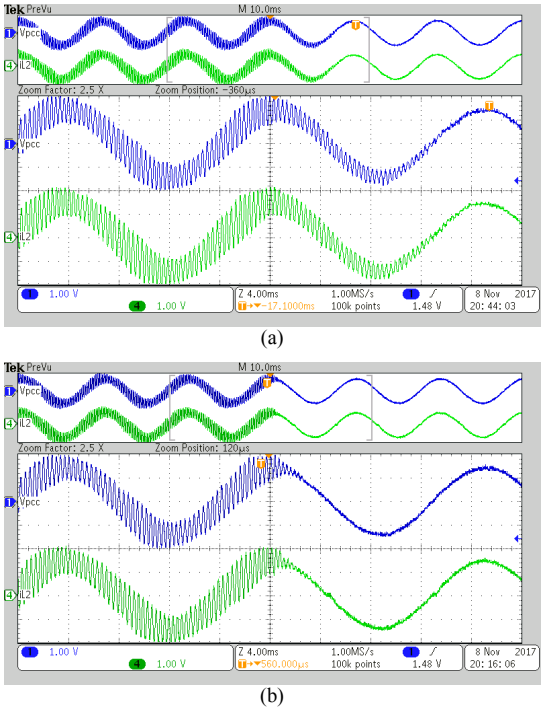
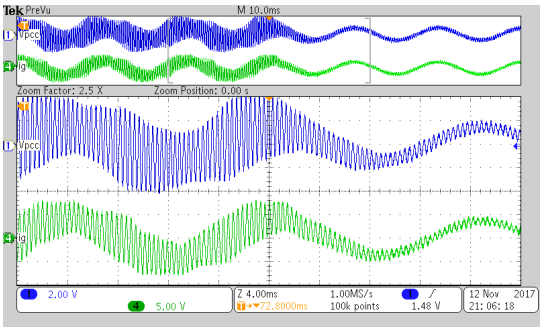
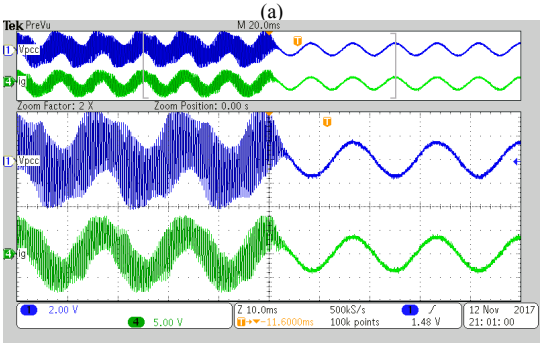


Fig.14. Single grid-tied inverter case. (a) The inverter switches to lag controller. (b) The inverters switches to lag controller combined with virtual resistor.



(a)



(b)

Fig.15. Microgrid case. (a) Two of the inverters are switched to PBC. (b) Three inverters are switched to PBC.

CONCLUSION

The passivity concept offers the possibility to localize the stability target of the AC microgrid to each individual converter. In this way, modeling of the entire system can be avoided and the stability design can be simplified. A passivity margin criterion for improving the stability of AC microgrid is proposed and verified in the paper. A passivity-oriented design approach for the lead-lag controller and virtual resistor active damping is provided. It should be noted that passivity is a sufficient yet not necessary condition for stability. Therefore there is a trade-off between a more stable system and less conservative controller design.

APPENDIX

TABLE I. SYSTEM PARAMETERS

Parameter		Symbol	Value
Input voltage		V_{in}	200V
Grid voltage (RMS)		V_g	110V
Current sensor gain		H_i	0.015
Fundamental frequency		f_o	60Hz
Sampling frequency		f_s	20kHz
Switching frequency		f_{sw}	10kHz
PWM converter transfer fucntion		K_{PWM}	200
DER Inverters	Power rating	P_o	6kW
	Converter-side inductor	L_1	300μH
	Filter capacitor	C_f	20μF
	Grid-side inductor	L_2	100μH
DESD Inverter	Power rating	P_o	3kW
	Converter-side inductor	L_1	400μH
	Filter capacitor	C_f	12μF
	Grid-side inductor	L_2	150μH

TABLE II. PARAMETERS OF THE CONTROLLERS

Controllers	G_{PR}	G_{lag}	H_{ic}, G_{lead}
DER Inverters	k_p=0.9, k_r=250	τ_1=3.95×10^{-5}, k_{lag}=1.2, α=4.0	H_{ic}=0.005, τ_2=3×10^{-5}, k_{lead}=0.4, β=8
DESD Inverter	k_p=1.33, k_r=316	τ_1=3.5×10^{-5}, k_{lag}=1.1, α=2.3	H_{ic}=0.008, τ_2=2.8×10^{-5}, k_{lead}=0.4, β=6

ACKNOWLEDGMENT

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000666. The views and opinions of authors expressed herein do not necessarily state or reflect those of the US Government or any agency thereof.

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