A High-Voltage-Gain DC-DC Converter for Powering a Multi-mode Monopropellant-Electrospray Propulsion System in Satellites

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***Abstract* - This paper introduces a high-voltage-gain dc-dc converter designed to act as a power processing unit for a multi-mode monopropellant-electrospray propulsion system used in satellites. The high-voltage-gain converter is capable of offering a voltage gain ranging from 200 to 350. This converter is made up of two stages: 1). A two-phase interleaved boost stage on the input side and 2). A Cockcroft-Walton voltage multiplier on the output side. This converter is employed to boost a 15 V battery voltage to 3400 V required for operating the thruster in electrical mode. The theoretical analysis and design procedure of the converter is discussed in detail. Hardware test results supporting the converter operation and analysis are also provided.**

Keywords – high-voltage-gain dc-dc converter, multi-mode monopropellant-electrospray propulsion system, power processing unit, Cockcroft Walton voltage multiplier, modified square wave

I. INTRODUCTION

A Multi-mode Monopropellant-Electrospray Propulsion System (MMEPS) is a single propulsion thruster operating in both catalytic chemical mode and electrospray electric mode, while utilizing a same ionic propellant. Therefore, this single propulsion system provides for more mission design space within the satellite. The Missouri S&T Satellite Research Team is currently building a microsatellite which, if down selected by the Air Force Research Laboratory's final selection review panel, will be launched to low Earth orbit. The satellite's payload is an MMEPS, which uses an ionic liquid as the propellant to generate both chemical and electrical modes of propulsion. The electric propulsion mode requires a constant voltage of 3400 V at 10 W. However, the satellite's current power boards generate a maximum of 12 V. Therefore, an intermediary Power Processing Unit (PPU) must be designed to achieve the desired voltage for the thruster.

Limited energy available in the battery system and the form factor requirement of the PPU make efficiency and size to be the most critical factors while constructing it. With the battery voltage in the satellite varying anywhere between 9.5 V to 17 V, the PPU should be capable of regulating the output at a constant voltage of 3400 V to power the electrical mode. These factors demand a PPU that employs a power electronic converter to achieve the desired output voltage of 3400 V. Many high-voltage-gain dc-dc converters have been proposed for integration of renewable energy sources over the last decade [1-7]. These converters, however, would barely be able to meet the voltage gain requirement of the PPU. Most of these converters make use of a two-phase interleaved (TPI) boost stage in series with a voltage multiplier (VM) circuit to achieve high voltage gain. Dickson charge pump [1], modified Dickson charge pump [2], Cockcroft Walton (CW) [3], and a voltage quadrupler [4], are some of the common voltage multiplier circuits that were used. Among these, the Cockcroft Walton VM stands out as it offers a higher voltage multiplication factor for a given component count.

Using a regular TPI boost in series with an n-stage CW voltage multiplier to achieve the voltage gain does not go well with the efficiency requirement, due to the increased number of diodes, nor with the size requirement, due to increased capacitor count. This calls for an improvement to the TPI boost stage to increase the voltage gain. In [5-7], coupled inductors have been used in the TPI boost stage to achieve further higher voltage gains. A combination of coupled inductor based TPI boost stage along with a CW voltage multiplier would make the best combination to achieve the desired gain. In this paper, a high-voltage-gain dc-dc converter is proposed using this combination to obtain a voltage gain ranging from 200 to 350 making it a suitable candidate for the MMEPS PPU. The following parts of the paper discuss the topology, analyze its voltage gain, and calculate the component stresses. Experimental results are provided to support the theoretical claims.

II. TOPOLOGY

The proposed topology is constructed using a two-phase interleaved (TPI) boost stage connected in series with a Cockcroft Walton (CW) voltage multiplier circuit (see Fig. 1). The TPI boost stage utilizes a three-winding coupled inductor to boost the 15 V input to a Modified Square Wave (MSW) voltage between terminals A and B. It does so by switching both its switches S_1 and S_2 at duty cycles d_1 and d_2 such that one of them is ON at any point of time (see Fig. 2). To achieve a symmetric operation, both S_1 and S_2 are switched at equal duty cycle 'd' while being 180º out of phase from each other. The MSW voltage output of the TPI boost stage (V_{AB}) is

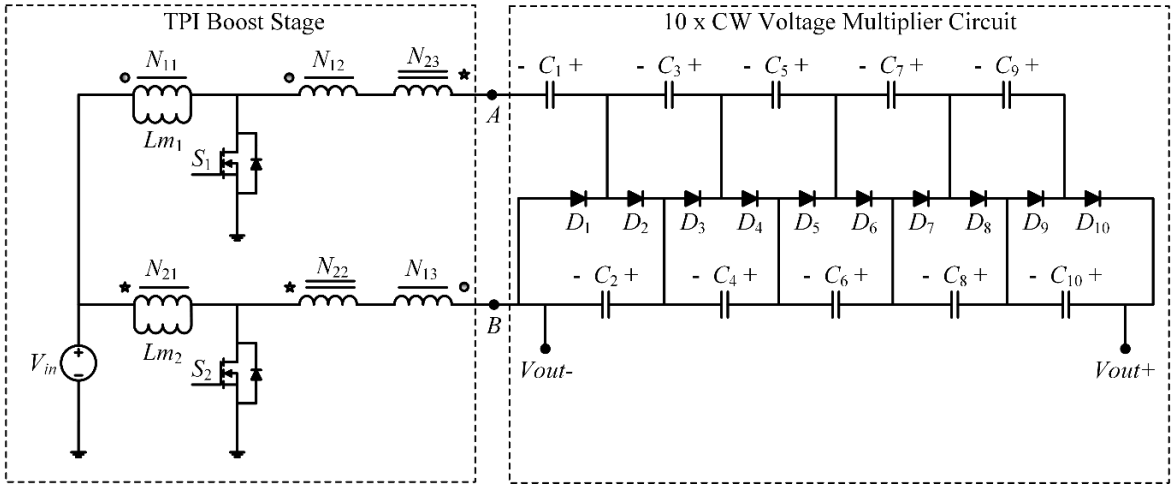

Fig. 1. Two stages of the proposed high-voltage-gain dc-dc converter

rectified and further boosted by the 10x CW voltage multiplier circuit to provide 3400 V at its output terminals.

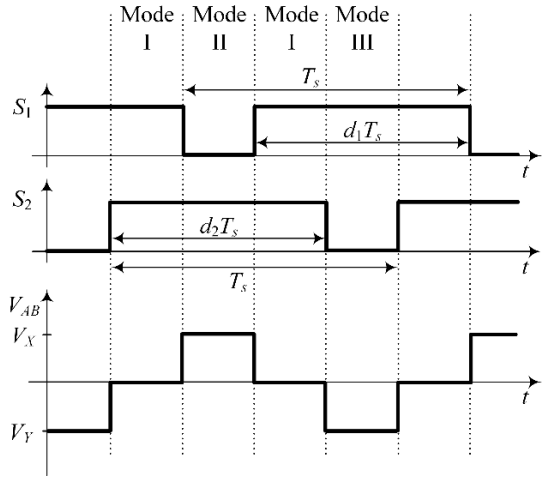

Fig. 2. Switching signals and MSW voltage output of the TPI boost stage

In mode-I of operation, both switches S_1 and S_2 are ON and the magnetizing inductances L_{m1} and L_{m2} of the coupled inductors charge linearly. In mode-II of operation, switch S_1 is OFF and S_2 is ON. The energy stored in the magnetizing inductance L_{m1} discharges to charge the even numbered capacitors while discharging the odd number capacitors. In mode-III of operation, switch S_1 is ON and S_2 is OFF. The energy stored in the magnetizing inductance L_{m2} discharges to charge the odd numbered capacitors while discharging the even number capacitors.

The theoretical analysis that follows, is based on the assumption that the magnetizing inductances of the TPI boost stage are selected to operate in continuous conduction mode (CCM). Using volt-second balance on the magnetizing inductances L_{m1} and L_{m2}, the peak voltages V_X and V_Y of the MSW voltage V_{AB} (see Fig. 2) are calculated as

$$V_X = V_Y = (2n+1)\frac{V_{in}}{1-d} \tag{1}$$

where, V_{in} is the input voltage. 'n' is the turns ratio of the coupled inductors and is calculated as

$$n = \frac{N_{12}}{N_{11}} = \frac{N_{13}}{N_{11}} = \frac{N_{22}}{N_{21}} = \frac{N_{23}}{N_{21}} \tag{2}$$

The output voltage of a 10x CW voltage multiplier can be calculated as

$$V_{Cout} = 5(V_X + V_Y) \tag{3}$$

From (1), (2), and (3), the voltage gain of the proposed PPU is derived to be

$$\frac{V_{out}}{V_{in}} = \frac{10(2n+1)}{1-d} \tag{4}$$

Despite having a high voltage at the output, the voltage stress experienced by the switches is low. It can be calculated using (5). The voltage stress on the 10x CW voltage multiplier circuit capacitors is calculated using (6). The peak voltage stress on diodes D_1 to D_{10} is given by (7).

$$V_{S1} = V_{S2} = \frac{V_{in}}{1-d} \tag{5}$$

$$V_{C1} = \frac{7 \times V_{in}}{1-d};$$

$$V_{C2} = V_{C3} = V_{C4} = V_{C5} = V_{C6} = V_{C7} = V_{C8} = V_{C9} = V_{C10} = \frac{14 \times V_{in}}{1-d}; \tag{6}$$

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = V_{D6} = V_{D7} = V_{D8} = V_{D9} = V_{D10} = \frac{14 \times V_{in}}{1-d}; \tag{7}$$

To achieve the desired voltage gain, the turn's ratio of the coupled inductors is selected to be 1:3:3. Therefore, n is 3. With switches S_1 and S_2 operating at a duty cycle of 69.12%, the 15 V nominal input of the battery system is boosted to 3400 V. The voltage stress on the switches is 48.57 V and the capacitor voltages of C_1, C_2-C_{10} are 340 V and 680 V, respectively.

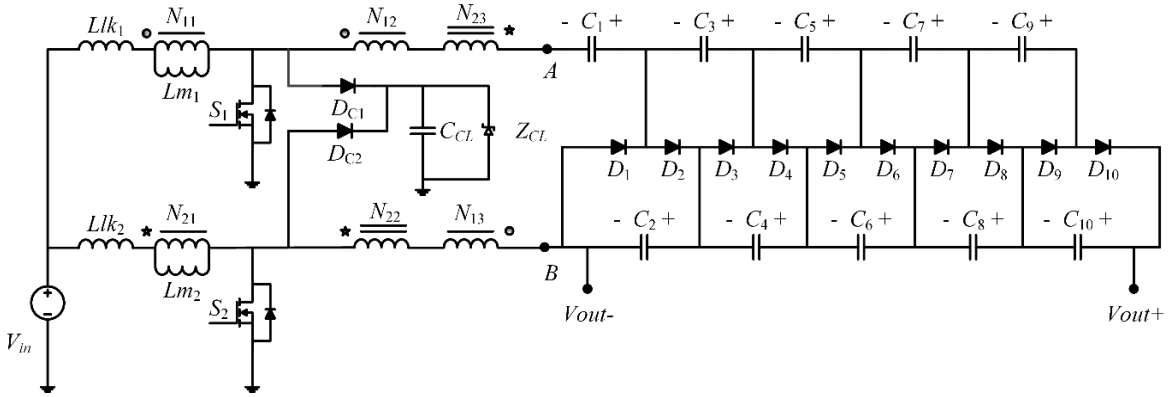

Fig. 3. Practical PPU topology with passive zener clamp circuit

A practical PPU will fall short of the ideal voltage gain derived above due to 1). Leakage inductances (L_{lk1}, L_{lk2}) and equivalent series resistance (*ESR*) of the coupled inductors, 2) forward voltage drop on the diodes, 3) R_{dsON}, parasitic capacitances of MOSFETs, and 4) *ESR* of the VM stage capacitors. The leakage inductance of the coupled inductors plays a significant part in this deviation compared to other non-idealities. As the voltage gain of the practical PPU is complex to derive, a simulation model of the PPU developed in PLECS was used to determine the duty cycle requirements. The leakage inductance also causes voltage spikes on the switches leading to their failure. Hence, a clamping circuit is required to prevent any switch failure. As the power rating of the PPU is low, a passive clamp circuit is a simple, reliable, and cost effective solution. The practical PPU topology with a passive zener clamp is shown in Fig. 3. The clamping circuit is implemented using two diodes, a clamp capacitor and a zener diode. As the zener diode limits the voltage across the switch, its rating should be selected appropriately to be below the maximum switch voltage rating.

III. Experimental Results

A hardware prototype of the PPU was built for the specifications listed in Table I. Figs. 4 and 5 show the top and bottom view of the PPU. The different sub-circuits within the PPU, i.e., the zener clamp circuit and 10xCockcroft Walton voltage multiplier are highlighted in these figures. Also, the coupled inductors, Si MOSFETs and gate driver (MIC4424) are highlighted. The hardware implementation of the PPU meets the desired form factor requirements, i.e., a board dimension of 96 mm x 90 mm.

Table I: PPU specifications and component ratings

Parameter	Symbol	Value
Input voltage	V_{in}	15 V
Output voltage	V_{out}	3400 V
Output power	P_{out}	10 W
Switching frequency	f_{SW}	100 kHz
Magnetizing inductance	L_{m1}, L_{m2}	1.2 mH
VM capacitors	V_{c1}, $V_{c2\text{-}10}$	0.94 uF, 1 kV
MOSFET	S_1, S_2	100 V, 0.54 Ω
Zener – Clamp circuit	Z_{CL}	60 V

For the coupled inductors, an ETD 34/17/11 ferrite magnetic core is used. An air gap of 0.2 mm is used to improve the energy storing ability in the coupled inductor core. With 50 turns on the primary and an A_L value of 0.482 uH/turns^2, the magnetizing inductance of coupled inductor is obtained to be 1.2 mH. This value of magnetizing inductance is high enough to have the converter operating in CCM. As the selected turns ratio is 1:3:3, the no. of turns on the secondary and tertiary windings are 150. *Vishay IRF510* Si MOSFETs have been used for switches S_1 and S_2. *ON Semiconductor's MUR1100* is used for all diodes in the 10xCW voltage multiplier circuit. Two 0.47uF ceramic capacitors rated at 1100V are used in parallel for each of the VM capacitors.

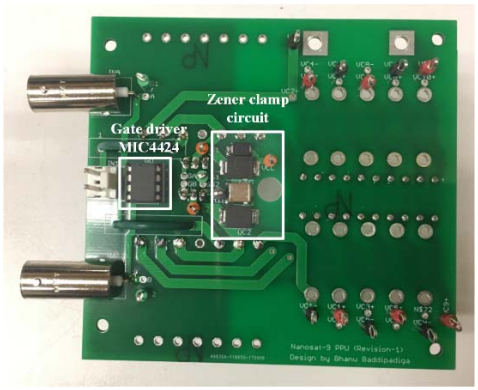

Fig. 4. Hardware prototype – top side

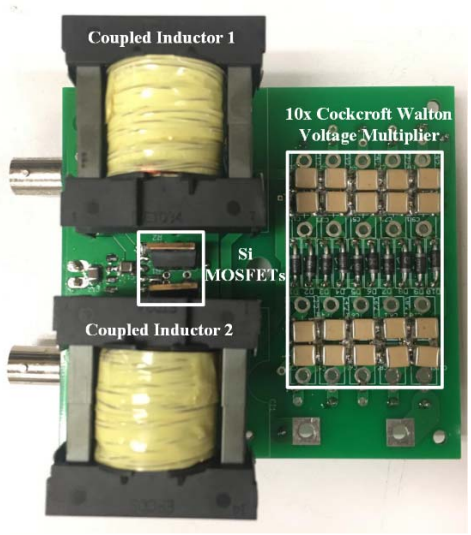

Fig. 5. Hardware prototype – bottom side

The experimental waveforms observed on the oscilloscope are shown in Figs 6, 7, 8, and 9. In these experimental waveforms, switching signals G_{S1} and G_{S2} are included in order to observe the variations in the observed parameters during the changes in modes of operation. Fig.6 shows the gate voltages of switches S_1 and S_2 at 66.4% duty cycle (*channels* 1 and 2). The peak voltage of the switches is below 60 V (*channels* 3 and 4), i.e., the zener diode Z_{CL} voltage. However, the steady state value is observed to be 44.8 V, which is equivalent to the theoretical value calculated using (5). The voltage observed on capacitors C_1 and C_4 are 338.4 V and 685.2 V, respectively, as shown in Fig. 7 (*channels* 4 and 3, respectively). In Fig. 8, it can be seen that the output voltage is 3400 V (*channel* 3) The input current is continuous and is measured to be 0.81 A (*channel* 4). The input current ripple is small due to the ripple cancellation caused by the phase shifted operation of switches S_1 and S_2 in the TPI boost stage. The clamp capacitor voltage can be seen to be 60 V in Fig. 9 (*channel* 4) as the zener diode used in the clamp circuit is rated at 60 V. The experimental waveforms validate the theoretical analysis of the proposed converter.

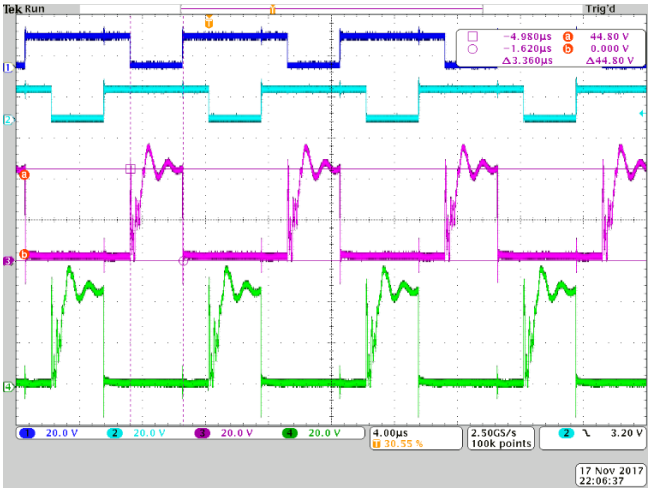

Fig. 6. Gate voltages (G_{S1} and G_{S2}) and switch voltages (V_{S1}, V_{S2})

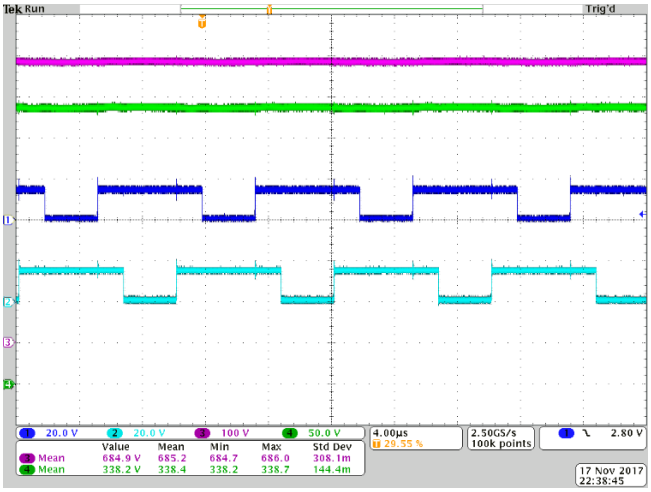

Fig. 7. Gate signals (G_{S1} and G_{S2}) and capacitor voltages (V_{C1}, V_{C4})

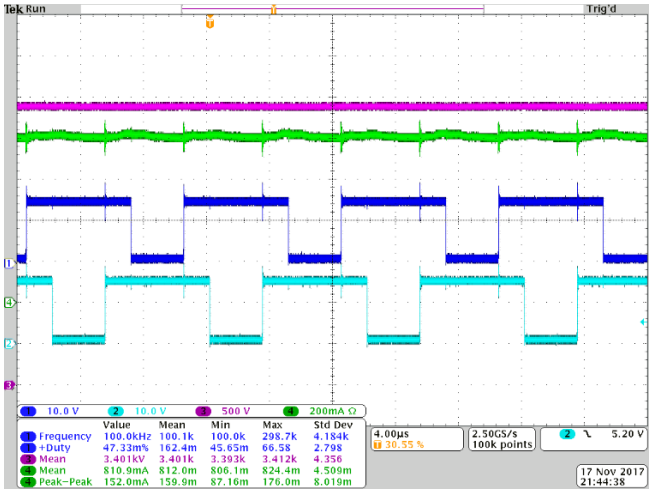

Fig. 8. Gate signals (G_{S1} and G_{S2}), input current (I_{IN}), and output voltage (V_{OUT})

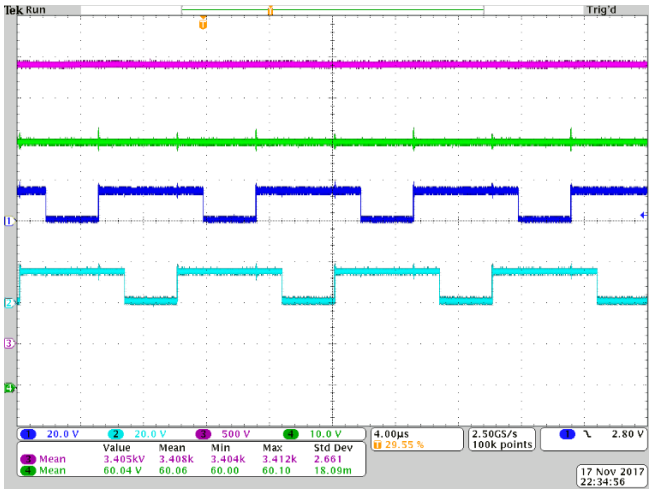

Fig. 9. Gate signals (G_{S1} and G_{S2}), output voltage and clamp capacitor voltage

The efficiency of the hardware prototype was measured for 10 W output power operation over changing input voltages (shown in Fig. 10). The maximum efficiency of the proposed converter is observed to be 85.57% at 15 V input voltage. The hardware images, experimental waveforms, and efficiency plot display the effectiveness of the proposed topology in terms of form factor and performance.

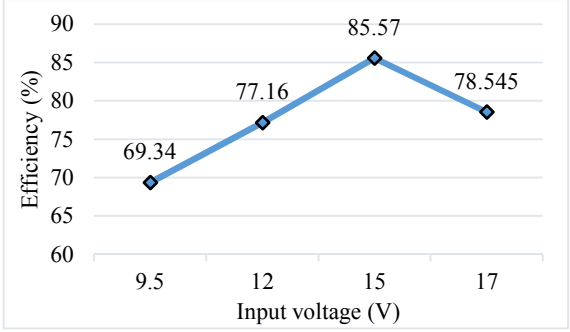

Fig. 10. Efficiency plot over varying input voltage (10 W output power)

IV. CONCLUSION

This paper introduces a high-voltage-gain dc-dc converter that acts as a power processing unit for a multi-mode monopropellant-electrospray propulsion system used in satellites. The proposed topology offers a higher voltage gain range that is capable of regulating the power processing unit output voltage at 3400 V over a varying input voltage range, i.e., 9.5 V to 17 V. The semiconductor switches in the topology observe a very small voltage relative to the output voltage. The input current drawn from the batteries is continuous with very low ripple. The construction, modes of operation, and theoretical analysis of the converter have been discussed and later verified by building a hardware prototype of the PPU. The hardware prototype developed to verify the theoretical analysis displayed a peak efficiency of 85.57%. The proposed high-voltage-gain dc-dc converter offers better efficiency, form factor, and reliability making it most suitable for space applications.

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