A Nonisolated Three-Level Bidirectional DC-DC Converter

Jianfei Chen[1, 2], Caisheng Wang[2], Jian Li[1], Chenguang Jiang[2] and Chen Duan[2]
1. School of Electrical Engineering, Chongqing University, Chongqing, China, 400044, China
2. Electrical and Computer Engineering, Wayne State University, Detroit, Michigan, 48202, US.
Email: cjf6221@gmail.com, cwang@wayne.edu, lijian@cqu.edu.cn

***Abstract* — A new nonisolated three-level bidirectional dc-dc converter (TLBDC) is introduced in the paper. Compared with the existing TLBDCs, the proposed TLBDC shows superior performance, including a large conversion ratio, small voltage stresses across all components, common ground for input and output terminals, and automatic current balancing function for inductor currents. A closed control strategy including a voltage loop and a voltage balance loop is also developed. Experimental results confirm the validity of the proposed converter and the closed loop control strategy.**

***Keywords* — dc-dc; High Conversion Ratio; Automatic Current Balancing; Voltage Balance.**

I INTRODUCTION

For dc energy systems consisting of cells connected in series and parallel, such as battery energy storage systems and fuel cell systems, it is desirable to have fewer cells connected in series so that the system can achieve higher system reliability and easier system management (such as voltage balancing) [1]. Fewer cells connected in series with more in parallel result in lower voltage and higher current. However, on the other hand, a higher dc link voltage is needed for better system performance including higher system efficiency. In electric vehicles, for example, the dc link voltage of the motor inverter has a tendency to increase in order to utilize high-speed high-power motor and improve conversion efficiency and power density of the inverter [2]. Therefore, a bidirectional dc-dc converter with a large conversion ratio is needed.

Traditional two-level non-isolated buck/boost converter has been used in many applications due to its simple structure, low cost, and high efficiency. However, in medium-to-high voltage (more than 400V) and medium-to-high power applications such as electric vehicles [2, 3], battery energy storage system [4, 5], fuel cell systems [6], fast dc charging stations [5, 7], and voltage-balance systems [8], an input-series-output-series three-level bidirectional dc-dc converter (ISOS-TLBDC) is more preferred as it reduces the voltage stress on the switches by half, doubles the effective switching frequency, and reduces the magnetic core size. However, there is a drawback that the conversion ratio of the three-level buck/boost converter is the same as that of the two-level buck/boost converter. Another limitation is that the input terminal and the output terminal are not commonly grounded, which increases electromagnetic interference (EMI) and limits its wide application in industry. A flying-capacitor based three-level bidirectional dc-dc converter (FC-TLBDC) is proposed to solve the commonly grounded issue [9, 10]. However, the conversion ratio is still low as they are all input-series-output-series (ISOS) architectures essentially. A switched-capacitor based three-level bidirectional dc-dc converter (SC-TLBDC) is also presented in [11] to achieve a large conversion ratio at the expense of current stresses across switches and high current ripple.

In order to address the aforementioned challenges, a new three-level bidirectional dc-dc converter (TLBDC) is proposed in the paper. A large conversion ratio, small voltage stresses across all devices and automatic current balancing at a full duty cycle range are achieved in the proposed TLBDC. Besides, the input terminal and the output terminal of the proposed TLBDC are commonly grounded, which helps reduce EMI. All the work in the paper is an extension of the researches in [12] and [13].

II OPERATING PRINCIPLE

The proposed TLBDC is presented in Fig. 1. It uniquely combines two phase buck converters (or two phase Boost converters) and a switched-capacitor network, which makes a nonisolated input-series-output-parallel three-level Buck converter possible. In the topology, C_1, S_1, S_3, and L_1 construct one Buck module, named as Buck I; C_2, S_5, S_2, and L_2 construct the other Buck module, named as Buck II. It should be noted that Buck II is an indirect Buck converter as the two switches S_5, S_2 are not connected directly. The Buck II is indirectly developed with an additional switch S_4 and one flying capacitor C_f inserted in the topology. It can be seen that S_4, C_f together with C_1 and S_2 construct the switched-capacitor network, in which the capacitor voltage of C_f is clamped by the capacitor voltage of C_1. The detailed operating principle analysis of the topology is given as below.

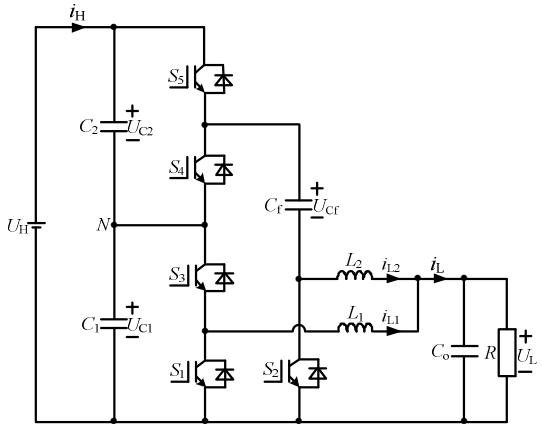
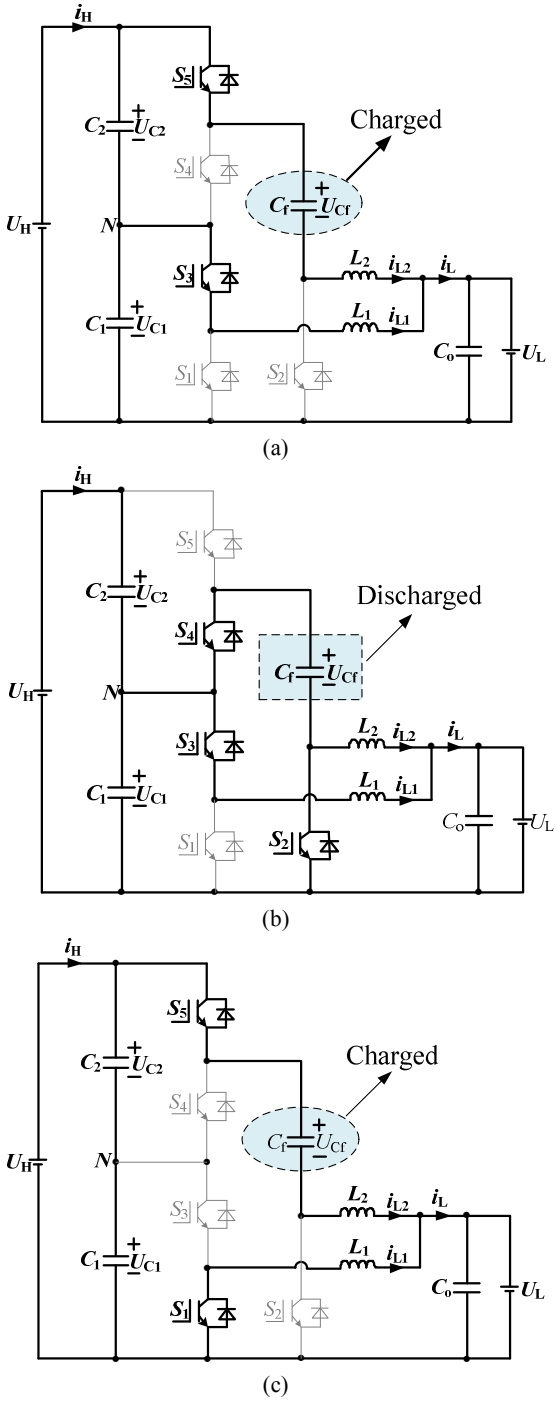


Fig.1 The proposed TLBDC.

A. Operating Principle for the Step-down Mode

Fig. 2 shows topological stages of the proposed TLBDC under the step-down mode. Switches S_1 and S_2 are driven by the same duty cycle with a phase shift angle of 180 degrees, while S_1, S_3 are complementary and S_2, S_5 are complementary. The switches S_2 and S_4 are driven by the same signal. The voltage of C_f is clamped by the capacitor voltage of C_1 due to the conduction of S_2 and S_4 in the switched-capacitor network, i.e., U_{Cf} equals to U_{C1}.



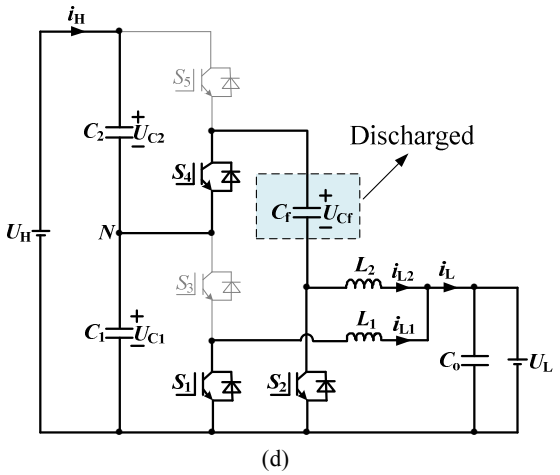


Fig. 2. Equivalent circuits of the proposed TLBDC under the step-down mode: (a) stage I; (b) stage II; (c) stage III; (d) stage IV.

1) Stage I: When switches S_3, S_5 turn on, the low voltage side load is charged through inductor L_1 by capacitor C_1 in Buck I. At the meantime, as the capacitor voltage U_{Cf} is clamped by the capacitor voltage U_{C1} in Stages II and IV, i.e., U_{Cf} equals to U_{C1}. Therefore, it can be regarded that the low voltage side load is also charged through inductor L_2 by capacitor C_2 in Buck II. During this stage, the flying capacitor C_f provides voltage support for developing the Buck II and it is charged with the current i_{L2} flowing through the inductor L_2.

2) Stage II: When switches S_2, S_3, S_4 turn on, the low voltage side load is still charged through inductor L_1 by capacitor C_1 in Buck I, while inductor L_2 charges the load in Buck II. More importantly, the voltage of C_f is clamped by the capacitor voltage of C_1 due to the conduction of switches S_4 and S_2 in the switched-capacitor network, i.e., U_{Cf} equals to U_{C1}. The two parallel capacitors C_1 and C_f together serve as the input voltage of Buck I. During this stage, the flying capacitor C_f is discharged as it is clamped by the capacitor C_1 in Buck I.

3) Stage III: When switches S_1, S_5 turn on, only inductor L_1 charges the low voltage side load in Buck I. Like stage I, U_{Cf} equals to U_{C1}, thus the load is charged through inductor L_2 by the capacitor C_2 in Buck II and the flying capacitor C_f is charged with the current i_{L2} flowing through the inductor L_2 during this stage.

4) Stage IV: When switches S_1, S_2, S_4 turn on, the two inductors L_1 and L_2 both supply energy to the low voltage side load. Moreover, the flying capacitor C_f is also clamped by the capacitor C_1 due to the conduction of switches S_4 and S_2. Like stage II, the flying capacitor C_f is discharged as it is clamped by the capacitor C_1 in Buck I during this stage.

Assuming the duty cycle of switches S_3 and S_5 is d_1. When d_1 is over 0.5, the converter under the step-down mode operates at the periodic stages of I, II, I, and III. When d_1 is smaller than 0.5, it operates at the periodic stages of IV, II, IV, and III. On the whole, the same output expressions can be derived by:

$$\frac{U_L}{U_H}=\frac{d_1}{2} \tag{1}$$

$$U_{C1} = U_{C2} = \frac{1}{2} U_H \tag{2}$$

$$\Delta i_{L1} = \Delta i_{L2} = \frac{U_L}{L} \frac{1 - d_1}{f_s} \tag{3}$$

Where U_{C1}, U_{C2} represent the voltages of C_1 and C_2, and Δi_{L1}, Δi_{L2} represent the current ripples of L_1 and L_2. Besides, the total output current ripple is not difficult to calculate by:

$$\Delta i_L = \begin{cases} \frac{U_L}{L} \frac{(2d_1 - 1)(1 - d_1)}{d_1 f_s} & d_1 > 0.5 \\ \frac{U_L}{L} \frac{1 - 2d_1}{f_s} & d_1 \le 0.5 \end{cases} \tag{4}$$

B. Step-up Mode

When the proposed converter operates under the step-up mode, the operating principle is similar to that under the step-down mode. Thus, it is not repeated in this section. Under the step-up mode, d_2 represents the duty cycle of S_1 and S_2. The key output results are achieved as follows:

$$\frac{U_H}{U_L} = \frac{2}{1 - d_2} \tag{5}$$

$$\Delta i_{L1} = \Delta i_{L2} = \frac{U_L}{L} d_2 T_s = \frac{U_L}{L} \frac{d_2}{f_s} \tag{6}$$

$$\Delta i_L = \begin{cases} \frac{U_L}{L} \frac{2d_2 - 1}{f_s} & d_2 > 0.5 \\ \frac{U_L}{L} \frac{d_2(1 - 2d_2)}{(1 - d_2) f_s} & d_2 \le 0.5 \end{cases} \tag{7}$$

III PERFORMANCE ANALYSIS

A Component Stresses

Taking the step-down mode as an example, the voltage stresses across all the components are half of the input voltage U_H:

$$U_{C1} = U_{C2} = U_{Cf} = U_{S1} = U_{S2} = U_{S3} = U_{S4} = U_{S5} = \frac{1}{2} U_H \tag{8}$$

The average currents across S_1-S_5 are given as follows:

$$I_{S1} = (1 - d_1) I_{L1} = 0.5(1 - d_1) I_L \tag{9}$$

$$I_{S1} = I_{S2} = I_{L2} = 0.5 I_L \tag{10}$$

$$I_{S3} = I_{S4} = I_{S5} = I_H \tag{11}$$

B Automatic Current Balancing

It can be seen from Fig. 2 that flying capacitor C_f is discharged only when switches S_4 and S_2 turn on during stages II and IV. Hence, the average discharging current flowing through C_f is as the same as the average current flowing through S_4 during one whole switching period. As a consequence, the discharged electric charges of C_f during one switching period can be written as $I_{S4}*T_s$. In addition, when the duty cycle d_1 is smaller than 0.5, C_f is only charged during stage III with the average charging current I_{L2} and the charging time $d_1 T_s$. When d_1 is greater than 0.5, C_f is charged during stage I and stage III with the average charging current I_{L2} and the total charging time $d_1 T_s$. It can be found that the charged electric charges of C_f during one switching period can be calculated by $I_{L2}*d_1 T_s$ no matter the duty cycle d_1 is greater or smaller than 0.5. Therefore, according to the Ampere-Second Balance Principle applied on the flying capacitor C_f, there is:

$$I_{S4} * T_s = I_{L2} * d_1 T_s \tag{12}$$

On the other hand, according to Kirchhoff's Current Law, there is

$$I_{S1} = I_{S3} = I_{S4} = I_{S5} = I_{in} \tag{13}$$

According to Power Conservation Principle, there is

$$I_{L1} + I_{L2} = I_o = \frac{I_{in} U_{in}}{U_o} \tag{14}$$

Finally, according to (10)-(14), there is

$$I_{L1} = I_{L2} = \frac{1}{2} I_o \tag{15}$$

From (15), it can be found that the two inductor currents in the converter are automatically balanced under the step-down mode. Also, the same automatic balancing mechanism can be suitable for the converter under the step-up mode. Thus, additional current-sharing control strategies as well as current sensors required in parallel interleaving multi-phase dc-dc converters [14], are not needed for the proposed converter.

C Comparative Analysis

Comparative analysis among the ISOS-TLBDC, FC-TLBDC, SC-TLBDC and the proposed TLBDC is presented in Table I. It can be found that the proposed converter shows superior performance, including a two-time conversion ratio, small voltage stresses across all the switches, and automatic current balancing though some more components are added. The input and output terminals are commonly grounded. More importantly, all the performance for the converter is achieved at a full duty cycle range. The automatic current balancing function makes it easy to control and current sensors for the inductors are not necessary.

Table. I Comparative analysis

TLBDCs	*L*	*S*	*C*	G (step-down)	G (step-up)	Voltage Stress	Current Stress	Current Ripple	Commonly Grounded	Automatic Current Balancing
ISOS-TLBDC	2	4	2	d_1	$1/(1-d_2)$	$0.5U_H$	Large	Small	No	-
FC-TLBDC	1	4	2	d_1	$1/(1-d_2)$	$0.5U_H$	Large	Small	Yes	-
SC-TLBDC	1	4	3	$d_1/2$	$2/(1-d_2)$	$0.5U_H$	Large	Large	Yes	-
Proposed	2	5	3	$d_1/2$	$2/(1-d_2)$	$0.5U_H$	Small	Small	Yes	Yes

D Closed Loop Control

Like the existing three-level bidirectional dc-dc converters, the voltage difference between C_1 and C_2 in the proposed topology should be considered. For the converter under the step-down mode, to address the neutral-point potential imbalance issue, a closed loop control strategy with including a voltage loop and a voltage-balance loop is given in Fig. 3.

d_{S3} and d_{S5} respectively represents the duty cycles of S_3 and S_5 with a voltage balance loop. Δd_1 represents the duty cycle variables due to the voltage-balance loop. C_{a1}, C_{a2} are two triangular carrier waves with phase shift angle of 180 degrees. Thus, the two duty cycles d_{S3}, d_{S5} can be written by:

$$\begin{cases} d_{S3} = d_1 - \Delta d_1 \\ d_{S5} = d_1 + \Delta d_1 \end{cases} \tag{16}$$

When U_{C2} increases, U_{C1} will decrease because the input voltage is constant under steady state. According to Fig. 3, Δd_1 becomes positive, which makes d_{S3} decrease and d_{S5} increase. As a result, U_{C1} increases while U_{C2} decreases as U_o is stable due to the voltage loop. On the whole, a negative feedback has been built automatically. Finally the two capacitor voltages can be balanced with the same value and the neutral-point potential imbalance issue can be solved.

Also, for the converter under the step-up mode, the duty cycles of S_1 and S_2 are given in (17) and the closed loop control strategy is given in Fig. 4. At this mode, the voltage balance process is similar to that under the step-down mode.

$$\begin{cases} d_{S1} = d_2 - \Delta d_2 \\ d_{S2} = d_2 + \Delta d_2 \end{cases} \tag{17}$$

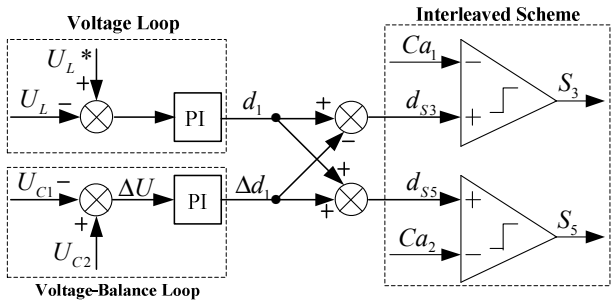


Fig. 3 Closed loop control under the step-down mode.

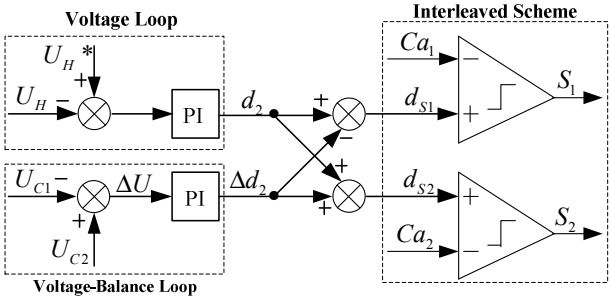


Fig. 4. Closed loop control under the step-up mode.

IV Experimental Verification

To verify the proposed converter and control strategy, a 400W experimental prototype has been built according to the following parameters: the low side voltage is 48V and the high side voltage is 400V; the switching frequency is 25 kHz; the two inductors are designed to be 780uH, and the three capacitors are all 470uF; all the power switches are selected as G80N60. The experimental prototype is presented in Fig. 5. The key experimental results of the converter under the step-down mode and the step-up mode are presented in Figs. 6 and 7, respectively.

It can be seen from Fig. 6 that the output voltage of the converter is stable with the designed value 48V under the step-down mode. The total output current ripple is smaller than the two inductor current ripples and the total output current ripple frequency is 50 kHz, which is two times the switching frequency 25 kHz. Furthermore, the two average inductor currents are both 4.9 A, and the total inductor current is 9.8A, which nearly matches with its theoretical value 10.0A. The same average inductor current verifies the automatic current balancing function. Besides, the two input capacitor voltages are nearly the same with 200V, which also verifies the voltage balance control strategy. On the other hand, Fig. 7 shows that the output voltage of the converter under the step-up mode is stable with the designed value 400V. The drive signals of switches S_1 and S_2 are phase shifted with 180 degrees. The two inductor currents are also balanced with the same average value.

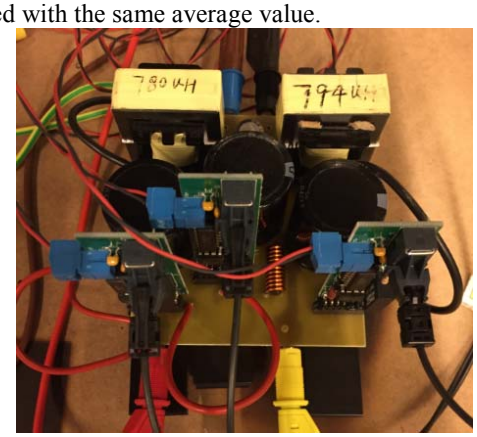
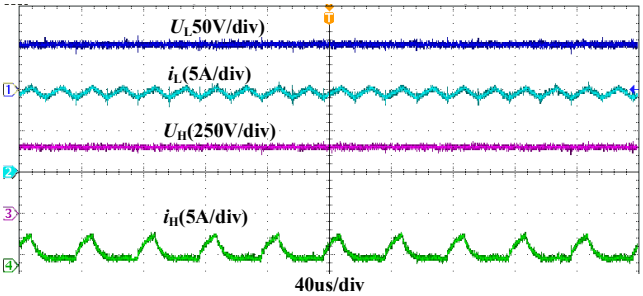


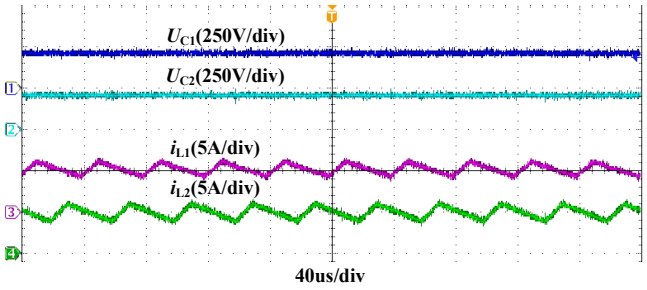
Fig. 5 The experimental prototype.

Taking the step-down mode as an example, the voltage balance process is also given in Fig. 8. It can be seen from Fig. 8 that there is about 10V voltage difference between the two capacitors C_1 and C_2. However, it is reduced to be zero once the voltage-balance control is added. And this verifies correctness of the proposed voltage-balance control strategy. On the other hand, taking the step-up mode as an example, the dynamic results of the converter are presented in Fig. 9. It can be seen that the output voltage keeps stable when the input voltage jumps from 48V to 96V. Under this condition, the two inductor currents decrease smoothly from one high stable value into another low stable value. It indicates that the converter has a good dynamic performance.

In the end, the conversion efficiency of the converter is 92.9% under the step-down mode and 92.08% under the step-up mode. Much high conversion efficiency can be reached by optimizing circuit design, using soft switching technique and wide bandgap semiconductor devices in the further.

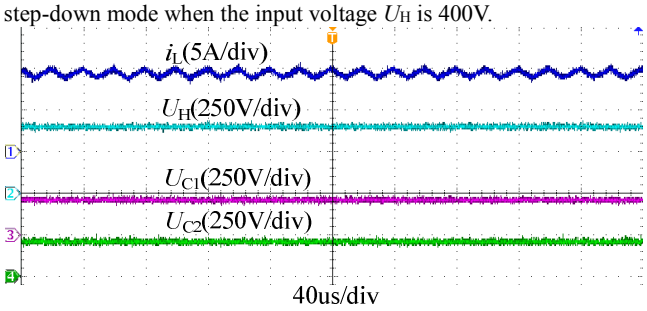


(a) key results

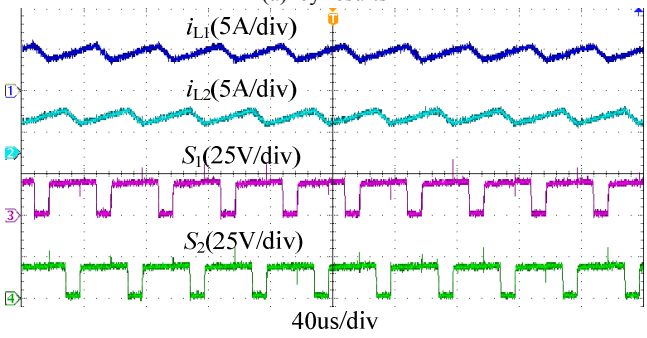


(b) capacitor voltages

Fig. 6. Key experimental results of the converter under the step-down mode when the input voltage U_H is 400V.



(a)key results



(b) inductor currents and key drive signals

Fig. 7. Key experimental results of the converter under the step-up mode when input voltage U_L is 48V.

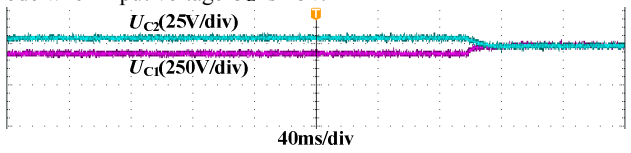
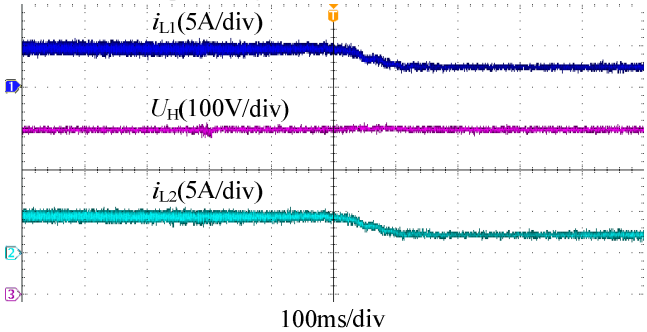


Fig. 8. Voltage balance process of the converter under the step-down mode when the input voltage U_H is 400V.



(c) dynamic results

Fig. 9. Key experimental results of the converter under the step-up mode when input voltage U_L jumps from 48V to 96V.

V Conclusion

A new non-isolated TLBDC introduced in the paper with superior performance. A closed loop control with simple voltage balance control is presented to make it easy to implement. All of these makes it a good alternative for nonisolated dc-dc conversion applications. The drawback of the converter is increased power loss due to the switched-capacitor network.

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