A phase-shift-based synchronous rectification scheme for bi-directional high-step-down CLLC resonant converters

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***Abstract*—A frequency-modulated bi-directional CLLC resonant converter with high-step-down feature designed for power-to-gas applications is presented. To avoid magnetizing current being provided from low voltage side, which causes remarkable conduction loss and current stress in a high-step-down design, a novel synchronous rectification scheme based on small phase shift technique is proposed. The switching transient under the proposed scheme is analyzed, which indicates that the reactive current of low-voltage side can be eliminated when the switching frequency equals the resonant one. Furthermore, the steady-state characteristics of the converter are discussed. A prototype is built, and experimental results have verified the principles and the benefits of the proposed scheme.**

Keywords—CLLC resonant converter, phase shift, synchronous rectification, high-step-down

I. INTRODUCTION

Power-to-gas (P2G) is an emerging solution for massive energy storage, where excessive electricity from renewable energy plants is utilized to produce hydrogen or synthetic natural gas, and the collected gas is consumed to generate electricity during high-demand periods [1]. A promising technology to realize the electrochemical reactions is solid-oxide cells (SOC), which, need bi-directional power converters to interchange energy with the grid. Commonly, a SOC stack module demands an isolated power supply with high operating current but low terminal voltage [2]-[3], and it is preferred to apply a cascaded design to satisfy these demands step-by-step, as shown in Fig. 1. Additionally, there have also been attempts to integrate both high-step-down and wide-output-range features into one single dc-dc converter, but in many cases, the efficiency drops when the output voltage deviates from the nominal value [4]-[6].

In pursuit of high efficiency, this study applies the frequency-modulated CLLC resonant converter [7] for the high-step-down dc-dc conversion demand of SOCs, i.e., the converter #2 in Fig. 1. Comparing to the common LLC converter, CLLC converter has symmetrical characteristic for bi-directional operations [8]-[9], and is hence preferred in P2G application. However, the efficiency of a CLLC converter is heavily influenced by two issues: power loss due to diode forward voltage, and conduction loss caused by high magnetizing current from the low voltage side. Synchronous

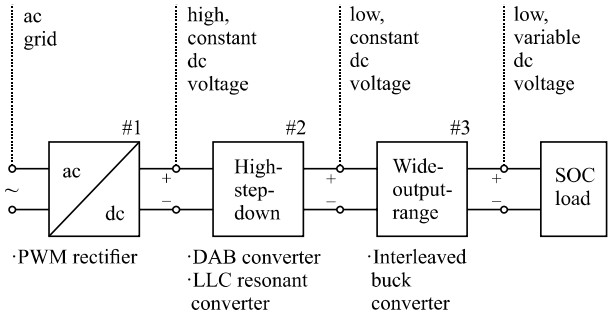
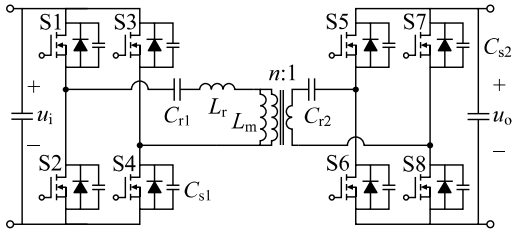
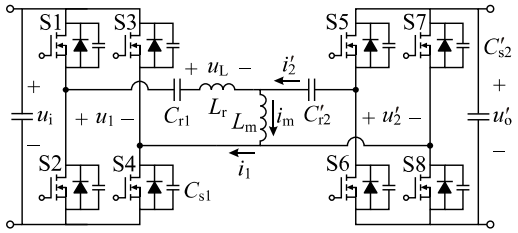


Fig. 1. Diagram of power converter for SOCs



(a) Basic topology



(b) Normalized equivalent circuit

Fig. 2. Circuit of full-bridge CLLC resonant converter

rectification (SR) is a potential way to solve the first issue, and has been widely applied on LLC converters [10]-[11], but so far relevant discussions are limited on CLLC designs [12]. In [13], a modified SR scheme aiming at eliminating additional circulating current is proposed, but still it does not address the second issue, which emerges in certain cases depending on the design of resonant tank and power direction, and still lacks thorough study. Aim at these issues, a novel SR scheme based on small phase shift is proposed in this paper, and the steady-state characteristics of the converter are analyzed. Furthermore,

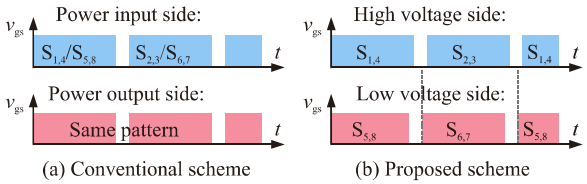


Fig. 3. Conventional and proposed SR schemes for CLLC converter

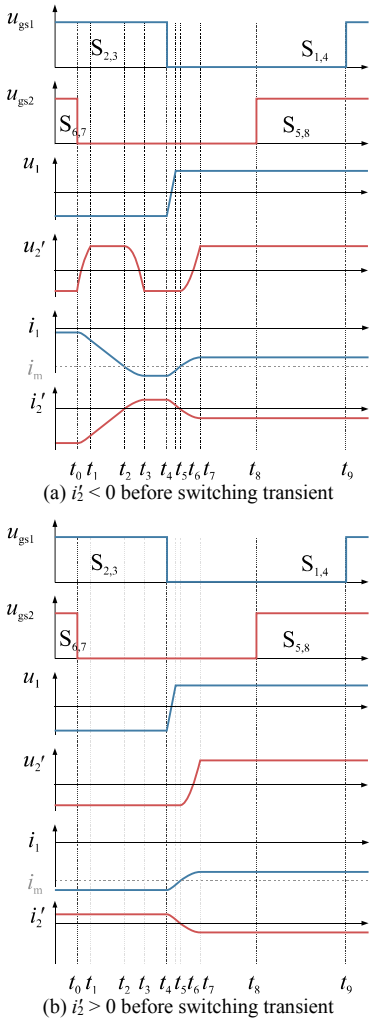


Fig. 4. Key waveforms of switching transient

a prototype is built and the theoretical conclusions are verified through experiments.

II. Principle of Switching Transient

The schematic and the normalized equivalent circuit of a frequency-modulated CLLC resonant converter are illustrated in Fig. 2, where L_r, C_{r1}, C_{r2} compose a resonant tank with a resonant frequency of f_r, and L_m is usually more than three times larger than L_r. The conventional SR scheme for full-bridge resonant converter is shown in Fig. 3(a). Under this scheme, the source of the magnetizing current cannot be actively decided, and when provided by the low voltage side, the magnetizing component of the current will reach a very high level, causing significant copper loss in transformers as well as conduction loss in switches.

However, considering cost, power density and some other practical limitations, it is not always allowable to reduce the magnetizing current by further increasing f_r or L_m, and it is hoped to have the magnetizing current constantly provided by the high voltage side in all conditions, so the current stress and loss can be reduced. Aim at this demand, an improved SR scheme is proposed, as illustrated in Fig. 3(b), where the switches of both sides run at the same duty cycle that slightly lower than 50% due to the existence of dead-time; the gate signals for the low voltage side has a small phase shift, which is less than the dead-time.

The following assumptions are made for the analysis of switching transient:

(i) As L_m is significant than L_r, the voltage on L_m is close to a square wave, and therefore, i_m is regarded as a triangular wave in a switching period, and is constant during switching transient;

(ii) The resonant period of the resonant tank is far longer than the switching transient, so the voltage variation of C_{r1}, C_{r2} are neglected during the switching transient;

(iii) In the application of this work, the output voltage of CLLC converter only varies in a small range, so $u_i = u_o' = u_{dc}$;

(iv) Apart from switching transients, the changing rates of i_1 and i_2' are generally low, and its influence is ignored in the switching transient analysis.

The switching transient when u_1, u_2' change from negative to positive is taken here as an example. According to the direction of i_2', two circumstances are discussed separately. The theoretical waveforms are shown in Fig. 4.

A. $i_2 < 0$ before switching transient

Before t_0, $u_1 = u_2' = -u_{dc}$, and $i_m < 0$. Based on assumption (iv), u_L is close to zero. S6 & S7, as well as S2 & S3 are conducting.

Stage 1 [t_0, t_1]: At time t_0, S6 & S7 turn off. The direction of i_2' satisfies ZCS condition, and i_2' begins to charge the parasitic capacitance of S6 & S7 and discharge that of S5 & S8, until at time t_1, when $u_2' = u_{dc}$, and body diodes D5 & D8 start conducting. If the initial value of i_2' is large, this process will be very quick.

Stage 2 [t_1, t_2]: Since $u_2' = u_{dc}$, i_1 decreases and i_2' increases at a high and constant rate, which is equal to

$$\frac{di_2'}{dt} = \frac{2u_{dc}}{L_r} \tag{1}$$

Stage 3 [t_2, t_3]: At time t_2, i_2' reaches zero, D5 & D8 turn off and, after another charging process, D6 & D7 turn on. The resonant process of C_{s2}' and L_s determines the time and the end state of this stage, which are

$$T_{23} = 0.5\pi\sqrt{L_s C_{s2}'} \tag{2}$$

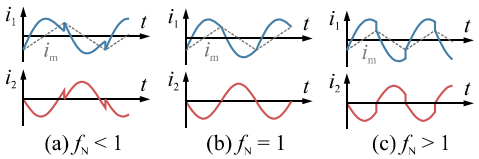


Fig. 5. Key steady-state current waveforms

$$i_2' = 2u_{dc}\sqrt{\frac{C_{s2}'}{L_r}} \tag{3}$$

Stage 4 [t_3, t_4]: At this stage, $u_1 = u_2' = -u_{dc}$, u_L is almost zero, hence i_1, i_2' change at a very slow rate. Moreover, as $i_m < 0$ and i_2' is slightly larger than 0, there should be $i_1 < 0$, meaning that S2 & S3 are conducting.

Stage 5 [t_4, t_5]: At time t_4, S2 & S3 turn off. i_1 begins to charge/discharge the parasitic capacitance of S1-S4, and when finished, the body diodes D1 & D4 start conducting. The time of this stage is mainly decided by i_m. If i_m is not too small, the period of this stage can be neglected.

Stage 6 [t_5, t_6]: With $u_L = 2u_{dc}$, i_2' decreases at a high and constant rate, which is opposite to the value in (1). Combining (1) and (3), the lasting time would be

$$T_{56} = \sqrt{L_s C_{s2}'} \tag{4}$$

Stage 7 [t_6, t_7]: At time t_6, i_2' reaches zero, D6 & D7 turn off and, after another charging process, D5 & D8 turn on. Again, the resonant process of C_{s2}' and L_s determines the time and the end state of this stage, which are opposite to the values in (2) and (3).

Stage 8 [t_7, t_8]: During this stage, i_1, i_2' change at a very slow rate, and if the remaining time is short enough, i_2' will still be negative at the end of this period.

Stage 9 [t_8, t_9]: At time t_8, gate signals of S5 & S8 turns positive, and since D5 & D8 are on right before time t_8, the turning-on satisfies ZVS conditions.

Stage 10: At time t_9, similarly, S1 & S4 turn on under ZVS conditions.

B. $i_2 > 0$ before switching transient

If $i_2 > 0$, then at time t_0 the current will switch from S6 & S7 to D6 & D7, and afterwards the status of the system will not change significantly. Before the turn-off signals of S2 & S3 arrive, there will be $u_1 = u_2' = u_{dc}$, $u_L = 0$, $i_2' > 0$, $i_m < 0$, $i_1 < 0$, the same to the status of Stage 3 in part A. Therefore, when S2 & S3 turn off, the system will respond as [t_4, t_9] described in the previous part.

In summary, for both cases, at the end of the switching transient, i_2' equals to its value at time t_7, which is

$$i_2' = -2u_{dc}\sqrt{\frac{C_{s2}'}{L_r}} \tag{5}$$

If the load is not very light, the value will be far below the peak value of i_2', so it can be considered that i_2' equals to 0 at the end of the conversion. Apparently, when the converter is modulated at a switching frequency close to f_r, the low voltage side will provide almost zero reactive power, and the magnetizing current is fully provided by the high voltage side.

III. Steady-State Characteristic

In a CLLC converter, the current waveform beyond switching transients can be regarded as sinusoidal waves at resonant frequency. Based on this assumption, the simplified key steady-state current waveforms are illustrated in Fig. 5 where $f_N = f_s/f_r$ and dead-time is neglected.

The steady-state voltage gain characteristic can be obtained using the fundamental harmonic approximation analysis method. Firstly, the phasor quantities $\dot{\boldsymbol{U}}_{1ac}$, $\dot{\boldsymbol{U}}_{2ac}'$ and $\dot{\boldsymbol{U}}_m$ are introduced, which respectively denote to the fundamental phasor of u_1, u_2' and the voltage of X_m. The zero phase is defined as the phase of $\dot{\boldsymbol{U}}_{2ac}'$, so scalar quantity U_{2ac}' is directly used in the following analysis. Due to the existence of deadtime, the phase of $\dot{\boldsymbol{U}}_{1ac}$ is neither exactly zero nor the phase-shift of the controller, so the phase should remain as a variable. The relationships between the dc voltage and the fundamental phasor amplitude are

$$U_{1ac} = \frac{\sqrt{2}}{2}\frac{4}{\pi}u_i = \frac{2\sqrt{2}}{\pi}u_i \tag{6}$$

$$U_{2ac}' = \frac{\sqrt{2}}{2}\frac{4}{\pi}u_o' = \frac{2\sqrt{2}}{\pi}u_o' \tag{7}$$

Then, define k_b as the ratio of the reactive and the active parts of fundamental harmonics of i_2', which is calculated as follows.

$$\begin{aligned} k_b(f_N) &= \frac{I_{2\text{-imag}}'}{I_{2\text{-real}}'} = \frac{\int_0^{1/f_N}\sin\pi t\cdot\cos\pi f_N t\cdot \mathrm{d}t}{\int_0^{1/f_N}\sin\pi t\cdot\sin\pi f_N t\cdot \mathrm{d}t} \\ &= \frac{\int_0^{1/f_N}\left[\sin\frac{1+f_N}{2/\pi}\cdot\cos\frac{1+f_N}{2/\pi} - \sin\frac{f_N-1}{2/\pi}\cdot\cos\frac{f_N-1}{2/\pi}\right]\mathrm{d}t}{\int_0^{1/f_N}\left[\sin\frac{1+f_N}{2/\pi}\cdot\sin\frac{1+f_N}{2/\pi} - \sin\frac{f_N-1}{2/\pi}\cdot\sin\frac{f_N-1}{2/\pi}\right]\mathrm{d}t} \\ &= \frac{\frac{f_N}{f_N+1}\left[\cos\left(\frac{\pi(f_N+1)}{f_N}\right)-1\right] - \frac{f_N}{f_N-1}\left[\cos\left(\frac{\pi(f_N-1)}{f_N}\right)-1\right]}{\frac{f_N}{f_N-1}\sin\left(\frac{\pi(f_N-1)}{f_N}\right) - \frac{f_N}{f_N+1}\sin\left(\frac{\pi(f_N+1)}{f_N}\right)} \end{aligned} \tag{8}$$

As the amplitude of voltages and the phase of low-voltage side current are known, it can be deduced from Kirchhoff's circuit laws that the following equations are satisfied.

$$\frac{\dot{\boldsymbol{U}}_{1ac} - \dot{\boldsymbol{U}}_m}{\mathrm{j}(X_L + X_{C1})} = \frac{\dot{\boldsymbol{U}}_m}{\mathrm{j}X_m} + \frac{P}{U_{2ac}'}(1 + \mathrm{j}k_b(f_N)) \tag{9}$$

$$\dot{\boldsymbol{U}}_m = U_{2ac} + \mathrm{j}X_{C2}\cdot\frac{P}{U_{2ac}'}(1 + \mathrm{j}k_b(f_N)) \tag{10}$$

Where P is the output power of the converter.

Furthermore, to acquire a more general solution, the voltages and P in the equations are transformed into per-unit values, and the following symbols are introduced: $\lambda = L_m/L_r$, and $k_c = C_{r1}/(C_{r1}+C_{r2}/n^2)$, which is ratio of the two capacitor impedances. Note that if $k_c = 0$ or 1, the converter will have C_{r1} or C_{r2} short-circuited.

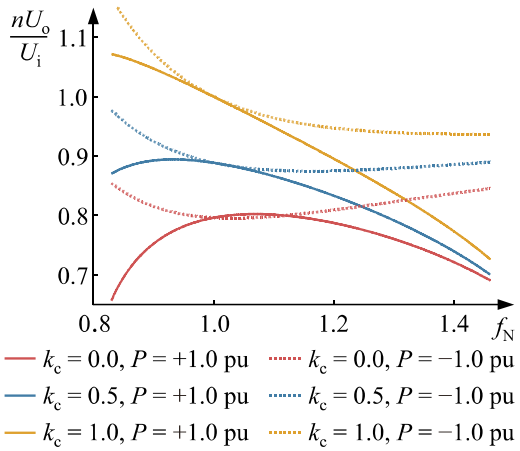


Fig. 6. Sample frequency-gain curves

$$X_m = \lambda X_L \tag{11}$$

$$X_{C1} = -k_c X_L / f_N^2 \tag{12}$$

$$X_{C2} = -(1 - k_c) X_L / f_N^2 \tag{13}$$

Based on (6) – (13), the frequency-gain curves of some sample circumstances are demonstrated in Fig. 6, where λ is set to 4 in all cases.

The figure indicates that when P = +1 pu, the output voltage U_o will reach maximum value at around f_N = 1, and U_o will decrease as f_N deviates from 1. When P = −1 pu, however, the variation tendency is reversed. The effective output voltage range should be between the maximum U_o of P = +1 pu and the minimum U_o of P = −1 pu, since any voltage within this range can be reached in all power conditions. Therefore, it can be concluded from the figure that the larger k_c is, the wider the output voltage range will be.

On the other hand, smaller k_c results in lower output voltage due to higher voltage being divided by C_{r1}-L_r, and for a desired ratio of the input and output voltages, the turns ratio of the transformer can be lowered. This feature helps reducing the transformer ratio n and is encouraged in a high-step-down design.

IV. Phase-Shift Calculation

When u_1 and u_2' change from positive to negative, the current i_2' will be the opposite of (5). Then, after half of the switching period, right before u_2' change from negative to positive, the end value of i_2' will be

$$i'_{2\text{-end}} = I'_{2\text{-amp}} \sin\left[\pi f_N + \arcsin\left(\frac{2u_{dc}\sqrt{C'_{s2}/L_r}}{I'_{2\text{-amp}}}\right)\right] \tag{14}$$

Where $I'_{2\text{-amp}}$ is the amplitude of low voltage ac current, but its sign is the same to P, i.e.,

$$I'_{2\text{-amp}} = \frac{P}{2\sqrt{2}U_o/\pi} \cdot (1 + k_b^2(f_N)) \tag{15}$$

If $i'_{2\text{-end}} < 0$, the waveform will be the same as Fig. 4(a). In this case, the high voltage switches must not turn off until i_2' becomes positive. Therefore, the time of phase-shift Δt should

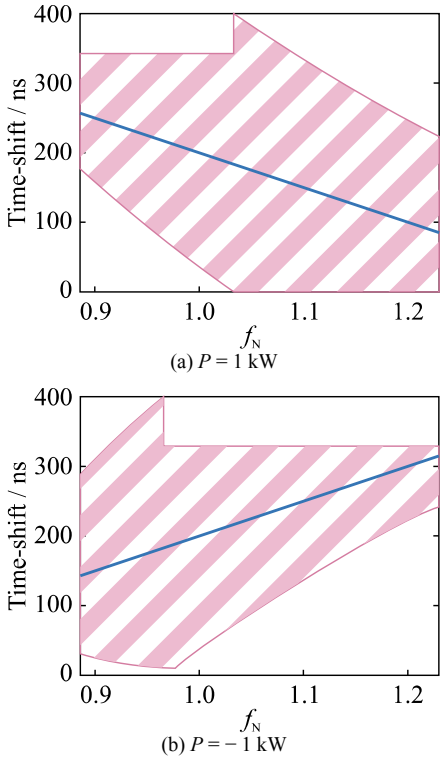


Fig. 7. Feasible time of phase-shift for a sample CLLC converter depending on switching frequency, where the shaded areas represent feasible operating point, and the blue line sketches a feasible control law for the shift

satisfy

$$\Delta t > -\frac{i'_{2\text{-end}} L_r}{2u_{dc}} \tag{16}$$

Then, after the high voltage switches turn off, the low voltage switches should turn off after i_2' becomes negative, i.e.,

$$t_{dead} - \Delta t > 0.5\pi\sqrt{L_r C'_{s2}} \tag{17}$$

However, if power flows from low voltage side to high voltage side, the trigger for low voltage switches should not be too late, otherwise i_2' will becomes positive and ZVS condition will not be satisfied, so

$$t_{dead} - \Delta t < \frac{1}{2\pi f_r} \arcsin\left(\frac{2u_{dc}\sqrt{C'_{s2}/L_r}}{I'_{2\text{-amp}}}\right) \tag{18}$$

If $i'_{2\text{-end}} > 0$, the waveform will be the same as Fig. 4(b). In this case, after the high voltage switches turn off, the low voltage switches should turn off after i_2' becomes negative, which is $i'_{2\text{-end}}$ divided by the current changing rate.

$$t_{dead} - \Delta t > \frac{i'_{2\text{-end}} L_r}{2u_{dc}} \tag{19}$$

Similarly, there is a maximum time period between the high voltage switches turn off and the low voltage switches turn on.

$$t_{dead} - \Delta t < \frac{u_{dc}\sqrt{C'_{s2}/L_r}}{\pi f_r I'_{2\text{-amp}}} \tag{20}$$

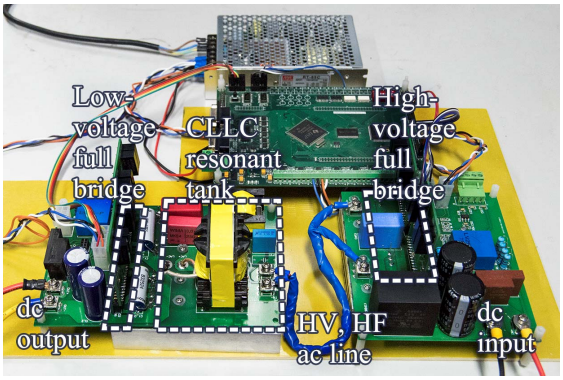


Fig. 8. Prototype of CLLC resonant converter

Combining the above equations, the feasible time-shift Δt can finally be acquired. An example of time-shift calculation result for a prototype CLLC resonant converter (parameters shown in Table 1) is shown in Fig. 7, where dead-time is constantly set to 400 ns. From the figures, it can be concluded that $\Delta t = t_{dead}/2$ is generally suitable for all cases. When $P > 0$, i.e., power flows from high voltage side to low voltage side, the best phase-shift decreases as switching frequency increases; when $P < 0$, phase-shift should be increased when switching frequency increases.

TABLE I. SPECIFICATION OF PROTOTYPE

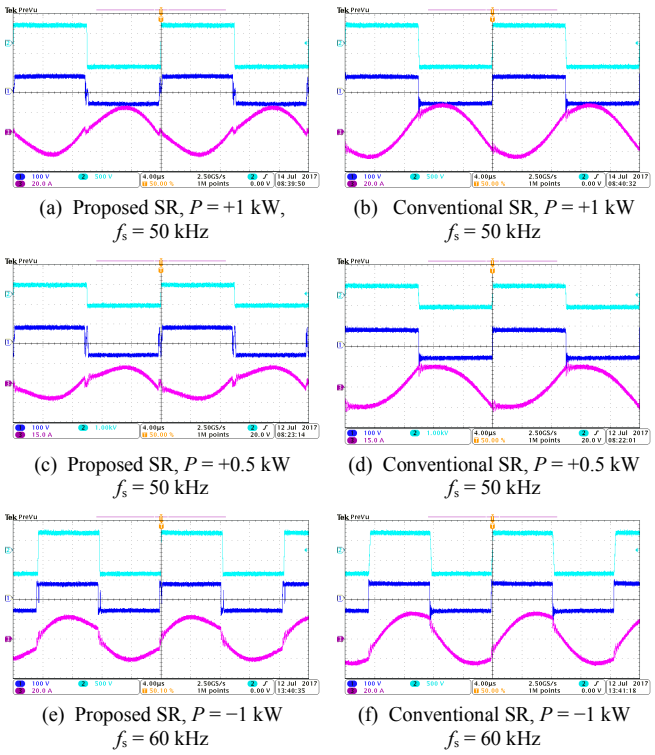
Parameter	Value	Parameter	Value
Nominal input voltage U_i	520 V	n (N_p:N_s)	34:5
Nominal output voltage U_o	70 V	L_r	150 μH
Nominal power P_0	±1.0 kW	L_m	550 μH
High voltage switches	Cree C2M0080120D	C_{r1}	0.1 μF
Low voltage switches	Infineon IRFP4127	C_{r2}	8.0 μF
		f_r	52 kHz

V. EXPERIMENT VERIFICATION

A prototype of the CLLC resonant converter has been built, as shown in Fig. 8, with the parameters summarized in Table 1. According to Fig. 7, the dead-time is chosen to be 400 ns, and phase-shift Δt is set as shown in (21), which, when when P = ±1 kW, is also the same to the blue lines in Fig. 7.

$$\Delta t = 200 - (f_N - 1)P/2 \text{ ns} \quad (21)$$

The experimental waveforms are given in Fig. 10, where switching frequency f_s is selected when both the high-voltage side voltage U_i and low-voltage side voltage U_o equal to the nominal values under the proposed scheme. The results clearly show that under the proposed SR scheme, the ac current of the low-voltage side i_2 is reset to a small value after every switching transient, and consequently the reactive part of the current is significantly suppressed. Comparing to the conventional SR scheme, the proposed SR scheme is capable to eliminate the fundamental reactive current from the low voltage side, and reduce the peak value of i_2. According to Fig.



(a) Proposed SR, P = +1 kW, f_s = 50 kHz
(b) Conventional SR, P = +1 kW f_s = 50 kHz
(c) Proposed SR, P = +0.5 kW f_s = 50 kHz
(d) Conventional SR, P = +0.5 kW f_s = 50 kHz
(e) Proposed SR, P = −1 kW f_s = 60 kHz
(f) Conventional SR, P = −1 kW f_s = 60 kHz

Fig. 9. Experimental waveforms of conventional and proposed SR scheme. Cyan line: u_1; blue line: u_2; magenta line: i_2.

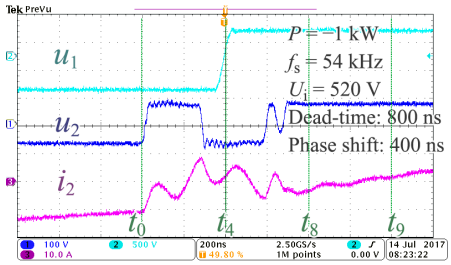


Fig. 10. Zoom-in of switching transient

10 (c) and (d), the advantage of proposed SR is even more significant under lower power operating points, where the magnetizing current component is more notable.

A typical transient waveform at switching moment is given in Fig. 10, where the dead-time is deliberately set to a higher value (800 ns) to clearly show the switching transient. The waveform shows consistency to the theoretical analysis in the previous sections.

Furthermore, a set of constant load, variable switching frequency (from 46 to 64 kHz) experiments under fixed U_i = 520 V condition were implemented, where U_o and the efficiency were measured, as plotted in Fig. 11. The results show the significant and important difference of the output-voltage characteristic between the two SR schemes: under the traditional scheme, U_o can hardly reach the nominal 70 V value in all cases. The reason is that the source of i_m differs under f_N > 1 and f_N < 1 conditions, leading to segmented f_N-U_o

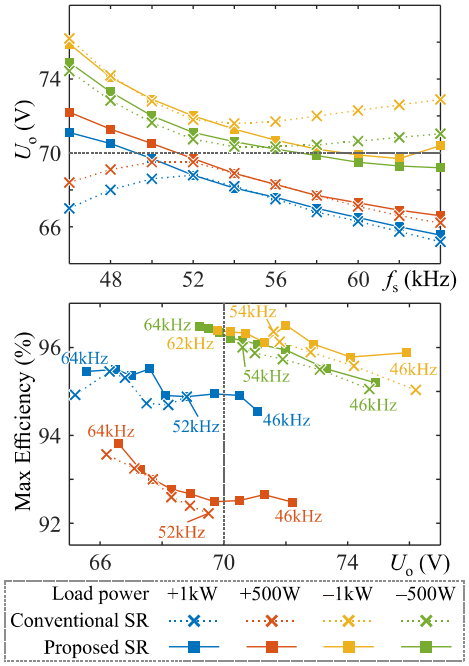


Fig. 11. Experimental results of efficiency with f_s limits noted in plot

characteristic with a limit of U_o reached near f_N = 1. The proposed scheme, however, has a unified f_N-U_o characteristic due to the constant source of magnetizing current, and consequently achieving an extended range of U_o, so the nominal output voltage is achieved in all cases.

Moreover, the figure also shows that at the same operating point (same U_o and P), the proposed SR scheme can generally achieve higher efficiency than the traditional SR scheme.

VI. Conclusions

This paper has proposed a new SR scheme for bi-directional high-step-down CLLC resonant converter. Utilizing the transient process of a phase shift between the bridges, this scheme keeps the magnetizing current being provided from a designated side. The principle of the switching process and the steady-state voltage gain of the converter have been analyzed and further verified by experiments. Comparing to the conventional scheme, the proposed one not only achieves higher efficiency in a high-step-down design by reducing the conduction loss of low voltage side, but also has a wider voltage gain and is thus able to stabilize the output voltage under bi-directional conditions. Still, the output voltage range is narrower than CLLC converters without SR, and the transient process is highly dependent to multiple parameters, bringing complexity to the selection of dead-time and phase shift.

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References

[1] S. Clegg and P. Mancarella, "Integrated modeling and assessment of the operational impact of power-to-gas (P2G) on electrical and gas transmission networks," *IEEE Transactions on Sustainable Energy*, vol. 6, no. 4, pp. 1234-1244, Oct. 2015.

[2] J. S. Herring, J. E. O'Brien, C. M. Stoots, et al, "Progress in high-temperature electrolysis for hydrogen production using planar SOFC technology", *International Journal of Hydrogen Energy*, vol. 32, no. 4, pp. 440-450, Mar. 2007.

[3] A. Kolli, A. Gaillard, A. De Bernardinis, et al, "A review on DC/DC converter architectures for power fuel cell applications", *Energy Conversion and Management*, vol. 105, pp. 716-730, Nov. 2015.

[4] Ke Jin and Xinbo Ruan, "Hybrid full-bridge three-level LLC resonant converter - a novel DC-DC converter suitable for fuel cell power system," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 361-367.

[5] T. LaBella, W. Yu, J. S. Lai, et al, "A bidirectional-switch-based wide-input range high-efficiency isolated resonant converter for photovoltaic applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3473-3484, July 2014.

[6] X. Sun, Y. Shen, Y. Zhu and X. Guo, "Interleaved boost-integrated LLC Resonant converter with fixed-frequency PWM control for renewable energy generation applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4312-4326, Aug. 2015.

[7] W. Chen, P. Rong and Z. Lu, "Snubberless bidirectional DC–DC converter with new CLLC resonant tank featuring minimized switching loss," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3075-3086, Sept. 2010.

[8] Z. U. Zahid, Z. M. Dalala, R. Chen, et al, "Design of Bidirectional DC–DC Resonant Converter for Vehicle-to-Grid (V2G) Applications," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 3, pp. 232-244, Oct. 2015.

[9] Yingying Cai, Cong Wang, Feng Zhao et al, "Design of a high-frequency isolated DTHB CLLC bidirectional resonant DC-DC converter," in *2014 IEEE Conference and Expo Transportation Electrification Asia-Pacific (ITEC Asia-Pacific)*, Beijing, 2014, pp. 1-6.

[10] W. Feng, F. C. Lee, P. Mattavelli and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3775-3781, Aug. 2012.

[11] M. Mohammadi, N. Shafiei and M. Ordonez, "LLC synchronous rectification using coordinate modulation," in *2016 IEEE Applied Power Electronics Conference and Exposition*, 2016, pp. 848-853.

[12] S. Zhao, Q. Li and F. C. Lee, "High frequency transformer design for modular power conversion from medium voltage AC to 400V DC," in *2017 IEEE Applied Power Electronics Conference and Exposition,* 2017, pp. 2894-2901

[13] S. Zou, J. Lu, A. Mallik, et al, "Bi-directional CLLC Converter with Synchronous Rectification for Plug-in Electric Vehicles," *IEEE Transactions on Industry Applications*, vol. PP, no. 99, pp. 1-1.