Single-Loop Control of Buck Power-Pulsation Buffer for AC-DC Converter System

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***Abstract*— Power converters interfacing single-phase ac and dc power sources and loads typically require an energy storage device to handle the double-line frequency power ripple. Among the active power storage solutions, called power-pulsation buffers (PPBs), the bidirectional buck topology is popular for its low component count and voltage stress, as well as good performance. However, existing control methods of the buck PPB are rather complex and typically employ at least two feedback loops. This paper presents a simplified, single-loop control of the buck PPB. To achieve the dc-bus-voltage-ripple magnitude below 3 % of the average bus voltage, the voltage feedback loop action was supplemented with current feedforward control. The performance of the proposed control was evaluated on a 1-kW PPB experimental prototype.**

Keywords—single-phase ac-dc converter; active power decoupling; power pulsation buffer; control

I. INTRODUCTION

In single-phase ac-dc applications, shown in Fig. 1(a), an energy storage device (ESD) is necessary to handle instantaneous imbalance of the input and output power that is illustrated in Fig. 1(b). Without the ESD, instantaneous input/output power imbalance causes a high double-line-frequency ripple across the load. The ESD, connected across the load, reduces/eliminates power imbalance by storing energy during periods when the input power is higher than the output power and supplying energy during periods when the input power is lower than the output power. Commonly, the ESD is implemented as bus capacitor C_B across the load, as shown in Fig. 2. Due to low double-line frequency, a high capacitance C_B is required which is typically implemented with relatively large aluminum electrolytic capacitors. Large size of electrolytic capacitors adversely affects power density and limits reliability of the entire power system since the life of aluminum electrolytic capacitors typically is shorter than the life of other system electronic components.

To reduce required bus capacitance C_B, an active energy storage device, called Power-Pulsation Buffer (PPB), can be used in parallel with C_B [1]-[11]. With the PPB, capacitance C_B can be considerably lower because of the more efficient utilization of energy storage components in the buffer. PPB can be implemented with any bidirectional topology. The bidirectional buck topology, shown in Fig. 2, is very popular due to its low component count and voltage stress, as well as good performance [1], [2], [4]-[11]. However, control of the buck PPB poses a major design challenge.

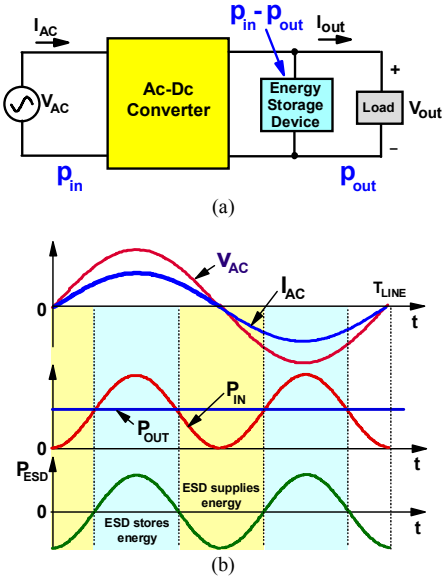


Fig. 1. Single-phase ac-dc power system. (a) High-level schematic. (b) Waveforms.

The control described in [1] has two loops, the inner loop for duty cycle calculation and the outer loop for regulating the average value of voltage V_{CS} on PPB energy-storage capacitor C_S. Specifically, the duty cycles of switches S1 and S2 are calculated by DSP based on sensed bus voltage V_B, energy-storage capacitor voltage V_{CS}, and double-line frequency current I_2. Drawbacks of this control are sensitivity of calculated duty cycle to sensing and processing errors and enormous computational resources needed for calculation of the duty cycles. Also the control in [1] is applicable only to the buck PPB which operates in the discontinuous conduction mode (DCM).

The control of the bus-voltage ripple in the buck PPB described in [2] is accomplished by means of a single feedback loop which regulates inductor current I_{LS}, shown in Fig. 2. The reference for the current feedback loop is a sinusoidal signal of the double-line frequency whose magnitude is proportional to the PFC stage load current. However, the waveform of actual inductor current I_{LS} has significant higher-order harmonics and,

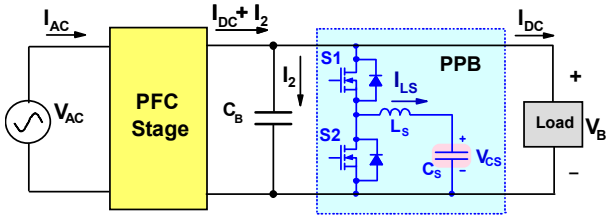


Fig. 2. Single-phase ac-dc power system with buck power pulsation buffer (PPB).

therefore, cannot tightly follow the sinusoidal reference. For this reason, the control in [2] requires relatively high values of bus capacitance C_B and PPB energy-storage capacitance C_S to achieve the low bus-voltage ripple. High values of capacitances C_B and C_S lead to low PPB power density.

The PPB ripple-reduction capability can be considerably increased by employing feedforward control, as demonstrated in [3] on the boost PPB used for the output-current-ripple reduction of an ac-dc LED driver. The boost PPB control in [3] employs the conventional two-loop control, where the inner loop regulates the average current of the boost inductor and the outer loop regulates the average value of voltage V_{CS}. In addition, the feedforward signal, proportional to the double-line frequency current and phase shifted by -90° is summed with the output signal of the inner-loop error amplifier. However, the feedback control, proposed in [3], is not applicable to the buck PPB.

Finally, a high-performance multi-loop control of the bidirectional buck PPB employed in grid-tied inverter applications is described in [4]. In this control, both feedback and feedforward controls are employed. The feedback control has an inner current loop for regulating inductor current I_{LS}. The reference of the inner current loop is the sum of the signals coming from several feedback loops and from the feedforward path. The signals coming from the feedback loops include (a) the scaled output of PI regulator which processes the error between the sensed bus voltage and the estimated V_B reference and (b) the scaled outputs of the resonant regulators tuned to the 2nd, 4th, and 6th harmonics of the line voltage, which process the sensed bus voltage. The signal coming from the feedforward path is the double-line frequency harmonic of the inductor current I_{LS}, calculated based on the sensed ac component of the inverter output power and sensed voltage V_{CS}. The control in [4] also has additional feedback loop, which regulates the average value of voltage V_{CS}. Due to complexity, digital implementation of the control in [4] requires a very powerful processor.

In this paper, the single-loop control of the buck PPB which directly regulates the bus voltage ripple, is proposed. To further reduce the bus voltage low-frequency ripple, the feedforward control which injects the signal proportional to the double-line frequency current into the voltage feedback loop at the input of the error amplifier, is added. Due to its simplicity, the proposed control does not require DSP implementation, i.e., it can be easily implemented with analog components. The performance of the proposed control is experimentally evaluated on a 1-kW, boost PFC stage designed to operate with 180-265-V line voltage, 50-Hz line frequency, and 400-V dc bus voltage. PPB inductor L_S operates in the continuous conduction mode (CCM) with its current changing polarity during each switching cycle, that makes possible zero-voltage-switching operation of the PPB switches. The PPB switching frequency is 120 kHz. The values of PPB capacitor C_S and inductance L_S are 60 μF and 50 μH, respectively.

II. PPB Operation with Single-Loop Voltage-Feedback Control

The block diagram of the proposed single-loop voltage-feedback control is shown in Fig. 3, where K_D is the resistive voltage divider gain and EA is the error amplifier. Fig. 4 shows voltage-feedback control loops of both PFC stage and PPB. According to Fig. 4, bus voltage V_B is regulated by two loops, namely, by the PFC stage voltage loop and by the PPB voltage loop. The purpose of the PFC stage voltage loop is to regulate the dc component of the bus voltage, whereas the purpose of the PPB loop is to attenuate low-frequency ac ripple of the bus voltage. It should be also noted that PPB is not capable of continuously regulating the bus voltage dc component since its only energy source is capacitor C_S. To avoid interaction of the voltage loops for regulation of the bus voltage dc component, the dc gain of the PPB loop should be much lower than that of the PFC stage voltage loop. Practically, this can be achieved by designing PPB error amplifier with finite dc gain which corresponds to the PPB loop gain shown in Fig. 5(a), or by sensing only ac component of the bus voltage which corresponds to the PPB loop gain shown in Fig. 5(b). The latter approach could be preferable since it does not require matching of voltage references V_{ref} and V_{ref1}, shown in Fig. 4, but at the same time requires addition of physical high-pass filter or software which

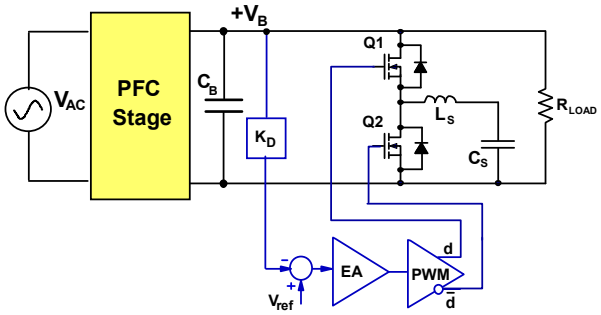


Fig. 3. Block diagram of PPB voltage feedback loop.

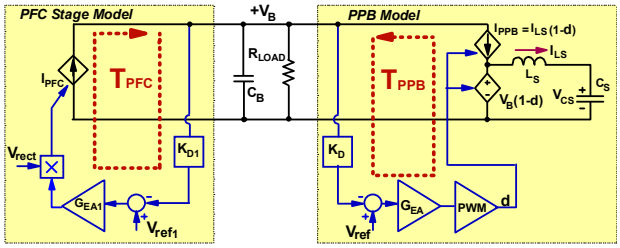


Fig. 4. PPB and PFC stage feedback control block diagram with voltage loops shown.

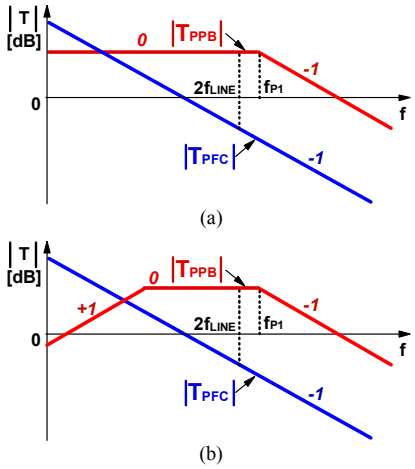


Fig. 5. Desirable low-frequency loop gains of PFC and PPB converters. (a) Both ac and dc components of the bus voltage are sensed by PPB. (b) Only ac component of the bus voltage is sensed.

removes dc component of sensed voltage V_B. It should also be noted that at double-line and higher frequencies PFC voltage loop effect on the bus voltage regulation can be completely neglected since, for conventional PFC stage design, its voltage loop bandwidth is selected well below the double-line frequency.

To design PPB control loop, its model has to be established. Derivation of the PPB large-signal averaged model is straightforward and leads to the equivalent circuit, shown in Fig. 6. In Fig. 6, PFC stage is represented by output current I_{PFC}, which is the sum of dc component I_{DC} and double-line frequency ac component I_2 whose peak value is equal to I_{DC}. The bus voltage dc component is determined by the PFC voltage loop as $V_{B(DC)} = I_{DC} \cdot R_{LOAD}$. It should be noted that current I_2, as well as PPB inductor current I_{LS} and capacitor voltage V_{CS} are time-dependent variables that vary widely within half-line period. Therefore, linearization of this model produces linear differential equations with periodic time-variable coefficients, which are not useful for control design. To obtain a linear time-invariant model, a quasi-static assumption is made. Specifically, it is assumed that for several adjacent switching cycles around time instant t_0, slow-changing variables, such as current I_2 and voltage V_{CS} are considered constant. Then, in the vicinity of time instant t_0, capacitor C_S is replaced with dc voltage source $V_{CS0} = V_{CS}(t_0)$ and ac current I_2 is replaced with dc current source $I_{20} = I_2(t_0)$, as shown in Fig. 7. The equivalent circuit in Fig. 7 can be linearized to obtain the PPB small-signal model. As time instant t_0 varies from zero to half-line period $T_{LINE}/2$, the values of voltage source V_{CS0} and current source I_{20} also vary. Therefore, PPB control loop should be designed stable at any time instant during half-line cycle.

During a half-line cycle it is sufficient to consider four time instants t_{0A}, t_{0B}, t_{0C}, and t_{0D}, shown in Fig. 8. At instants $t_{0A} = 0$ and $t_{0C} = T_{LINE}/4$, PPB current I_{PPB} is zero and voltage V_{CS} is at its minimum and maximum values, respectively. At instants t_{0B} and t_{0D}, voltage V_{CS} is equal to its average value and current I_{PPB} has the highest magnitude. At instant t_{0B} current I_{PPB} is positive and equal to load dc current I_{DC}, whereas at instant t_{0D} current

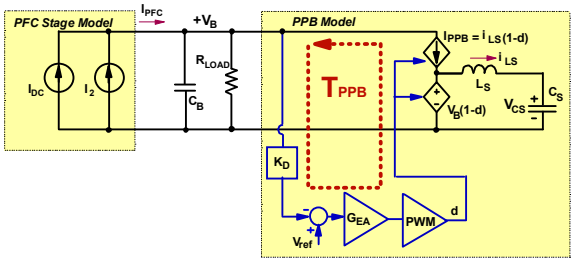


Fig. 6. PPB large-signal time-variant model.

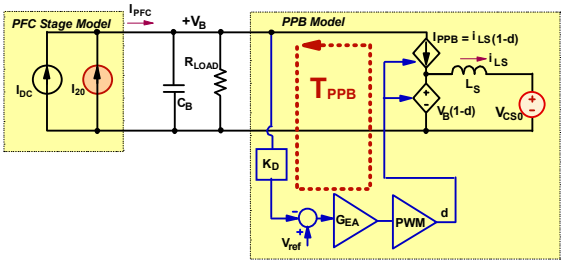


Fig. 7. PPB large-signal model at time instant t_0.

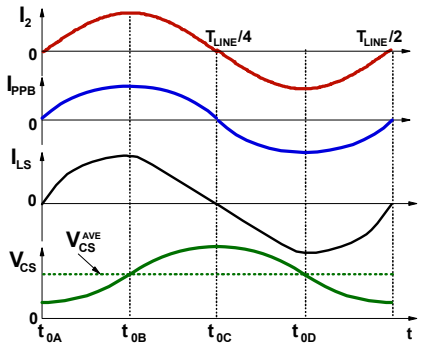


Fig. 8. Selection of time instants t_{0A}-t_{0D} for calculation of control-to-output transfer function $G_{VD}(s)$.

I_{PPB} is negative and equal to $-I_{DC}$. Linearization of the large-signal model in Fig. 7 at indicated time instants produces following equations for control-to-output transfer function $G_{vd}(s) = \hat{V}_B/\hat{d}$:

at instant t_{0A}

$$G_{vd}(s) = \frac{V_{B(DC)}}{1-D_{max}} \cdot \frac{1}{s^2/\omega_0{}^2 + s/\omega_0 Q + 1}, \quad (1)$$

at instant t_{0C}

$$G_{vd}(s) = \frac{V_{B(DC)}}{1-D_{min}} \cdot \frac{1}{s^2/\omega_0{}^2 + s/\omega_0 Q + 1}, \quad (2)$$

at instants t_{0B} and t_{0D}

$$G_{vd}(s) = \frac{V_{B(DC)}}{1-D_{ave}} \cdot \frac{1 \pm s/2\pi f_{z(vd)}}{s^2/\omega_0{}^2 + s/\omega_0 Q + 1}, \quad (3)$$

where resonant frequency $\omega_0 = (1-D)/\sqrt{L_S \cdot C_B}$,

quality factor $Q = (1-D)^2 R_{LOAD}/(\omega_0 \cdot L_S)$,

and zero frequency $f_{z(vd)} = (1-D)^2 R_{LOAD}/(2 \cdot \pi \cdot L_S)$.

In the numerator of (3), a left-half-plane zero corresponds to instant t_{0B} when PPB operates in the buck mode ($I_{LS} > 0$), whereas a right-half-plane zero corresponds to instant t_{0D} when PPB operates in the boost mode ($I_{LS} < 0$). Duty cycles D_{min}, D_{ave}, and D_{max} correspond to the maximum, average, and minimum values of voltage V_{CS}, respectively. It should be noted that in (1)-(3) a zero related to the ESR of capacitor C_B is neglected, since its frequency is considered much higher than the PPB loop bandwidth.

Then, the PPB loop gain is calculated as

$$T_{PPB} = K_D \cdot G_{EA}(s) \cdot F_M \cdot G_{VD}(s), \quad (4)$$

where F_M is the PWM gain. Asymptotic frequency responses of PPB power stage and error amplifier transfer functions and loop gain are plotted in Fig. 9. To design error amplifier transfer function $G_{EA}(s)$, it is assumed that zero frequency $f_{z(vd)}$ is much higher than PPB loop bandwidth. In this case, proposed error amplifier has two poles and two zeroes, as shown in Fig. 9. EA pole f_{P1} is placed 2-4 times higher than double-line frequency. EA zeroes f_{Z1} and f_{Z2} are placed between frequency f_{P1} and loop crossover frequency f_C, as shown in Fig. 9. EA pole f_{P2} is placed above crossover frequency f_C. The major trade-off of the EA design is to maximize the loop gain at frequencies of even harmonics of the line frequency, which provides the highest attenuation of the bus voltage low-frequency ripple, while keeping the loop stable. For the PPB power stage specified in Introduction, the EA transfer function was designed to have dc gain of 3.2, poles at 200 Hz and 22 kHz, and two zeroes at 600 Hz.

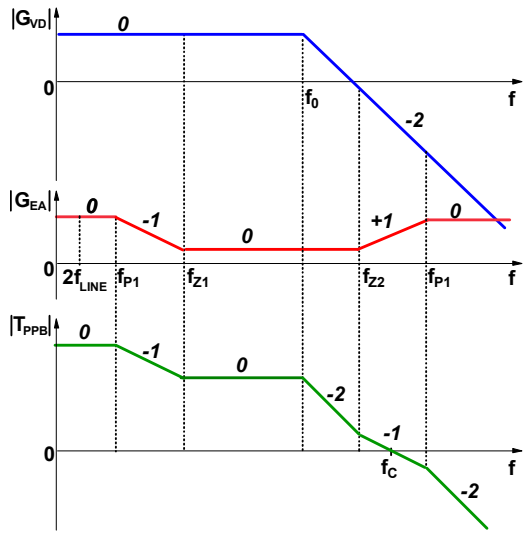


Fig. 9. Asymptotic frequency responses of transfer functions $G_{VD}(s)$, $G_{EA}(s)$, and loop gain $T_{PPB}(s)$.

Resulting loop gain T_{PPB} at time instants t_{0A}-t_{0D} is plotted in Fig. 10 for minimum and maximum V_{CS} values of 80 V and 320 V, respectively. The loop bandwidth, stability margins, and the loop gain magnitude at $2f_{LINE}$ frequency are presented in Table I. Table I shows that at all four time instants the loop has wide bandwidth and adequate stability margins. However, despite the wide bandwidth, the loop gain values at the double-line frequency at time instants t_{0B}-t_{0D} are relatively low. With these values, high attenuation of the bus voltage ripple cannot be expected. The bus voltage waveform, simulated at 1-kW load with only voltage feedback loop, has peak-to-peak ripple of 10.8 % with respect to the bus voltage dc component. If there was no PPB at PFC stage output and the dc bus capacitance was a sum of C_B and C_S, the V_B peak-to-peak ripple would be 39 %. This means that the voltage feedback control achieves only moderate reduction of the bus voltage ripple. To further decrease the bus voltage ripple, the PPB control performance is enhanced by employing the feedforward control which is presented in the next Section.

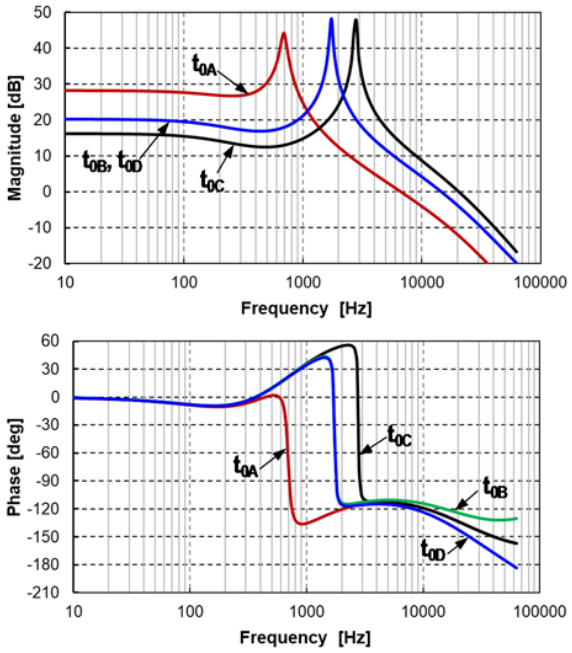


Fig. 10. PPB loop gain Bode plots for time instants t_{0A}-t_{0D}.

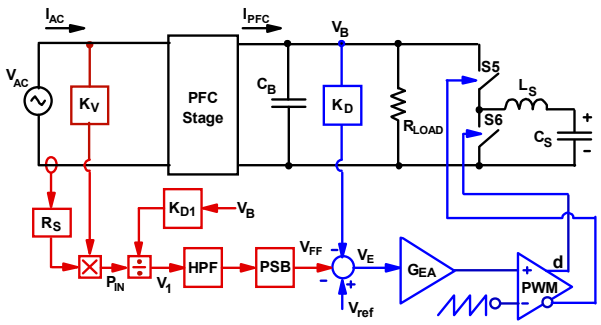
TABLE I. BANDWIDTH, STABILITY MARGINS, AND LOOP GAIN VALUE AT DOUBLE-LINE FREQUENCY

Time Instant	Band-width	Phase Margin	Gain Margin	$\lvert T_{PPB}\rvert$ at $2 \cdot f_{LINE}$
t_{0A}	6.7 kHz	66°	> 36 dB	27.7 dB
t_{0B}	14.7 kHz	60°	17.7 dB	19.6 dB
t_{0C}	20.6 kHz	46°	> 24 dB	15.5 dB
t_{0D}	14.7 kHz	47°	18.6 dB	19.6 dB

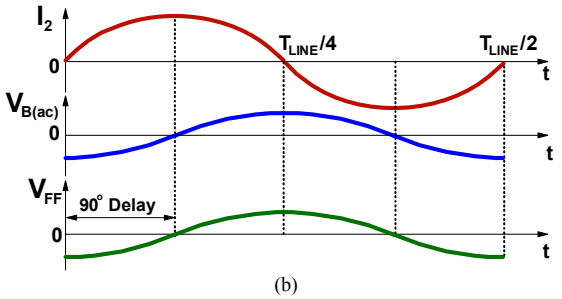
III. PPB Operation with Feedback and Feedforward Control

The entire PPB control block diagram is shown in Fig. 11(a) with the proposed feedforward control shown in red color, whereas key PPB waveforms during one half-line cycle are shown in Fig. 11(b). The feedforward control improves performance of the feedback loop by increasing error signal V_E without increasing loop gain T_{PPB} and, therefore, without deteriorating the loop stability margins. For proper feedforward control, feedforward voltage V_{FF} should increase the error signal of the feedback loop, i.e., be in phase with bus voltage ac component $V_{B(ac)}$, as shown in Fig. 11(b). The desired feedforward voltage waveform is obtained from double-line frequency current I_2 waveform by delaying it 90 degrees. Fig. 11(a) shows that double-line frequency current I_2 waveform is calculated as a product of sensed ac line voltage $K_V \cdot V_{AC}$ and sensed line current $R_S \cdot I_{AC}$ waveforms, divided by sensed bus voltage $K_{D1} \cdot V_B$. Then, the divider output signal is processed by high-pass filter HPF to remove its dc component and by phase-shift block PSB which provides -90° phase shift of the feedforward signal at the double-line frequency. Resulting PSB output signal V_{FF} finally is summed with feedback signal $K_D \cdot V_B$. One simple analog implementation of high-pass filter and phase-shift block is shown in Fig. 12, where HPF is implemented by R_1, C_1 network and PSB is implemented by R_2, C_2 network. The combined transfer function of these two blocks is

$$G_1(s) = \frac{V_{FF}}{V_1} = K_1 \cdot \frac{s/(2\pi \cdot f_{c1})}{(1+s/(2\pi \cdot f_{c1})) \cdot (1+s/(2\pi \cdot f_{c2}))}, \quad (5)$$



(a)



(b)

Fig. 11. Block diagram and key waveforms of proposed PPB control.

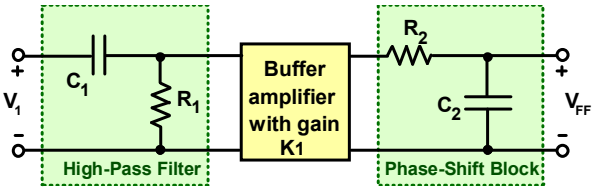


Fig. 12. Simple implementation of high-pass filter and phase-shift block.

where $f_{c1} = 1/(2\pi \cdot R_1 \cdot C_1)$ and $f_{c2} = 1/(2\pi \cdot R_2 \cdot C_2)$ are corner frequencies of HPF and PSB transfer functions, respectively.

Based on Fig. 11(a) and equation (5), the waveform of feedforward signal V_{FF} is calculated as

$$V_{FF}(t) = A_{FF} \cdot cos(4\pi \cdot f_{LINE} \cdot t + \alpha - \beta), \quad (6)$$

where $$\alpha = \pi/2 - tan^{-1}(2 \cdot f_{LINE}/f_{c1}), \quad (7)$$

$$\beta = tan^{-1}(2 \cdot f_{LINE}/f_{c2}), \quad (8)$$

and magnitude A_{FF} of the feedforward signal is

$$A_{FF} \approx \frac{R_S \cdot K_V \cdot K_1}{K_{D1}} \cdot \frac{V_{AC}^{rms} \cdot I_{AC}^{rms}}{V_B^{dc}} \cdot \frac{f_{C2}}{2f_{LINE}}. \quad (9)$$

According to (7), to introduce phase lead below 5° at the double-line frequency, corner frequency f_{c1} is selected at least 11 times below $2f_{LINE}$. According to (8), to provide phase lag above 85° at the double-line frequency, corner frequency f_{c2} is selected at least 11 times below $2f_{LINE}$. Once corner frequencies f_{c1} and f_{c2} were selected, the model of the PPB together with the PFC stage was simulated for different feedforward signal magnitudes A_{FF} to obtain the bus voltage ripple waveform. The simulation results are plotted in Figs. 13 and 14. Fig. 13 shows the dependence of the bus voltage peak-to-peak ripple on the feedforward signal magnitude. As magnitude A_{FF} increases from zero to 260 mV, the bus voltage ripple decreases from 43.2 to 9.1 V_{PP}. However, further increase of the feedforward signal magnitude causes the bus voltage ripple to increase. Such behavior can be explained by analysis of the bus voltage 2nd harmonic magnitude and phase which are plotted versus magnitude A_{FF} in Fig. 14. It should be remembered that the proposed feedforward control attenuates the bus voltage ripple by providing zero phase shift between the feedforward signal and the second harmonic of the bus voltage. As Fig. 14 shows, the feedforward control decreases the second harmonic amplitude from 21.5 V_{PEAK} at $V_{FF} = 0$ to 1.05 V_{PEAK} at $V_{FF} = 260$ mV, but at the same time the phase of the 2nd harmonic increases from 5° to 42°. When voltage V_{FF} increases further, the feedforward signal and the bus voltage 2nd harmonic rapidly become completely out of phase that makes the feedforward control no longer effective. Also the proposed feedforward control can reduce only the 2nd harmonic of the bus voltage. As the 2nd bus voltage harmonic is attenuated by the

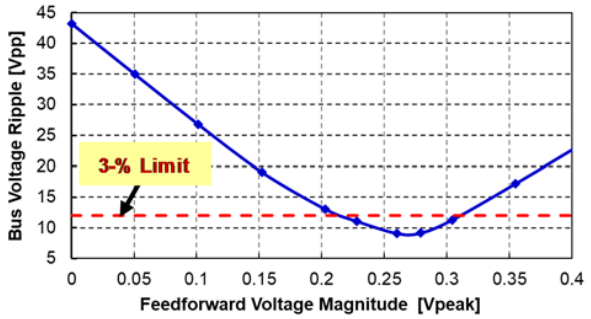


Fig. 13. Bus voltage ripple magnitude versus feedforward voltage magnitude. f_{C2} = 21.3 Hz; P_{LOAD} = 1 kW.

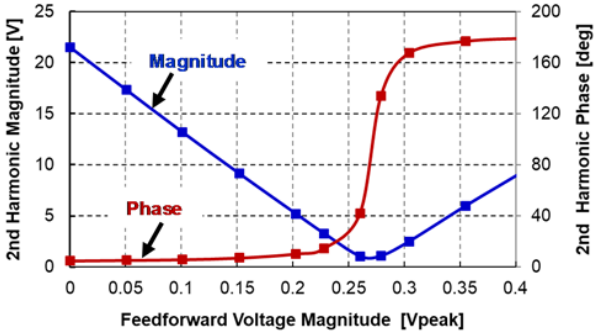
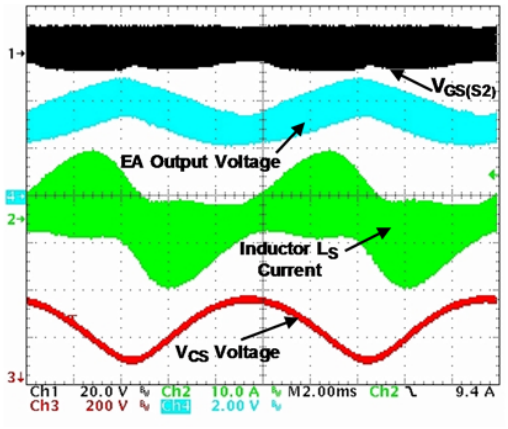


Fig. 14. Bus voltage 2nd harmonic magnitude and phase versus feedforward voltage magnitude. f_{C2} = 21 Hz; P_{LOAD} = 1 kW.

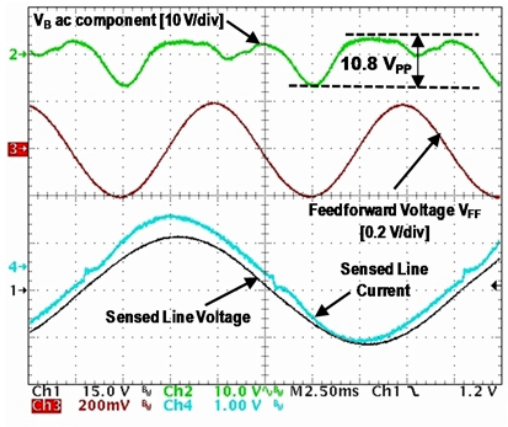
control, the higher-order harmonics limit further decrease of the bus voltage ripple. According to Fig. 13, the PPB design meets 3-% bus voltage ripple when the feedforward voltage is selected in the range of 0.22-0.31 V.

IV. Experimental Results

Experimental setup included 1-kW server ac-dc power supply with two 470-µF/450V aluminum bulk capacitors at the PFC stage output and the PPB prototype. Aluminum bulk capacitors were replaced with polypropylene 450-V capacitors whose total capacitance was 42 µF. The 120-kHz PPB prototype had 60-µF energy-storage polypropylene capacitor C_S and 50-µH inductor L_S. Switches S5 and S6 were implemented with Infineon IPW65R080CFD MOSFETs. To simplify implementation, signal divider of the feedforward control was replaced with the constant gain block whose gain is reciprocal of the bus average voltage. Measured waveforms of the PPB operation at 1-kW load power are shown in Figs. 15(a) and (b), whereas waveforms at 500-W and 100-W loads are shown in Figs. 16(a) and (b), respectively. The waveform of inductor current I_{LS} in Fig. 15(a) indicates that the current changes its direction every switching cycle and, therefore, creates condition for ZVS operation of switches S1 and S2. Fig. 15(b) shows output signals of the line voltage and current sensors and feedforward voltage V_{FF} which has double-line frequency. Fig. 15(b) also shows the 10.8-V_{PP} magnitude of the bus voltage ripple waveform that is less than 3 % of the bus voltage dc value. Voltage V_{CS} across the energy-storage capacitor varies in the range from 88 V to 376 V that indicates excellent utilization of capacitor energy.



(a)

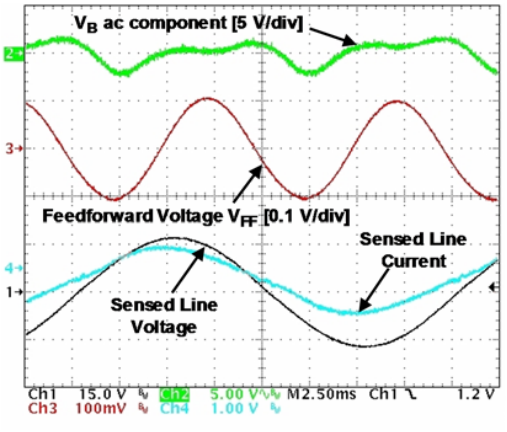


(b)

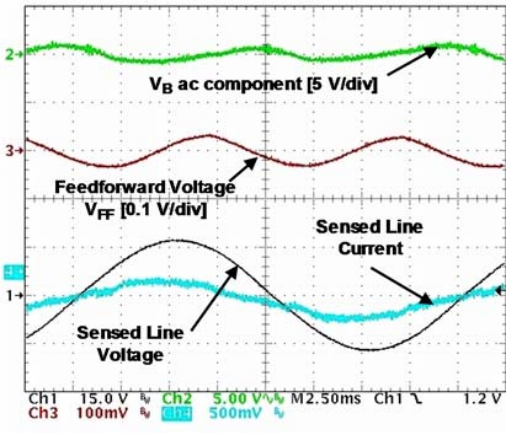
Fig. 15. Measured PPB waveforms at 1-kW load. Time scale is 2.5 ms/div.

Experimental data measured in the entire PPB load range is shown in Table II. As the load power decreases, Fig. 15(b) and Figs. 16(a) and (b) indicate reduction of the feedforward voltage magnitude. However, current ripple second harmonic I_2 also decreases and overall effect of these two factors on the bus voltage ripple makes it decrease monotonically, as indicated in Table II. The data in Table II also demonstrates that, with the load power decrease, the range of voltage V_{CS} becomes more narrow as PPB stores and supplies less energy.

Since, for selected feedforward control implementation, the magnitude and the phase of feedforward voltage V_{FF} depend on line frequency, the effect of the line frequency on the bus voltage ripple and the range of voltage V_{CS} on the PPB energy-storage capacitor was measured and the results are shown in Table III for the worldwide line-frequency range. The highest bus voltage ripple corresponds to the minimum line frequency of 47 Hz for two reasons. First, at the minimum line frequency, PPB capacitor C_S has to process the maximum energy during its charge/discharge cycle. Therefore, at 47-Hz frequency, the PPB control should provide the widest variation of the duty cycle, but the duty cycle variation is limited by feedback and feedforward gains of the control. Second, at 47-Hz line frequency, the



(a)



(b)

Fig. 16. Measured PPB waveforms at (a) 500-W load and (b) 100-W load. Time scale is 2.5 ms/div.

TABLE II. MEASURED BUS VOLTAGE RIPPLE AND VOLTAGE V_{CS} RANGE VERSUS LOAD

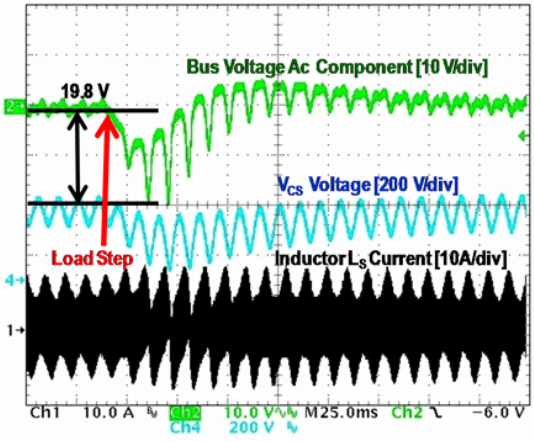
Load Power [W]	1000	750	500	250	100	0
Bus Voltage Ripple [V_{PP}]	10.8	6.6	4.4	2.9	2.2	2.1
V_{CS} Voltage Range [V]	88-376	136-352	168-328	200-299	216-288	232-272

impedance of bus capacitor C_B is the highest, whereas the magnitude of the PFC stage output current ripple does not depend on the line frequency. Therefore, at 47 Hz the voltage across the bus capacitor is the highest. With the line frequency increase, the bus voltage ripple decreases due to reduced demand to the PPB control response and to reduced impedance of the bus capacitor. Also V_{CS} voltage range becomes narrower, since at higher line frequency PPB processes less energy during shorter half-line period.

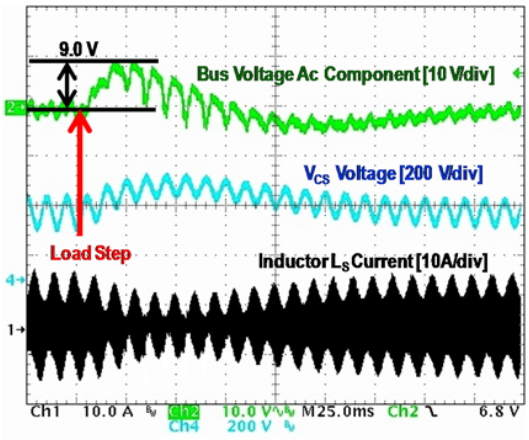
TABLE III. MEASURED BUS VOLTAGE RIPPLE AND V_{CS} RANGE VERSUS LINE FREQUENCY AT 1-KW LOAD

Line Frequency [Hz]	47	50	53	57	60	63
Bus Voltage Ripple [V_{PP}]	11.7	10.8	10.2	9.50	9.10	8.90
V_{CS} Voltage Range [V]	74-382	88-376	95-370	106-362	113-304	119-299

Waveforms of the transient response of the PFC stage with PPB to 12-A load current step-up and step-down are shown in Figs. 17(a) and (b), respectively. For comparison, load transient response was also measured for the setup where PPB was replaced with two 390-µF aluminum bus capacitors. Their total value was selected to provide approximately the same steady-state bus voltage ripple as the experimental PPB provides. In the case of the load step-up, the bus voltage undershoot for the PFC



(a)



(b)

Fig. 17. Measured PPB transient response to (a) 12-A load current step-up and (b) 12-A load current step-down. Time scale is 25 ms/div.

stage with aluminum capacitors was 6.0 V, whereas for the PFC stage with PPB the undershoot was 19.8 V. It should be noted that the load transient response is determined not by the PPB performance, but mostly by the value of the bus capacitor and the performance of the PFC stage voltage loop which has relatively low bandwidth of 12 Hz. Both PFC stage and PPB supply energy to meet the increased load demand. Namely, the PFC stage delivers energy from the ac line, whereas the PPB delivers energy from energy-storage capacitor C_S. PPB contributes to significantly higher undershoot due to its relatively slow control response which is attributed to two factors. First, the PPB feedback loop response is slow due to the relatively low loop gain at low frequencies. Second, the high time constants of HPF and PSB blocks slow down the feedforward path response. Fig. 17(a) indicates the specific effect of the PPB control on the transient response, namely, the increased bus voltage ripple during V_B drop after the load step-up. The increased transient bus voltage ripple also contributes to higher bus voltage undershoot in the PFC stage with PPB.

In the case of the load step-down, the bus voltage overshoot for the PFC stage with aluminum capacitors was 4.8 V, whereas for the PFC stage with PPB the undershoot was 9.0 V. The reasons for higher voltage overshoot for the PFC stage with PPB during load step-down are the same as those mentioned for the load step-up transient.

Finally, Fig. 18 shows measured efficiency of the PFC stage with aluminum bulk capacitors and of the PFC stage with PPB. Operation of the PFC stage with PPB at full load causes efficiency drop of 0.65 % or loss increase of 7.5 W with respect to the PFC stage operation with aluminum capacitors.

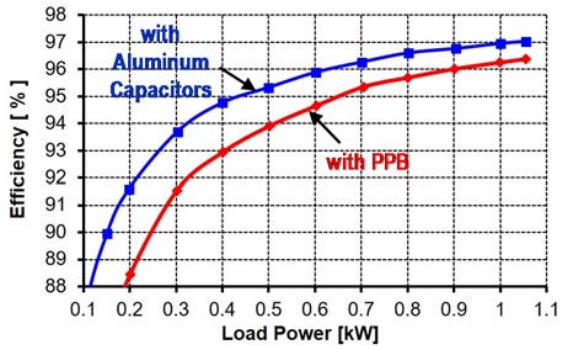


Fig. 18. Measured PFC stage efficiency with aluminum bus capacitors and with PPB.

V. SUMMARY

Single-phase ac-dc converters require an energy storage device to handle the double-line frequency bus voltage ripple. Among the active energy storage solutions, the bidirectional buck topology is popular for its low component count and voltage stress, as well as good performance. However, existing control methods of the buck PPB are rather complex and typically employ multiple feedback loops. This paper presents a simplified, single-loop control of the buck PPB, combined with the current feedforward control. Guidelines for the proposed control design were presented. The control performance was evaluated on a 1-kW PPB experimental prototype. The prototype achieved the dc bus voltage ripple below 3 % of the average bus voltage.

REFERENCES

[1] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage", IEEE Transactions on Power Electronics, vol. 26, no. 5, May 2011, pp.1430-1443.

[2] K.-H. Chao, P.-T. Cheng, and T. Shimizu, "New Control Methods for Single Phase PWM Regenerative Rectifier with Power Decoupling Function," in Proc. Power Electron. Drive Syst. Conf., Nov. 2009, pp. 1091–1096.

[3] Y. Yang, X. Ruan, L. Zhang, J. He, and Z. Ye, "Feed-Forward Scheme for an Electrolytic Capacitor-Less AC/DC LED Driver to Reduce Output Current Ripple ", IEEE Transactions on Power Electronics, vol. 29, no. 10, Oct. 2014, pp. 5508-5517.

[4] D. Neumayr, D. Bortis, and J.W. Kolar, "Ultra-Compact Power Pulsation Buffer for Single-Phase Dc/Ac Converter Systems", in Proc. 2016 IEEE Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), May 2016, pp. 1-10.

[5] D. Bortis, D. Neumayr, and J.W. Kolar," ηρ-Pareto Optimization and Comparative Evaluation of Inverter Concepts considered for the Google Little Box Challenge ", in Proc. 2016 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL), 2016, pp. 1-5.

[6] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active Power Decoupling for High-Power Single-Phase PWM Rectifiers", IEEE Transactions on Power Electronics, vol. 28, no. 3, Mar. 2013, pp.1308-1319.

[7] A. Morsy, M. Bayern, P. Enjeti, "High Power Density Single Phase Inverter Using GaN FETS and Active Power Decoupling for Google Little Box Challenge", in Proc. 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2015, pp. 323-327.

[8] Y. Tang, and F. Blaabjerg, "Power Decoupling Techniques for Single-Phase Power Electronics Systems – An Overview", in Proc. 2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 2541-2548.

[9] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC Active Power Decoupling Circuits for Second-Order Harmonic Mitigation in Kilowatt-Scale Single-Phase Inverters", IEEE Journal of Emerging and Selected Topics In Power Electronics, Vol. 4, No. 1, Mar. 2016, pp. 15-25.

[10] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of Active Power Decoupling Topologies in Single-Phase Systems", IEEE Transactions on Power Electronics, vol. 31, no. 7, Jul. 2016, pp. 4778-4794.

[11] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de A. R. Correa, "Low-Frequency Power Decoupling in Single-Phase Applications: A Comprehensive Overview", IEEE Transactions on Power Electronics, vol. 32, no. 4, Apr. 2017, pp. 2892-2912.