A Novel Zero-Sequence Current Elimination PWM Scheme for an Open-end Winding Motor Drive with Dual Two-Level Inverter

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***Abstract*—This paper introduces a novel pulse width modulation (PWM) scheme for an open-end winding motor drive with dual two-level three–phase inverter which can achieve zero sequence current (ZSC) elimination effect in ideal condition. Based on normal SPWM modulation scheme with appropriate phase-shift, the common mode voltage (CMV) in different inverters can keep the same and cancel out with each other which can realize the zero sequence voltage (ZSV) elimination effect finally. In this condition, the dual inverters can share the same DC power and simplify the structure of drive system. The phase current of the novel scheme can reach the maximum value as same as other ZSC elimination schemes while the THD can be reduced. In addition, the double frequency effect of proposed method can also decrease the requirement of DC side capacitor. To verify the analysis, both simulation and experimental results are presented to validate the superiority of proposed method.**

***Index Terms*—dual two-level inverter, common mode voltage, zero sequence current, phase shift**

I. Introduction

PWM-inverter-driven ac motors have become common in variable speed applications due to various advantages, such as high efficiency, superior dynamic performance and low harmonic distortion. Compared to conventional three-phase star-connected winding motor drive, open-end winding ac motor has better fault-tolerant capability because each phase current can be controlled separately [1] [2]. Moreover, the dual inverter fed open-end winding motor has higher DC bus utilization and is favorable for the occasion that motor voltage is higher than DC link voltage. With this advantage, open-end winding ac motor drives are widely used in electric vehicles [3] [4], wind generation systems [5] [6] and aircraft starter-generator [7]. In addition, conventional dual two-level inverter can output three level phase voltage which has similar effect with three-level inverter [8], but it has obvious advantages–the simple structure without neutral point clamping diode, the absence of neutral point fluctuation, and the flexibility and redundancy of space vector combinations [9].

The dual inverter usually can be fed by two isolated DC powers [10] [11] or single DC power [9] [12]. The two isolated DC powers can block the zero sequence path in open-end winding motor and suppress the zero sequence current (ZSC), the structure is shown in Fig. 1(a). Though this method can be adopted, the two isolated DC-powers lead the system bulky and increase the cost. So in some occasions with the requirement of power density and cost, the single DC power fed dual inverter is preferred. When the single DC power is utilized shown in Fig. 1(b), the potential ZSC will be generated and consequently causing unwanted power losses, torque ripple which degrades the system performance [13]. For open-end winding induction motor, the zero sequence voltage (ZSV) which is the source of ZSC is mainly caused by the difference of CMVs between two inverters. If the CMVs which is decided by the modulation scheme keep identical in every switching cycle, the ZSC can be theoretically controlled to zero [9][14]. In open-end winding permanent magnet synchronous motor (PMSM), the ZSV in back electromotive force (EMF) is another major disturbance source. In view of this situation, the freedom of zero vector redistribution should be utilized and ZSC regulator should be added into the control system [15]-[18].

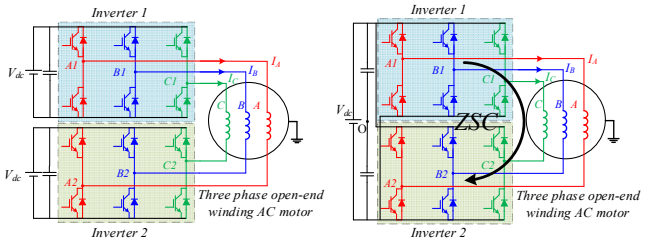


Fig. 1. The structure of dual two-level inverter fed open-end winding AC motor: (a) with two isolated DC-power, (b) with common DC-power

Though the ZSV elimination schemes based on two-level inverter modulation schemes can be easily implemented, like the traditional SVPWM (space vector PWM) and DPWM (discontinuous PWM) with PWM signal rotation [19] [20], the performance is not as good as unipolar double frequency SPWM, because the freedom for the dual inverter is not fully utilized. But convention unipolar double frequency SPWM keep the PWM signals symmetric and the ZSV still exist, so the modified method should be considered to eliminate the ZSV.

Base on the above analysis, the novel modulation scheme based on unipolar double frequency SPWM and phase-shift is proposed. The rest of this paper is organized as follows: in part

II, the definition of ZSV is first introduced, then the principle of conventional ZSV elimination schemes are investigated. On the basis of above analysis, the novel PWM method to eliminate ZSV for the dual two-level inverter is introduced in part III. The comparison of the conventional and novel PWM schemes are done by simulation in part IV, and the experimental results are presented in part V. Conclusions are made in part VI finally.

II. CONVENTIONAL PWM METHODS FOR DUAL TWO-LEVEL INVERTERS

A. The Analysis of ZSV and CMV in Dual Two-Level Inverter

For the dual two-level three-phase inverter fed open-end winding AC motor, the pole voltage of phase–legs can switch from $V_{dc}/2$ to $-V_{dc}/2$ with the DC link voltage of V_{dc}. In this case, the phase voltage can switch in V_{dc}, 0, $-V_{dc}$ which is similar with three-level inverter.

Generally, the CMV of inverter is the instantaneous average voltage of all phase. So the CMV of inverter1 and inverter2 can be defined in (1) and (2), where the V_{cm1} and V_{cm2} are the instantaneous CMV of two inverters correspondingly, and V_{A1O}, V_{A2O}, V_{B1O}, V_{B2O}, V_{C1O}, V_{C2O} are the output instantaneous pole voltages.

$$V_{cm1}=\frac{1}{3}\left(V_{A1O}+V_{B1O}+V_{C1O}\right) \tag{1}$$

$$V_{cm2}=\frac{1}{3}\left(V_{A2O}+V_{B2O}+V_{C2O}\right) \tag{2}$$

For dual two-level inverter fed open-end winding AC motor, the difference between V_{cm1} and V_{cm2} is the source of ZSC [21], namely the ZSV which can be defined in (3).

$$\begin{aligned} V_{ZSV}&=V_{cm1}-V_{cm2}\\ &=\frac{1}{3}\left[\left(V_{A1O}+V_{B1O}+V_{C1O}\right)-\left(V_{A2O}+V_{B2O}+V_{C2O}\right)\right]\\ &=\frac{1}{3}\left[\left(V_{A1O}-V_{A2O}\right)+\left(V_{B1O}-V_{B2O}\right)+\left(V_{C1O}-V_{C2O}\right)\right]\\ &=\frac{1}{3}\left(V_{A1A2}+V_{B1B2}+V_{C1C2}\right) \end{aligned} \tag{3}$$

where V_{ZSV} is ZSV, the V_{A1A2}, V_{B1B2}, V_{C1C2} are the instantaneous output phase voltages of three windings correspondingly. The even number of the total phase-legs makes the ZSV possible to be zero.

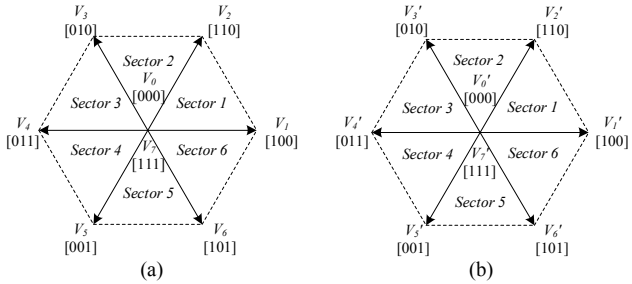


Fig. 2. The space voltage vectors of individual inverters: (a) inverter 1, (b) inverter 2

For dual two-level inverter, each of inverter can generate the same eight space voltage vectors shown in Fig. 2(a) and (b). The eight space voltage vectors have four CMV values totally, the peak value are $V_{dc}/2$ and $-V_{dc}/2$ corresponding to the voltage vectors V_7[111] and V_0[000], the voltage vectors V_1[100], V_3[010] and V_5[001] have the same CMV value of $-V_{dc}/6$, and the voltage vectors V_2[110], V_4[011] and V_6[101] have the same CMV value of $V_{dc}/6$.

Based on the combination of eight voltage vectors in one inverter, the number of space voltage vectors for dual two-level inverter is 2^6=64, and the combination of different voltage vectors can generate seven kinds of ZSV value. The ZSV of total sixty-four voltage vector combinations can be calculated and shown in Table. I.

TABLE I
RESULTED ZSV OF DIFFERENT VECTOR COMBINATIONS

Combinations of switching states	ZSV
V_{70}'	V_{dc}
V_{71}', V_{73}', V_{75}', V_{20}', V_{40}', V_{60}'	$2V_{dc}/3$
V_{72}', V_{74}', V_{76}', V_{10}', V_{30}', V_{50}', V_{21}', V_{23}', V_{25}', V_{41}', V_{43}', V_{45}', V_{61}', V_{63}', V_{65}'	$V_{dc}/3$
V_{00}', V_{11}', V_{22}', V_{33}', V_{44}', V_{55}', V_{66}', V_{77}', V_{24}', V_{26}', V_{42}', V_{46}', V_{62}', V_{64}', V_{13}', V_{15}', V_{35}', V_{31}', V_{51}', V_{53}'	**0**
V_{27}', V_{47}', V_{67}', V_{01}', V_{03}', V_{05}', V_{12}', V_{32}', V_{52}', V_{14}', V_{34}', V_{54}', V_{16}', V_{36}', V_{56}'	$-V_{dc}/3$
V_{17}', V_{37}', V_{57}', V_{02}', V_{04}', V_{06}'	$-2V_{dc}/3$
V_{07}'	$-V_{dc}$

For example, V_{15}' means utilizing the output voltage vector V_1[100] of inverter 1 and output voltage vector V_5'[001] of inverter 2 to synthesize the zero ZSV voltage vector because both of two inverters generate the same CMV of $-V_{dc}/6$. In addition, from Table I, it can be seen that there are total twenty voltage vector combinations which can realize the zero ZSV. These synthesized voltage vector can be divided into two kinds: the zero voltage vectors which have no contribution to synthesis of reference vector, and the effective voltage vectors which can be used to synthesize the reference vector. The all chosen zero ZSV voltage vectors in dual two-level inverter and the relationship to basic two-level inverters voltage vectors can be drawn and shown in Fig. 3. The effective synthesized voltage vectors are the thick blue arrows. Zero ZSV can be realized in every switching period if taking suitable arrangement of these special voltage vectors.

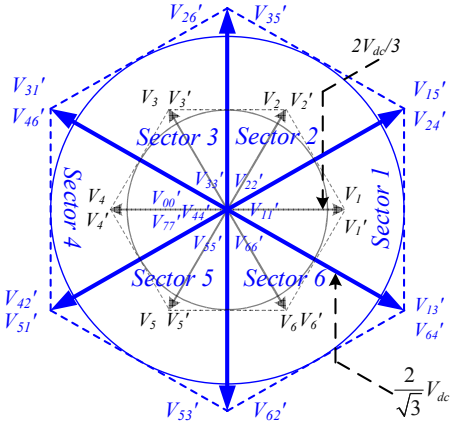


Fig. 3. The zero ZSV voltage vectors for dual-inverter

B. The Principle of Conventional ZSV Elimination PWM Scheme

The conventional ZSV elimination modulation scheme for dual-inverter can be deduced from normal SVPWM and DPWM schemes for two-level three-phase inverter. The principle is based on exchanging the PWM signals sequence for different inverters. This method can promise inverter 1 and inverter 2 always taking the same PWM signals which leads to the identical CMVs of the two inverters.

Taking sector 1 of inverter 1 for example, when DPWM scheme is adopted, the duty cycle of phase-leg A_1 is maximum and clamped to positive dc bus shown in Fig. 4(a). At the same time, by exchanging the sequence of PWM signals for inverter 1 to generate the corresponding PWM signals for inverter 2, then the duty cycle of phase-leg B_2 can keep the maximum and clamped to positive dc bus shown in Fig. 4(b). In this manner, the CMVs of different inverters can keep identical and the ZSV can be eliminated in every switching cycle. The detailed comparison for individual inverters is shown in Fig. 4. When considering the normal SVPWM scheme, the principle as well as effect are similar with DPWM.

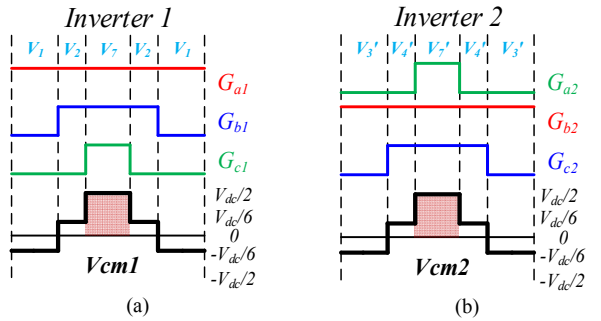


Fig. 4. The PWM signals and CMV for individual inverters with DPWM scheme: (a) inverter 1, (b) inverter 2

The principle of above ZSV elimination methods can be explained clearly with the principle of space voltage vector synthesis. According to the PWM signals shown in Fig. 4, the PWM signals G_{a1} and G_{b2} have the same maximum duty cycle which decides the direction of synthetic voltage vectors for inverter 1 V_{ref1} and inverter 2 V_{ref2}. So the V_{ref1} and V_{ref2} can be deduced where V_{ref1} is in sector 1 and V_{ref2} is in sector 3 shown in Fig. 5.

Considering the output average phase-leg voltage, the above schemes satisfy the equations:

$$\begin{cases} V_{A1O} = V_{B2O} \\ V_{B1O} = V_{C2O} \\ V_{C1O} = V_{A2O} \end{cases} \tag{4}$$

The space voltage vectors V_{ref1} and V_{ref2} can be represented as:

$$\overrightarrow{V_{ref1}} = V_{A1O} + V_{B1O}e^{j2\pi/3} + V_{C1O}e^{-j2\pi/3} \tag{5}$$

$$\begin{aligned} \overrightarrow{V_{ref2}} &= V_{A2O} + V_{B2O}e^{j2\pi/3} + V_{C2O}e^{-j2\pi/3} \\ &= V_{C1O} + V_{A1O}e^{j2\pi/3} + V_{B1O}e^{-j2\pi/3} \\ &= e^{j2\pi/3}\left(V_{C1O}e^{-j2\pi/3} + V_{A1O} + V_{B1O}e^{j2\pi/3}\right) \\ &= e^{j2\pi/3}\overrightarrow{V_{ref1}} \end{aligned} \tag{6}$$

So the included angle of the two voltage vectors is 120°, and the output resultant space vector V_{ref} can be expressed as:

$$\overrightarrow{V_{ref}} = \overrightarrow{V_{ref1}} - \overrightarrow{V_{ref2}} = \overrightarrow{V_{ref1}} - e^{j2\pi/3}\overrightarrow{V_{ref1}} = \sqrt{3}e^{-j\pi/6}\overrightarrow{V_{ref1}} \tag{7}$$

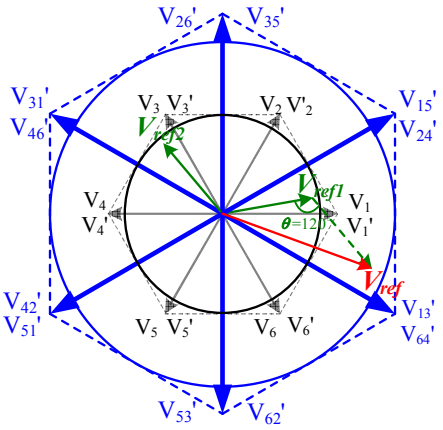


Fig. 5. Reference voltage combination with PWM signals changing sequence

Though the phase-leg voltage are non-sinusoidal by injecting the zero sequence component which has the ability to increase modulation index range, the zero sequence component can be cancelled out with the subtractive property and the phase voltage can still keep sinusoidal with the peak value of $\sqrt{3}$ times of pole voltage which is the value of V_{dc}. So the actually maximal modulation index value is reduced from 1.15 to 1 which is the maximum modulation index in dual inverter topology with single DC power. The SVPWM scheme which injects different zero sequence component also have the same modulation index range.

III. PRINCIPLE OF THE NOVEL PWM SCHEME

A. Principle of Normal SPWM Scheme

In normal SPWM modulation scheme, the duty cycles of three phases for inverter 1 can be expressed as:

$$\begin{cases} d_{a1} = (1 + m\cos\theta)/2 \\ d_{b1} = \left[1 + m\cos(\theta - 2\pi/3)\right]/2 \\ d_{c1} = \left[1 + m\cos(\theta + 2\pi/3)\right]/2 \end{cases} \tag{8}$$

where m is the modulation index, θ is the instantaneous angle, d_{a1}, d_{b1} and d_{c1} are the three phase duty cycles. The above equations can deduce the identical equation:

$$d_{a1} + d_{b1} + d_{c1} = \frac{3}{2} \tag{9}$$

In order to get the maximal phase voltage, the duty cycles of one winding connecting phase-legs should be complementary. So the relationship of duty cycles for each phase can be expressed as follows:

$$\begin{cases} d_{a1} + d_{a2} = 1 \\ d_{b1} + d_{b2} = 1 \\ d_{c1} + d_{c2} = 1 \\ d_{a2} + d_{b2} + d_{c2} = 1.5 \end{cases} \tag{10}$$

Under the above conditions, without losing generality, assume d_{a1} (the duty cycle of phase A_1) is maximal in six phase-legs which can deduce d_{a2} (the duty cycle of phase A2) is minimal, and $d_{b1} > d_{c1}$, $d_{b2} < d_{c2}$. The relationship can be shown in Fig. 6(a).

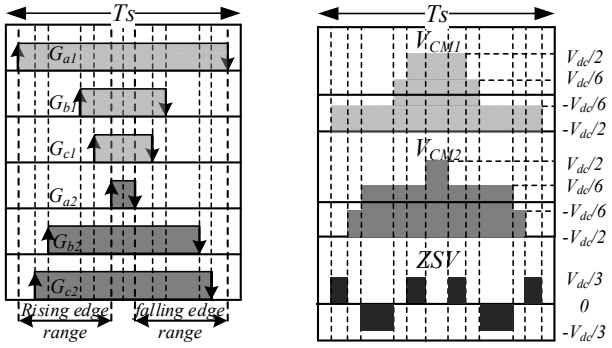


Fig.6 The PWM signals, CMVs and ZSV for normal SPWM scheme in one switching period: (a) PWM signals, (b) CMVs and ZSV

In fact, setting the maximal and minimal duty cycle in symmetric PWM scheme can prescribe limits to the range of rising edge and falling edge. Form Fig. 6(a), it can be found that the rising edges and falling edges are in different positions which lead to different CMVs for the two inverters and lose the function of eliminating ZSV. The CMV of two inverters and the difference of CMV are shown in Fig. 6(b).

B. Principle of the Novel PWM Scheme to eliminate ZSV

The losing the function of eliminating ZSV is owing to the symmetric PWM scheme. If appropriate phase-shift used, the rising and falling edges may have the ability to be aligned correspondingly. Fig. 7 show two kinds of phase-shift scheme to eliminate the instantaneous ZSV in one switching period. In this two schemes, the PWM signals of phase A which has the maximum or minimum duty cycle keeping symmetric while the PWM signals of phase B and C taking the phase-shift manner. Taking Fig. 7(a) for example, when the rising edge of C_2 PWM signal aligned with the rising edge of A_1 PWM signal with left side phase-shift, and the falling edge of B_2 PWM signal aligned with the rising edge of A_1 PWM signal with right side phase-shift, the state transition of ZSV caused by A_1 PWM signal can be cancelled out with cooperation of B_2 and C_2 PWM signals. In addition, the above phase-shift manner can keep the rising edges and falling edges stay in the corresponding position range. Similarly, the rising edge of B_1 PWM signal and the falling edge of C_1 PWM signal can be aligned with the rising and falling edges of A_2.

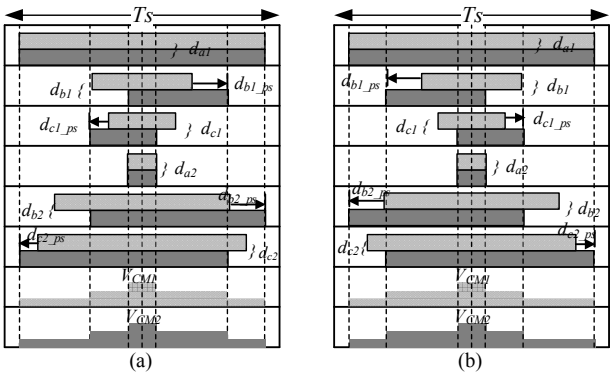


Fig. 7. The PWM signals and CMVs of ZSV elimination scheme based on SPWM: (a) scheme 1, (b) scheme 2

The above phase-shift actions can keep some rising and falling edges aligned, but the left rising and falling edges' position relationship should be taken into account, such as the falling edges of B_1 and C_2, the rising edges of C_1 and B_2. These action edge' positions can be calculated by the duty cycle and the length of phase-shift. The positions of left PWM edges can be expressed as:

$$\begin{cases} Ep_{B1\_f} = Ep_{B1\_r} + d_{b1} = Ep_{A2\_r} + d_{b1} = (1-d_{a2})/2 + d_{b1} \\ Ep_{C1\_r} = Ep_{C1\_f} - d_{c1} = Ep_{A2\_f} - d_{c1} = (1+d_{a2})/2 - d_{c1} \\ Ep_{B2\_r} = Ep_{B2\_f} - d_{b2} = Ep_{A1\_f} - d_{b2} = (1+d_{a1})/2 - d_{b2} \\ Ep_{C2\_f} = Ep_{C2\_r} + d_{c2} = Ep_{A1\_r} + d_{c2} = (1-d_{a1})/2 + d_{c2} \end{cases} \quad (11)$$

where Ep_{B1_f}, Ep_{C2_f}, Ep_{B2_r} and Ep_{C1_r} are the rising and falling edge positions correspondingly, d_{b1}, d_{b2}, d_{c1}, d_{c2} are the duty cycles for each phase-legs. Considering equations (8), (9) and (10), the rising edges and falling edges can be proved to be equal shown in equations (12) and (13).

$$\begin{aligned} Ep_{B1\_f} &= (1-d_{a2})/2 + d_{b1} = d_{a1}/2 + d_{b1} \\ &= (1-d_{a1})/2 + d_{a1} + d_{b1} - 1/2 \\ &= (1-d_{a1})/2 + 1 - d_{c1} = (1-d_{a1})/2 + d_{c2} = Ep_{C2\_f} \end{aligned} \quad (12)$$

$$\begin{aligned} Ep_{C1\_r} &= (1+d_{a2})/2 - d_{c1} = 1 - d_{a1}/2 - d_{c1} \\ &= (1+d_{a1})/2 - d_{a1} - d_{c1} + 1/2 \\ &= (1+d_{a1})/2 + d_{b1} - 1 = (1+d_{a1})/2 - d_{b2} = Ep_{B2\_r} \end{aligned} \quad (13)$$

So all of the rising edges and falling edges can keep aligned in normal SPWM scheme with combination of proper phase-shift, and the CMVs of two inverters can changed to be identical. In Fig. 7(b), though the phase-shift directions for phase B and C changed, but the situation can also keep the same CMVs and get ZSV elimination effect. According to the characteristic of the above manner, this modified scheme can be called as SPWM_PS (SPWM phase-shift) method.

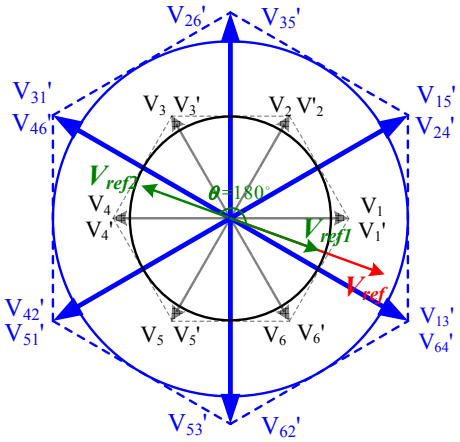


Fig. 8. Reference voltage combination for novel SPWM scheme

Finally, based on the duty cycles of each phase, the relationship of voltage vectors for two inverters can be easily deduced where V_{ref1} and V_{ref2} have the same amplitude and opposite directions. The resultant space vector V_{ref} for dual-inverter and V_{ref1}, V_{ref2} can be drawn and shown in Fig. 8. From Fig. 8, it can be clearly seen that the voltage vector synthesis principle of the proposed method is different from the normal ZSV elimination schemes, while the modulation index range can keep the same which can reach the maximal value 1.

IV. SIMULATION RESULTS

In order to verify the novel SPWM scheme and compare with conventional modulation schemes, the simulation based on MATLAB/SIMULINK have been developed. The real-time duty cycles for all phase-legs in novel SPWM modulation scheme can be easily calculated, the difficulty is to realize real-time phase-shift. Actually, the PWM phase-shift effect in simulation can be realized by changing the comparison values in first and second half switching period. The parameters for dual-inverter and the load are chosen and shown in Table II.

TABLE II
SIMULATION PARAMETERS

Symbol	Parameters	Value
V_{dc}	DC link voltage	300V
m_index	Modulation index	0.8
f_s	Switching frequency	10kHz
f_0	Fundamental frequency	50Hz
L_s	Load inductance	1mH
R_s	Load resistance	4.7Ω

First, the CMVs of different inverters for the SPMW_PS scheme are shown in Fig. 9. In Fig. 9(a), it can be found that the CMVs of SPWM_PS scheme have the same peak value of $\pm V_{dc}/2$. At the same time, the enlarged instantaneous CMVs for the novel scheme are shown in Fig. 9(b), it can be found that the CMVs of two inverters can keep identical which proves the ZSV of dual inverter can be cancelled out. In addition, the CMV waveforms are asymmetric because of phase-shift which is similar to the above theory introduction.

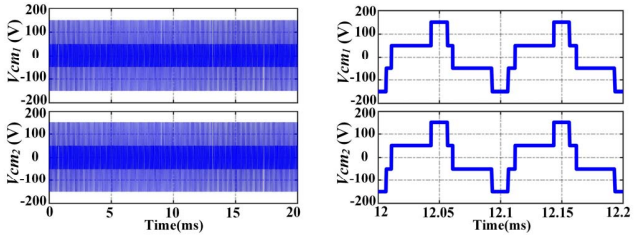


Fig. 9. The CMV comparison of individual inverters: (a) one fundamental period, (b) two switching periods

In order to verify the effect of phase-shift manner, the three phase currents and ZSC for SPWM and SPWM_PS schemes are drawn and shown in Fig. 10. It can be found that the influence of phase-shift manner to phase currents is limited, but the ZSC can be eliminated in idea condition whether in dynamic or steady state which is well worth implementing.

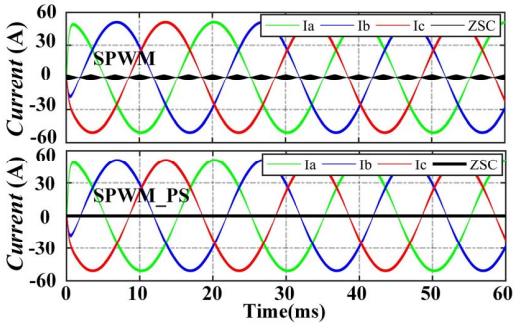


Fig. 10. The three phase currents and ZSC comparison for SPWM and RCMV_SPWM_PS schemes

In order to verify the performance of the novel method to phase current, the output phase current comparison for conventional DPWM, SVPWM and novel SPWM_PS schemes have been shown in Fig.11. It can be clearly seen that SPWM_PS has the smallest current ripple in time domain. Through frequency domain analysis, the THD of this three schemes can be calculated and are 4.38%, 3.07% and 2.41% correspondingly. The SPWM_PS scheme has the lowest THD value which is attributed to the elimination of odd switching frequency harmonics for output current shown in frequency domain, and the elimination of switching frequency harmonic (10kHz) which contributes the THD most.

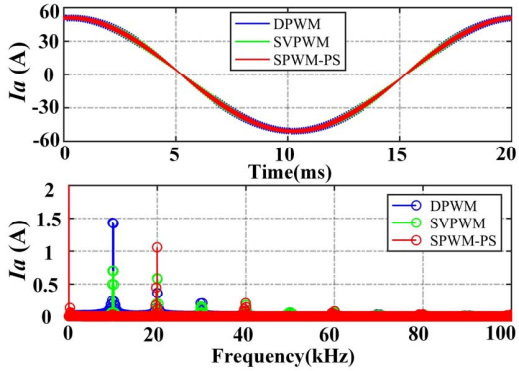


Fig. 11. The phase current comparison for different ZSV elimination schemes

Finally, the characteristic in DC side current for different schemes are compared and shown in Fig. 12. It can be clearly seen that the normal SPWM scheme without the elimination effect of ZSC has the maximum peak value shown in time domain. So regardless the double frequency effect in DC side current, the ZSC occurring in the AC side will enlarge the DC side current ripple which leads the maximum DC current for the normal SPWM scheme. In addition, the DPWM and SVPWM schemes cannot eliminate the switching frequency current which will occur bigger voltage ripple in DC side capacitance. The SPWM_PS scheme not only can eliminate the ZSC in AC side, but also can restrain odd switching frequency harmonics for DC current, particularly the elimination of switching frequency current which contributes the reduction of DC side voltage ripple most. So the proposed scheme has the potential to reduce the DC side capacitance value if taking the same voltage ripple as requirement.

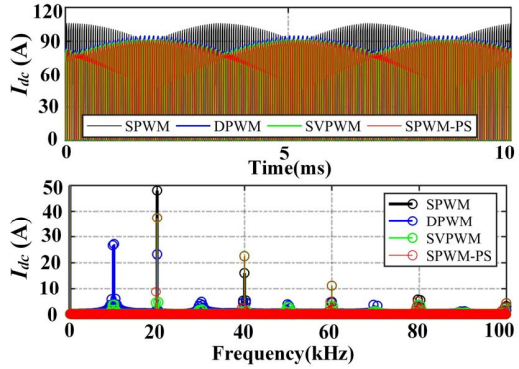


Fig. 12. Simulation comparison: DC side current

V. EXPERIMENTAL RESULTS

In order to verify the proposed method and compare with other methods, the test has been carried out in an experimental platform in which two inverters are supplied by one DC power source with 100V DC voltage. The control algorithm is implemented in a DSP TMS320F28335 and the switching frequency is 10 kHz. The three phase R-L load are connected to the corresponding phase-legs. The PWM signals can be recorded by the multi-channel oscilloscope, and the phase currents can be collected by the high resolution oscilloscope. The detailed experimental setup is shown in Fig. 13.

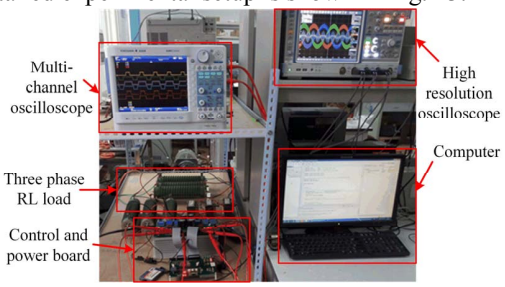
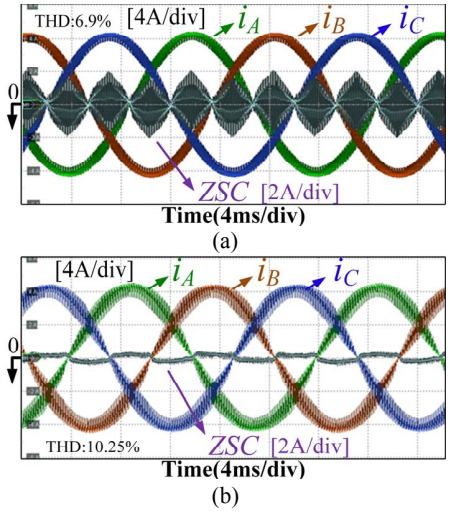


Fig. 13. The Experimental platform

Then, the three phase currents and ZSC are tested with different schemes. The waveforms are shown in Fig. 14. It can be found that the ZSC obviously exist in normal SPWM scheme shown in Fig. 14(a). The ZSC mainly consist of high frequency component caused by high frequency ZSV which coincides with the simulation result. In addition, the conventional DPWM and SVPWM schemes are tested to verify the ZSV elimination performance. The waveforms are shown in Fig. 14(b) and (c). It can be clearly seen that ZSC is significantly reduced comparing to the normal SPWM scheme, the small ZSC is caused by the dead time effect and other non-ideal factors, such as the asymmetrical three phase load, voltage drops on the power semiconductor devices and switching dead time. Meanwhile, the proposed SPWM_PS scheme is tested and the waveforms is shown in Fig. 14(d). It can be seen that the ZSC is also reduced and has the similar performance with DPWM and SVPWM schemes which proves the ZSV elimination performance.



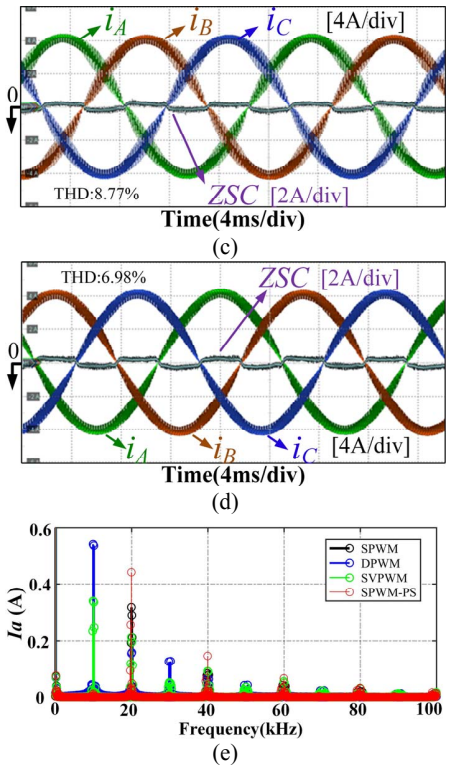


Fig. 14. The three phase currents and ZSC for different modulation schemes: (a) normal SPWM scheme, (b) DPWM scheme, (c) SVPWM scheme, (d) SPWM_PS scheme, (e) spectrum comparison

In addition, considering the THD in phase current for different ZSV elimination schemes, the SPWM_PS scheme has the lowest THD and the THD value is close to the normal SPWM scheme which also coincide with the simulation result. In order to further investigate the reason of THD reduction in phase current, the frequency domain analysis is adopted shown in Fig. 14(e). It can be found that the SPWM_PS and SPWM schemes have double frequency effect which can eliminate the odd switching frequency harmonics. So the proposed method's phase current THD can be reduced comparing to DPWM and SVPWM schemes. The frequency domain analysis of different schemes show the similar result with simulation.

Finally, the DC link voltage, DC capacitor current are measured and compared among different schemes shown in Fig. 15. The time domain comparison shown in Fig. 15(a)-(d), it can be found that the normal SPWM scheme has maximum peak value of DC ripple current while other schemes have similar peak values. The frequency domain analysis is shown in Fig. 15(e), though the normal SPWM scheme exists double frequency effect in DC side current, the ZSC occurring in the AC side amplifies the DC current ripple which leads the maximum DC current in twice switching frequency (20kHz). In addition, the DPWM and SVPWM schemes (especially the DPWM) cannot eliminate the switching frequency current which will generate bigger voltage ripple in DC side capacitance. Contrary, the SPWM_PS scheme can eliminate odd switching frequency harmonics and restrain the double switching frequency harmonic for DC ripple current. The elimination of switching frequency harmonic can obvious reduce the DC side voltage ripple which is beneficial for DC

side capacitance reduction if taking the same voltage ripple as requirement.

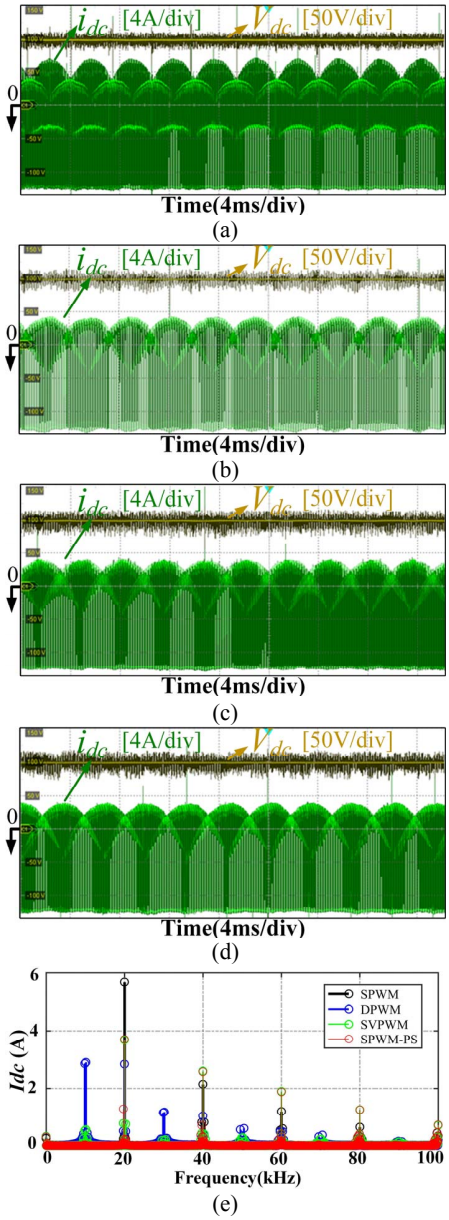


Fig. 15. The DC link voltage and DC capacitor current for different modulation schemes: (a) normal SPWM scheme, (b) DPWM scheme, (c) SVPWM scheme, (d) SPWM_PS scheme, (e) spectrum comparison

VI. CONCLUSIONS

This paper introduces the novel PWM method for dual two-level inverter fed open-end winding AC motor. Only by normal SPWM scheme and suitable phase-shift, the ZSV which leads to ZSC in open-end winding AC motor can be controlled to zero in ideal condition. The characteristic and effect are summarized for the proposed method:

1) The proposed modulation scheme can eliminate the odd switching frequency harmonics in phase current which can decrease the THD compared to conventional modulation schemes.
2) The proposed modulation scheme can also eliminate the odd switching frequency harmonics in DC side current. The elimination of odd switching frequency harmonics in DC side can restrain the voltage ripple of DC link and reduce the capacitance requirement which is benefiicial for increasing the power density of system.

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