Research on Different Balance Control Strategies for a Power Electronic Traction Transformer

Jingxi Yang*, Jianqiang Liu*, Jiepin Zhang*, Nan Zhao*, Trillion Q. Zheng*
*School of Electrical Engineering, Beijing Jiaotong University, Beijing, China
E-mail: liujianqiang@bjtu.edu.cn

***Abstract*—The power electronic traction transformer (PETT) consists of a single-phase cascaded H-bridge (CHB) converter and several output-parallel DC/DC converters. In order to make the PETT work steadily, it is needed to maintain its intermediate-dc-voltage balance and output-current sharing between different cells. In this paper, an overview of PETT balance control strategies is presented at first. Their basic control principle, main control structure and interrelation are investigated. Based on the control tasks of CHB and DC/DC converters, the balance control strategies can be classified into two categories. With the comparison of them, the second balance-control category has several advantages in the aspect of ac-input-current quality, balance control effectiveness, computation resource occupation and soft-starting performance, while it also brings several disadvantages with regard to auxiliary-power-supply design and balance-control regulation range. Finally, further research towards the simulation and experiment based on a five-cell PETT laboratory prototype with rated power of 30 kW is carried out.**

I. Introduction

In order to improve the electricity conversion efficiency of traction drive system, to lower the volume and weight of propulsion converters, and to reduce the total operation cost of high-speed trains, the concept towards power electronic traction transformer (PETT) is developed, which is hoped to replace the line-frequency traction transformer and the four-quadrant rectifier in next generation high-speed trains [1-3]. What's more, with the development of SiC devices [4], nanocrystalline material [5] and soft-switching technique [6], the power density of PETT equipment can be improved even much higher. PETT is a complicated system, which is made up of several converters through connecting them in series or in parallel. According to the functionality of these converters, PETT can be divided into two parts, including the cascaded H-bridge (CHB) converter in the front end and the output-parallel DC/DC converters in the backward stage. In order to make sure the normal operation of PETT system, it is needed to make the intermediate-dc-voltage balance and output-current sharing among different cells through control. Otherwise, due to the mismatch of the main circuit parameters, the intermediate dc voltages and the output currents in different cells may not be the same, and may even diverge to bring the PETT system into collapse. According to the roles of CHB and DC/DC converters in the balance control, the control strategies can be classified into two categories [10]:

This work was supported by the National Key Research and Development Program of China under Grant 2017YFB1200901-09.

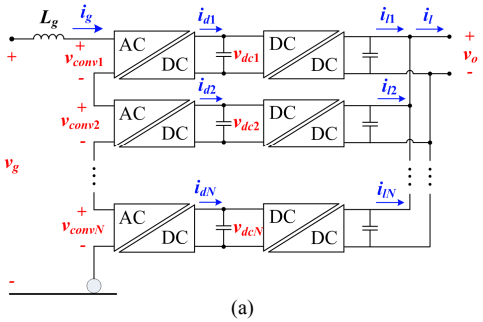
1) The intermediate-dc-voltage balance and output-current sharing (or intermediate-dc- current sharing) among different PETT cells are realized by CHB converter and DC/DC converters respectively [7-9].

2) The intermediate-dc-voltage balance and output-current sharing among different PETT cells are all realized by DC/DC converters, and none of balance control approaches are adopted by CHB converter [10-11].

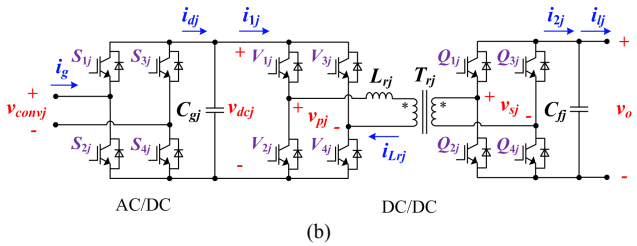
In order to obtain an optimal balance control scheme suitable for the PETT, it is necessary to compare the above categories of balance control strategies. In Section II, an overview of them is presented, including the basic control principle, main control structure and interrelation. Based on the corresponding characteristics of these two categories of balance control strategies, their advantages and disadvantages are analyzed respectively in Section III. The simulation and experiment results of these two categories of balance control strategies are exhibited in Section IV. Synthesize the theoretical analysis and the simulation and experiment results, the conclusion is given in Section V.

II. Overview of PETT Control Strategies

The circuit diagram of a PETT is shown in Fig. 1(a). The PETT consists of N AC/DC converters and N DC/DC converters. The input side of AC/DC converters is in series, which constitute the CHB converters. The output side of DC/DC converters is in parallel. A PETT cell is made up of an AC/DC converter and a DC/DC converter. These two converters are connected in dc side, which is defined as intermediate dc side. The circuit diagram of *Cell j* is shown in Fig. 1(b), where $j = 1,2,\cdots,N$. In this paper, the dual active H-bridge (DAB) DC/DC converter is taken as an instant in the DC/DC conversion stage.



(a)



(b)

Figure 1: The circuit diagram of (a) a PETT; and *Cell j* of a PETT.

In Fig. 1(a), L_g is ac input filter inductor, v_g is the ac input voltage, i_g is the ac input current, v_o is the dc output voltage, i_l is the dc output current. In *Cell j*, C_{gj} is the intermediate dc capacitor, C_{fj} is the dc output capacitor, L_{rj} is the DAB storage inductor, T_{rj} is the medium/high frequency transformer, v_{convj} is PWM voltage, i_{dj} is the dc output current of the H-bridge of AC/DC converter, v_{dcj} is the intermediate dc voltage, i_{1j} is the input current of the input H-bridge of DC/DC converter, v_{pj} is the square voltage of the input H-bridge of DC/DC converter, i_{Lrj} is the DAB inductor current, v_{sj} is the square voltage of the output H-bridge of DC/DC converter, i_{2j} is the output current of the output H-bridge of DC/DC converter, i_{lj} is the dc output current of DC/DC converter, S_{ij} is the switch of AC/DC converter, V_{ij} is the switch of the input H-bridge of DC/DC converter, and Q_{ij} is the switch of the output H-bridge of DC/DC converter, where $i = 1,2,3,4$.

As defined in [10], the control system of a PETT is made up of two parts, including the overall control and the balance control. In the overall control, the sum of intermediate dc voltages ($\sum v_{dcj}$), the ac input current (i_g), and the dc output voltage (v_o) are regulated. In the balance control, voltage balance and current sharing among different cells are maintained. From the point of the whole PETT system, the control strategies presented in the existing publication can be classified into two categories below:

1) *Two-stage overall control and two-stage balance control* (O2B2). In O2B2, the overall control is accomplished collectively by the CHB and the DC/DC converters, while the balance control is separated, where the intermediate-dc-voltage (v_{dcj}) balance is realized by the CHB, while the intermediate-dc-current (i_{1j}) or output-current (i_{lj}) sharing is realized by DC/DC converters [7-9].

2) *Two-stage overall control and single-stage balance control* (O2B1). In O2B1, the overall control is still accomplished collectively by the CHB and the DC/DC converters. However, only the DC/DC converters participate in the balance control, and all of the CHB modulating waves are the same. The intermediate-dc-voltage (v_{dcj}) balance is maintained through the regulation of DC/DC converters, and then the output-current (i_{lj}) sharing is achieved automatically [10-11].

A. Overview of O2B2

As known by the authors, in O2B2, there are two kinds of voltage balance control strategies for the CHB. They are briefly indicated as follows.

1) *The voltage balance control based on the feedback closed-loop regulation* (FCR) [8]. The control structure of FCR is shown in Fig. 2(a) with control structure modified. $G_{cv}(s)$ is the total intermediate-dc-voltage controller, $G_{ci}(s)$ is the ac-input-current controller and $G_{vb}(s)$ is the voltage balance controller. v_{ctrj} the PWM modulated wave of *Cell j*. The drive signal of S_{ij} is generated by the modulation between v_{ctrj} and its corresponding carrier.

It should be noticed that, different with the control structure presented in [8], in Fig. 2(a), the output control variable of $G_{vb}(s)$, y_{cj}, needs to be multiplied with the sign value of $i_{gm,ref}$ (the output control variable of $G_{cv}(s)$), which is denoted as $sign(i_{gm,ref})$. That is

$$v_{cj} = \frac{1}{N} v_{conv,ref} \cdot \left(1 + y_{cj} \cdot sign(i_{gm,ref})\right) \tag{1}$$

and

$$sign(i_{gm,ref}) = \begin{cases} +1, & i_{gm,ref} > 0 \\ -1, & i_{gm,ref} < 0 \end{cases} \tag{2}$$

The cause and the necessity of this modification will be analyzed detailedly in Section III.

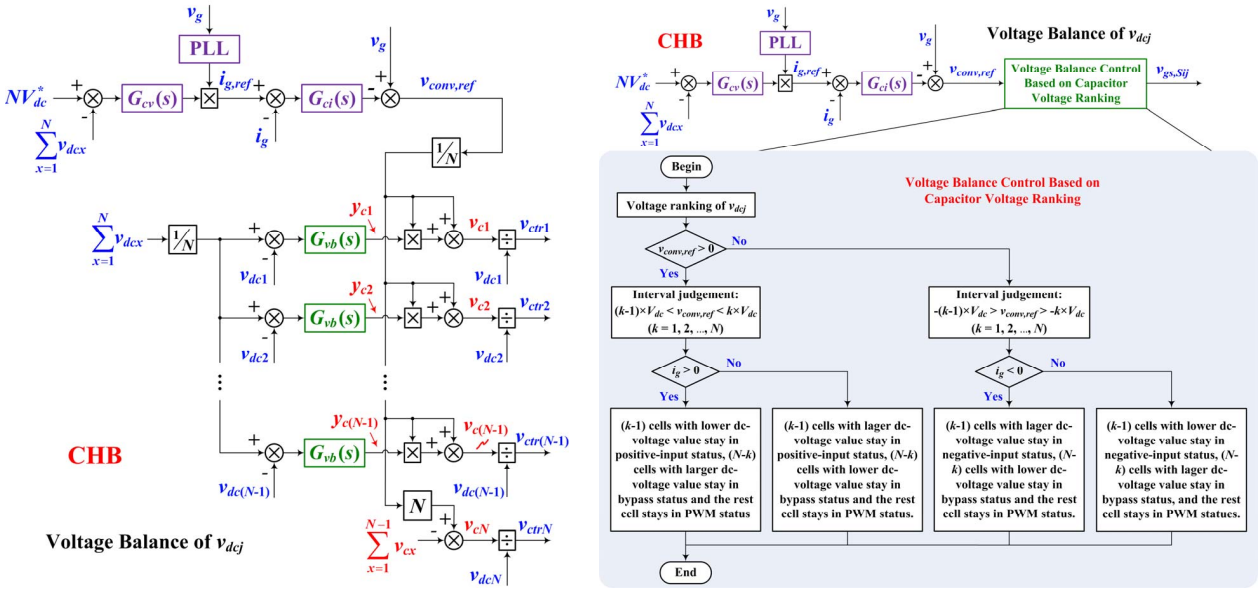
2) *The voltage balance control based on the capacitor-voltage ranking* (CVR) [7]. The control structure of CVR is shown in Fig. 2(b). The drive signal ($v_{gs,S_{ij}}$) of S_{ij} is generated directly from CVR. The most obvious characteristic of CVR is that in every switching period, only one cell processes PWM, and other cells are in positive-input status or negative-input status or bypass status. When a cell is in positive-input status, its PWM voltage v_{convj} is equal to $+v_{dcj}$; when a cell is in negative-input status, its PWM voltage v_{convj} is equal to $-v_{dcj}$; when a cell is in bypass status, its PWM voltage v_{convj} is equal to 0. CVR can be realized in several different ways. For example, when $(k-1)V_{dc} < v_{conv,ref} < kV_{dc}$ (V_{dc} is the nominal value of intermediate dc voltage v_{dcj}, and $k = 1,2,\cdots,N$) and $i_g > 0$, there can be $(k-1)$ cells in positive-input status, $(N-k)$ cells in bypass status and one rest cell in PWM status; or there can be k cells in positive-input status, one cell in negative-input status, $(N-k-2)$ cells in bypass status and one rest cell in PWM status; the other kinds of realization can be derived with similar principle. For the sake of analysis and comparison, the first kind of realization is taken as an instance in this paper.

As known by the authors, in O2B2, there are three kinds of current sharing control strategies for the DAB converters. They are briefly indicated as follows.

1) *The output-current sharing control* (OCS). Its control structure is shown in Fig. 3(a). $D_{cv}(s)$ is DAB dc-output-voltage controller while $D_{ib}(s)$ is the DAB output-current sharing controller. $d_{\varphi j}$ is the phase-shift control variable of the j-th DAB converter. The average value of the DAB output current i_{lj} is

$$\mathrm{Avg}(i_{lj}) = \frac{2}{T_{sw\_DAB}} \int_0^{0.5T_{sw\_DAB}} i_{lj}(t)\,dt \tag{3}$$

where T_{sw_DAB} is the DAB switching period. The variation period of i_{lj}, i_{1j} and i_{2j} is all equal to $0.5T_{sw\_DAB}$.



(a) (b)

Figure 2: For O2B2, (a) the control structure diagram of FCR after modified; and (b) the control structure diagram of CVR.

2) *The average-input-power balance control* (AIPB) [8]. Its control structure is shown in Fig. 3(b). $D_{pb}(s)$ is the DAB average-input-power balance controller. The average input power P_{in_DAB} is calculated by i_{Lrj} and v_{pj}. Suppose that there is no switching loss for V_{ij}, then

$$P_{in\_DAB} = \frac{2}{T_{sw\_DAB}} \int_0^{0.5T_{sw\_DAB}} i_{Lrj}\, v_{pj} dt = \frac{2}{T_{sw\_DAB}} \int_0^{0.5T_{sw\_DAB}} i_{1j}\, v_{dcj} dt \approx v_{dcj} \cdot \mathrm{Avg}(i_{1j}) \quad (4)$$

Therefore, in essence, AIPB is equivalent to the DAB input-current (i_{1j}) sharing control. Suppose that the efficiency of DAB converters is 100%, then

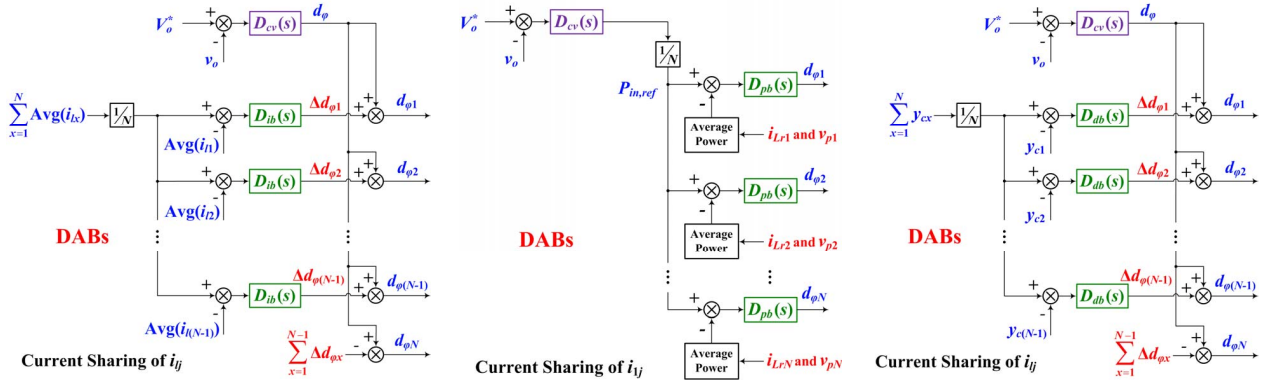
$$v_{dcj} \times \mathrm{Avg}(i_{1j}) = v_o \times \mathrm{Avg}(i_{lj}) \quad (5)$$

From this perspective, OCS and AIPB are equivalent. What's more, according to the above equation, if the intermediate dc voltages v_{dcj} are not the same, the DAB dc-input-current sharing and the DAB dc-output-current sharing can't be achieved at the same time. This is why in O2B2, the balance control should be separated and respectively taken by CHB and DABs.

3) *The current sensorless power balance control* (CSPB) [9]. Its control structure is shown in Fig. 3(c). $D_{db}(s)$ is the DAB balance controller. y_{cj} is the output variable of FCR controller $G_{vb}(s)$, and

$$\sum_{x=1}^{N} y_{cx} = 0 \quad (6)$$

Through the control of $D_{db}(s)$, the output y_{cj} of each FCR controller will tend to be the same. From Fig. 2(a), it can be seen that when y_{cj} tends to be the same, the modulated wave v_{ctrj} will tend to be the same. Meanwhile, the intermediate-dc-voltage (v_{dcj}) balance is achieved. Thus, from the point of control mechanism, CSPB is similar to O2B1, in which the DAB converters are all equivalent to an input-series-output-parallel (ISOP) system and the balance control objectives of a PETT are realized mainly through the DAB converters. The difference between them is that the voltage balance control loop of the CHB can't be omitted in CSPB.



(a) (b) (c)

Figure 3: For O2B2, (a) the control structure diagram of OCS; (b) the control structure diagram of AIPB; and (c) the control structure diagram of CSPB.

B. Overview of O2B1

In O2B1, none of balance control approaches are adopted by the CHB and all of the modulated waves v_{ctrj} are the same. The intermediate-dc-voltage (v_{dcj}) balance is controlled by DC/DC converters [10-11]. The control structure is shown in Fig. 4. $D_{vb}(s)$ is the DAB voltage balance controller. As the modulated waves v_{ctrj} from different cells are the same, the dc input currents $i_{dj} = i_g \times v_{ctrj}$ from different cells are equal to each other. Therefore, the input side of DAB converters is in series equivalently. As

$$i_{dj} \times v_{dcj} = i_{lj} \times v_o \tag{7}$$

It means that if the intermediate dc voltages v_{dcj} can be kept balance through control, the output-current (i_{lj}) sharing will be achieved automatically.

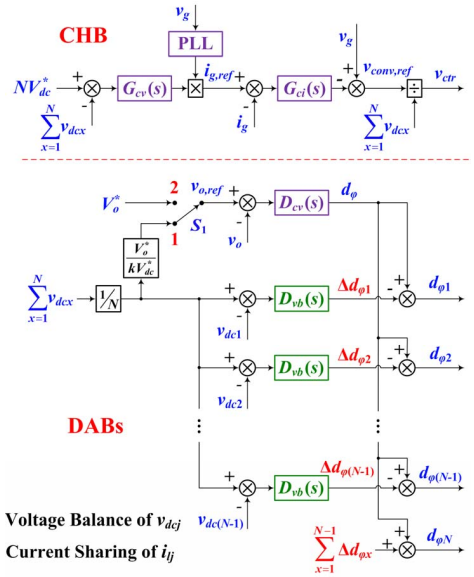


Figure 4: The control structure diagram of O2B1, where the DC/DC converters is the DABs.

III. Comparison of Different Balance Control Strategies

In the following paper, O2B2 and O2B1 are compared in the aspect of computation resource occupation, ac-input-current quality, balance control effectiveness in no-load condition or when power reversely flows, soft-starting performance, auxiliary-power-supply design and regulation range of balance control.

A. Advantages of O2B1

1) *Low computation resource occupation*. As the balance control is not needed for the CHB in O2B1, the control algorithm is substantially simplified, which can significantly reduce the resource occupation of digital chips, especially when the cell number is large. What's more, in some control strategies of O2B2, such as OCS and AIPB, the high-frequency sampling and filtering for current signals are needed, which will occupy more computation resource of digital chips. However, on the contrary, similar operation is not needed in O2B1.

2) *Better ac-input-current quality*. For O2B1, as all of the modulated waves v_{ctrj} are the same, it won't deteriorate the quality of ac input current i_g. However, for O2B2, v_{ctrj} may be different as the intermediate-dc-voltage balance is achieved by the CHB. Only when CSPB is adopted by DC/DC converters, v_{ctrj} can be equal to each other in steady state so that the ac input current i_g won't suffer any bad effect.

3) *Balance control effectiveness in no-load or light-load condition*. For O2B2, there is a serious problem that in no-load or light-load condition, FCR and CVR may lose their control effect, which will lead to the mismatch of v_{dcj}. The core control principle of CVR is that based on the dc voltage value (v_{dcj}) in different cells and the flowing direction of ac input current i_g, the low-voltage capacitors are charged and the high-voltage capacitors are discharged through controlling the IGBT devices. However, in no-load or light-load condition, the flowing direction of ac input current i_g may be misjudged by the PETT digital control system. In order to avoid aliasing and suppress the influence of power devices' switching operation on the sampling process, the sampling point is chosen as the middle place of the switching ripple of i_g. It can be seen from Fig. 5(a), in no-load or light-load condition, the sign of i_g and its discrete sampling value $i_{g,Discr}$ is not always the same. In such situation, CVR may lose its effect, as shown in Fig. 5(b). For FCR, the core control principle is that on the basis of $i_{dj} = i_g \cdot v_{ctrj}$, if the dc voltage ($v_{dcj}$) in some cell is lower than others, through increasing the amplitude of v_{ctrj}, the dc-side current i_{dj} will become large, and finally the dc voltage v_{dcj} will increase. However, when the CHB is in no-load or light-load condition, $i_g \approx 0$, and then $i_{dj} = 0 \cdot v_{ctrj} = 0$, which will make FCR lose its control effect, as shown in Fig. 5(c). Although similar phenomenon has been reported in [7] [11], the mechanism is regarded as large output-power unbalance in those papers. It is another kind of control-invalidation mechanism, which is different from the one indicated above. It can't be used to explain the invalidation of FCR in no-load condition.

What's more, it should be noticed that compared to FCR, the influence of the invalidation of CVR on the deviation of intermediate dc voltages is quite small. Therefore, it can be considered to use such control scheme: when the CHB is in no-load or light-load condition, CVR is adopted; and when the CHB is in heavy-load condition, FCR is adopted. It will bring extra benefit that the efficiency of the CHB in no-load or light-load condition is quite high. Because, for CVR, in every switching period, there is only one cell to process PWM. The simulation result related to this control scheme will be given in Section IV.

However, in any case, such balance-control-invalidation problem doesn't exist in O2B1.

4) *Balance control effectiveness when power reversely flows*. There is a serious problem for the traditional FCR: when power reversely flows, FCR will lose its control effect and make the intermediate dc voltages diverge. However, such problem is rarely mentioned in the existing publication. Here, the invalidation mechanism is introduced. When power forward

flows, the positive direction of the currents is shown in Fig. 1(b); and when power reversely flows, the direction of the currents is reverse. Then

$$i_{lj} - i_{aj} = C_{gj}\frac{dv_{dcj}}{dt} \tag{8}$$

and

$$i_{aj} = i_g \cdot v_{ctrj} \tag{9}$$

According to the control logic shown in Fig. 2(a), when power reversely flows and v_{dcj} is smaller than the average value $\left(\sum v_{dcj}\right)/N$, the output control variable of $G_{vb}(s)$, y_{cj}, will increase, following with the amplitude increasing of v_{ctrj} and i_{aj}. However, as a result, the capacitor current of C_{gj} will be reduced and then the voltage v_{dcj} will be deceased. Therefore, as the time going on, the voltage deviation will be enlarged and finally the dc voltages will diverge, as shown in Fig. 6(a).

In order to settle down this problem, a modification towards the FCR control structure is presented in Section II, as shown in Fig. 2(a). After modified, FCR is effective when power reversely flows, and the simulation waveforms is shown in Fig. 6(b).

However, in any case, such balance-control-invalidation problem doesn't exist in O2B1 or CVR.

5) *Soft-starting performance*. For O2B2, the CHB starts at first, and later, after the intermediate dc voltages reach their rated values, the DC/DC converters start. When DC/DC converters start, in order to pre-charge their dc output capacitors, the duty ratio of the input H-bridge (V_{1j}, V_{2j}, V_{3j} and V_{4j}) increases slowly from 0 to 0.5, and the output H-bridge (Q_{1j}, Q_{2j}, Q_{3j} and Q_{4j}) operates as an diode rectifier. After the dc output voltage v_o increases to a certain value, the DC/DC converters will change to the closed-loop control mode from open-loop control mode. During this control-mode change, there are two serious problem.

Firstly, if no soft changing method (for example, it can adjust the drive pulses, or repeatedly change the control parameters on line, or increase the reference with a slow slope) is adopted, the large peak value of inductor currents i_{Lrj} [12] or dc output voltages v_{dcj} can't be avoided; on the contrary, if some soft changing methods are adopted, in one hand, the duration of control-mode change may become very long, which will seriously influence the PETT starting speed, in another hand, as the robustness of the soft-changing parameters is not strong, it has to adjust the parameters according to the practical application.

Secondly, for the PETT using star-connected distributed control structure [13], all of the DC/DC converters can't change their control mode at the same time after pre-charging dc output capacitors, which will make the inductor current i_{Lrj} in some cells become very large.

However, similar problem doesn't exist in O2B1.

B. Disadvantages of O2B1

1) *Auxiliary-power-supply design*. If O2B1 is adopted, DC/DC converters must start at first, and then the CHB works as a diode rectifier to pre-charge the intermediate dc capacitors and the dc output capacitors [10]. It means that the PETT control system and the IGBT drivers of DC/DC converters must operate normally before PETT starts. It restricts the application of self-powered auxiliary power supply [14], in which the power for each cell comes from the local intermediate-dc capacitor.

2) *Regulation range of balance control*. For O2B1, the voltage balance and current sharing is accomplished all by the DC/DC converters. However, the regulation range of DC/DC converters is finite (that is to said, the phase-shift variation for DAB or the frequency variation for LLC resonant converter is finite). When the mismatch of the main circuit parameters is large, or some IGBT devices fail, it may beyond the regulation range of DC/DC converters, which will lead the intermediate dc voltages v_{dcj} and output currents i_{lj} into divergence. Different from O2B1, for O2B2, the voltage balance and current sharing is accomplished by the CHB and the DC/DC converters. If it doesn't beyond the regulation range of the CHB, even when DC/DC converters lose their balance control effect, the intermediate-dc-voltage balance can be realized. Meanwhile, the convergent mismatch exists in the output currents i_{lj}.

IV. Simulation and Experiment Results

Based on the five-cell PETT laboratory prototype with rated power of 30 kW, the simulation and experiment results are given below.

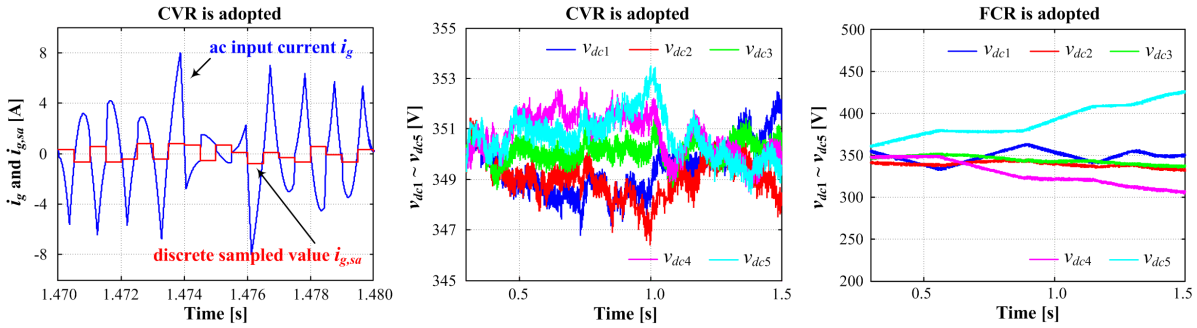
A. Simulation Results

In the simulation, the intermediate dc capacitance in *Cell* 1 ~ *Cell* 5 is set as 6.46 mF, 6.46 mF, 6.8 mF, 7.14 mF and 7.14 mF respectively, while the DAB inductance in *Cell* 1 ~ *Cell* 5 is set as 1.62 mH, 1.62 mH, 1.8 mH, 1.98 mH and 1.98 mH respectively.

In the first group of simulation, in order to avoid the influence of DC/DC converters on the performance of CHB balance control, the simulation model is only included the CHB. The CHB operates in no-load condition and two different kinds of balance control strategies, including CVR and FCR, are adopted. When CVR is applied, the simulation waveforms of the ac input current i_g and its discrete sampled value $i_{g,sa}$ are shown in Fig. 5(a), while the simulation waveforms of the intermediate dc voltages v_{dcj} $(j = 1,2,\cdots,5)$ are shown in Fig. 5(b). It can be seen in Fig. 5(a), the sign of i_g is not always the same as the one of $i_{g,sa}$, which may make the PETT control system misjudge, and result in charging high-voltage capacitors and discharging low-voltage capacitors. Therefore, as exhibited in Fig. 5(b), v_{dcj} is not identically equal to the rated value of 350 V, but oscillates from 347 V to 353 V. When FCR is applied, the simulation waveforms of the intermediate dc voltages v_{dcj} are shown in Fig. 5(c). It can be seen that v_{dcj} is divergent, which means that FCR is completely invalid.

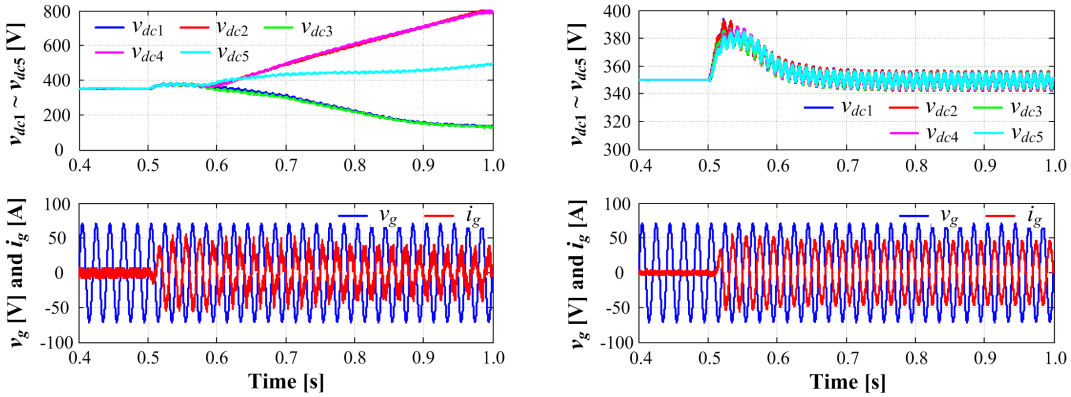
In order to compare the control performance of traditional FCR and modified FCR when power reversely flows, the related simulation waveforms are given in Fig. 6. The waveforms shown in Fig. 6(a) is based on the traditional FCR proposed in [8], while the waveforms shown in Fig. 6(b) is

based on the modified FCR proposed in this paper. In the simulation, when Time = 0.5 s, the no-load condition is suddenly changed to full-power energy-feedback condition. From Fig. 6, it can be seen that, when power reversely flows, FCR loses its control effect and the intermediate dc voltages v_{dcj} diverge; however, if the modified FCR is adopted, the balance control effectiveness won't suffer influence of the power flowing direction.



(a) (b) (c)

Figure 5: The simulation waveforms when the CHB operates in no-load condition, (a) with adopting CVR, the ac input current i_g and its discrete sampled value $i_{g,sa}$; (b) with adopting CVR, the intermediate dc voltages v_{dcj} $(j = 1,2,\cdots,5)$; (c) with adopting FCR, the intermediate dc voltages v_{dcj} $(j = 1,2,\cdots,5)$.



(a) (b)

Figure 6: The simulation waveforms when power reversely flows, (a) with adopting traditional FCR, the intermediate dc voltages v_{dcj} $(j = 1,2,\cdots,5)$ (Top), the ac input voltage v_g and the ac input current i_g (Bottom); (b) with adopting modified FCR, the intermediate dc voltages v_{dcj} $(j = 1,2,\cdots,5)$ (Top), the ac input voltage v_g and the ac input current i_g (Bottom).

In the second simulation group, CVR is adopted by the CHB, while OCS and interleaving technique [15] are adopted by the DABs. All of the DABs change to the closed-loop control mode from the open-loop control mode at the same time. The simulation waveforms of the intermediate dc voltages v_{dcj}, the output dc voltage v_o and DAB inductor currents i_{Lrj} when the DABs start are shown in Fig. 7. It can be seen that when the control mode changes, there is large peak value in some cells' inductor currents. It may result in large voltage drop in v_{dcj} and even damage the IGBT devices at worst.

In the three simulation group, OCS and interleaving technique are still adopted by the DABs, while CVR is adopted by the CHB in no-load or light-load condition and FCR is adopted by the CHB in heavy-load condition. The simulation waveforms are shown in Fig.8. In the simulation, when Time = 0.6 s, the input power P_{in} of the CHB is suddenly changed from 3 kW to 9 kW, and during the sudden load change, the voltage balance control strategy is switched from CVR to FCR.

From Fig. 8, it can be seen that when CVR is applied, the switching number of the IGBT devices in a switching period is quite small, which is beneficial to reduce the switching loss with the price of increasing harmonic distortion of ac input current.

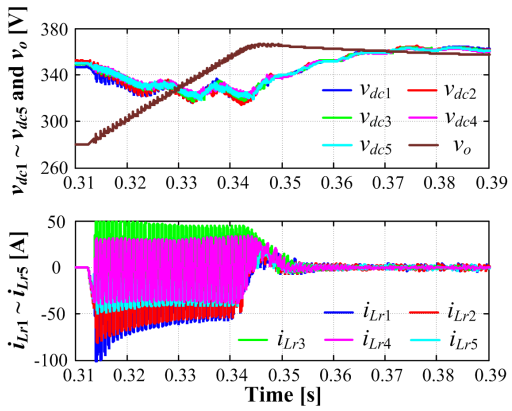


Figure 7: CVR is adopted by the CHB, and OCS is adopted by the DABs. The simulation waveforms of the intermediate dc voltages v_{dcj}, the output dc voltage v_o (Top) and DAB inductor currents i_{Lrj} (Bottom) when DABs start.

Compared to the scheme proposed in [16] to improve the efficiency in light-load condition by using diode rectifiers and active bypass switches, the CVR-FCR switchover scheme can not only improve the efficiency of the CHB in light-load

condition, but also reduce the THD value of i_g and improve the controllability and reliability of the PETT system.

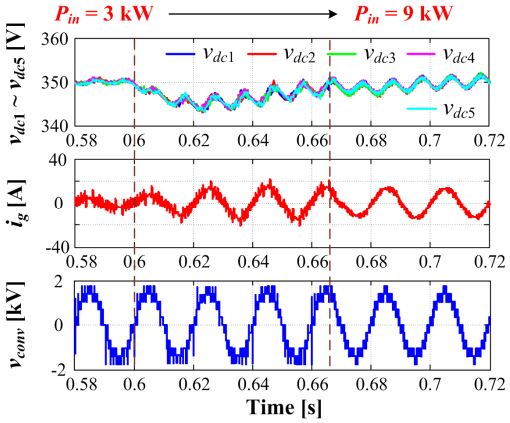


Figure 8: CVR-FCR switchover scheme is adopted. The simulation waveforms of the intermediate dc voltages v_{dcj} (Top), the ac input current i_g (Middle) and the PWM voltage v_{conv} (Bottom).

B. *Experiment Results*

In the experiment, O2B1 is adopted. The experiment waveforms of the intermediate dc voltages v_{dcj}, the output dc voltage v_o, the ac input voltage v_g and the ac input current i_g when the PETT starts in no-load condition are shown in Fig. 9.

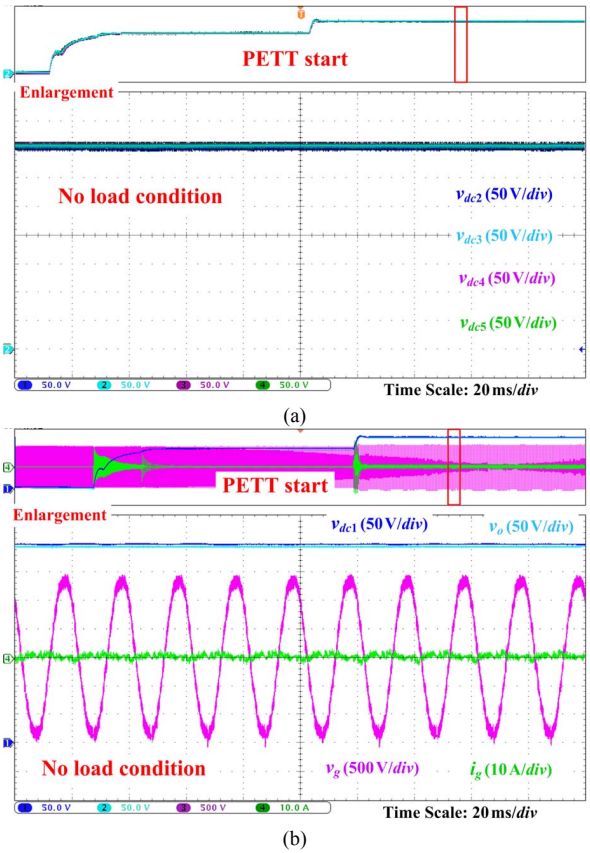


Figure 9: O2B1 is adopted. The experiment waveforms when PETT starts in no-load condition. (a) The intermediate dc voltage of *Cell* 2 ~ *Cell* 5, v_{dc2} ~ v_{dc5}; and (b) the intermediate dc voltage of *Cell* 1, v_{dc1}, the dc output voltage v_o, the ac input voltage v_g and the ac input current i_g.

It can be seen that the intermediate-dc-voltage balance is maintained in all the PETT starting process. In no-load condition, $i_g \approx 0$. However, there is no influence on the control performance of O2B1, and voltage balance is still achieved in no-load condition. When the ac input power is 24 kW, the experiment waveforms of the intermediate dc voltage of *Cell* 1 (v_{dc1}), the output dc voltage v_o, the ac input voltage v_g and the ac input current i_g are shown in Fig. 10(a), and the experiment waveforms of the DAB inductor currents of *Cell* 1 ~ *Cell* 4 (i_{Lr1} ~ i_{Lr4}) are shown in Fig. 10(b). The ac input current i_g is in phase with the ac input voltage v_g and free of low-order harmonics. With the use of interleaving technique, the phase different exists in different DAB inductor currents, which can reduce the switching ripple of the dc output voltage v_o.

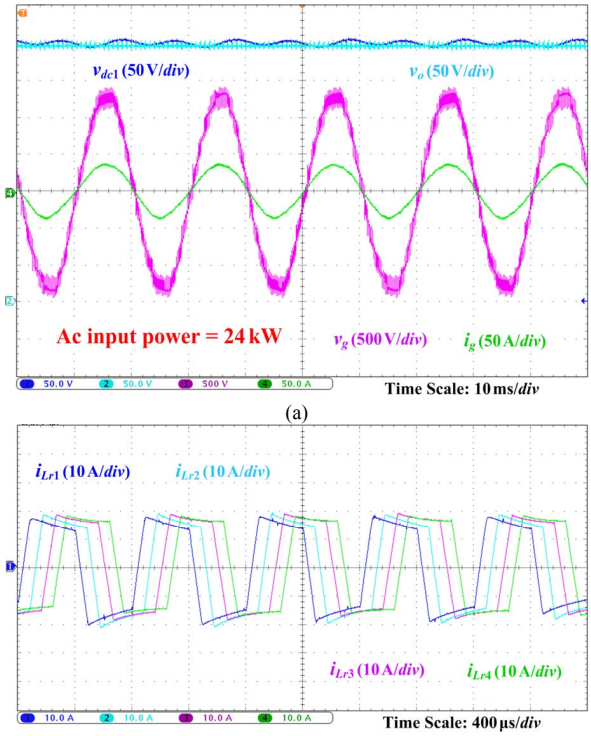


Figure 10: O2B1 is adopted. The experiment wave Figure 10: O2B1 is adopted. The experiment waveforms when the ac input power is 24 kW. (a) The intermediate dc voltage of *Cell* 1, v_{dc1}, the dc output voltage v_o, the ac input voltage v_g and the ac input current i_g; and (b) the DAB inductor currents of *Cell* 1 ~ *Cell* 4, i_{Lr1} ~ i_{Lr4}.

V. Conclusion

In this paper, the basic control principle, main control structure and interrelation of the balance control strategies for the PETT are investigated. The existing PETT control strategies can be classified into two categories, which are named as O2B2 and O2B1. With the comparison of them, O2B1 has several advantages in term of the ac-input-current quality, balance control effectiveness, computation resource occupation and soft-starting performance, and has several disadvantages in the aspect of auxiliary-power-supply design and balance-control regulation range. Simulation and experiment results based on a

five-cell PETT laboratory prototype are provided and all verify the effectiveness and correctness of the theoretical analysis. In a word, due to the much simpler structure, much stronger robustness of control parameters and much higher operation reliability, O2B1 is much more suitable for the PETT application.

VI. REFERENCES

[1] B. Sun, M. Li, C. An, J. Ma, and J. Yu, "Research on key technology of high-speed train energy consumption", in *Engineering Sciences*, vol. 17, no. 4, pp. 69-82, 2015.

[2] C. Zhao, D. Dujic, A. Mester, J. K. Steinke, M. Weiss, S. Lewdeni-Schmid, T. Chaudhuri and P. Stefanutti, "Power electronic traction Ttransformer—medium voltage prototype", in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3257-3268, July 2014.

[3] D. J. Taufiq, "Advanced propulsion drives and technology for tomorrow's railways", *presented at 3th Int. Conf.* on Railway Traction Systems, Tokyo, Japan, 2007, pp. 1-7.

[4] M. K. Das *et al*., "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," 2011 *IEEE Energy Conversion Congress and Exposition*, Phoenix, AZ, 2011, pp. 2689-2692.

[5] M. Leibl, G. Ortiz and J. W. Kolar, "Design and experimental analysis of a medium-frequency transformer for solid-state transformer applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 110-123, March 2017.

[6] J. Liu, J. Zhang, T. Q. Zheng and J. Yang, "A modified gain model and the corresponding design method for an LLC resonant converter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6716-6727, Sept. 2017.

[7] X. She, A. Q. Huang and G. Wang, "3-D space modulation with voltage balancing capability for a cascaded seven-level converter in a solid-state transformer," in *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3778-3789, Dec. 2011.

[8] T. Zhao, G. Wang, S. Bhattacharya and A. Q. Huang, "Voltage and power balance control for a cascaded H-bridge converter-based solid-state transformer," in *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1523-1532, April 2013.

[9] X. She, A. Q. Huang and X. Ni, "Current sensorless power balance strategy for DC/DC converters in a cascaded multilevel converter based solid state transformer," in *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 17-22, Jan. 2014.

[10] J. Liu, J. Yang, J. Zhang, Z. Nan and T. Q. Zheng, "Voltage Balance Control Based on Dual Active Bridge DC/DC Converters in a Power Electronic Traction Transformer," in *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1696-1714, Feb. 2018.

[11] G. Wang *et al*., "Comparisons of different control strategies for 20kVA solid state transformer," *2011 IEEE Energy Conversion Congress and Exposition*, Phoenix, AZ, 2011, pp. 3173-3178.

[12] B. Zhao, Q. Song, J. Li, Q. Sun and W. Liu, "Full-process operation, control, and experiments of modular high-frequency-link DC transformer based on dual active bridge for flexible MVDC distribution: A practical tutorial," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6751-6766, Sept. 2017.

[13] H. Geng, S. Li, C. Zhang, G. Yang, L. Dong and B. Nahid-Mobarakeh, "Hybrid communication topology and protocol for distributed-controlled cascaded H-bridge multilevel STATCOM," in *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 576-584, Jan.-Feb. 2017.

[14] T. Modeer, S. Norrga and H. P. Nee, "High-voltage tapped-inductor buck converter auxiliary power supply for cascaded converter submodules," *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, 2012, pp. 19-25.

[15] D. Dujic *et al*., "Power electronic traction transformer-low voltage prototype," in *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5522-5534, Dec. 2013.

[16] T. Besselmann, A. Mester, and D. Dujic, "Power Electronic Traction Transformer: Efficiency Improvements Under Light-Load Conditions," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3971-3981, August 2014.