Improved Zero-Crossing Distortion of A Boundary-Conduction-Mode Boost Converter with Digital Average-Current-Mode Control

Robert T. Ryan, John G. Hayes
Power Electronics Research Laboratory
School of Engineering
University College Cork
Cork, Ireland
john.hayes@ucc.ie
robertryan@umail.ucc.ie

Richard J. Morrison, Diarmuid N. Hogan
Excelsys Technologies
27 Eastgate Business Park
Little Island
Cork, Ireland
richardmorrison@excelsys.com
diarmuidhogan@excelsys.com

***Abstract*—Constant-on-time control (COTC) is typically used to regulate the output voltage of boundary-conduction-mode (BCM) boost converters, while also ensuring the input line current has a near-unity power factor. The downside of COTC is that the input line current drawn by the converter suffers from zero-crossing distortion. This distortion of the input line current reduces the converter's power factor. In this work, a digital closed-loop control scheme is designed to reduce the zero-crossing distortion based on the average-current-mode control (ACMC) technique, which is commonly used in the control of continuous-conduction-mode (CCM) boost converters. A digital controller is designed for a 600 W interleaved BCM boost converter using a TMS320F28069 microcontroller. The performance of the ACMC controller is compared to that of a COTC controller.**

Keywords - Power-factor correction, boost converter

I. Introduction

For power-factor correction (PFC) applications in the power range of 300 W to 600 W, the combination of a bridge rectifier and an interleaved BCM boost converter is a popular topology [1]–[6]. The BCM boost converter offers advantages such as small inductor size, and low switching losses due to zero-voltage and near-zero-voltage switching. The interleaving of two channels makes the converter a more suitable choice for higher power applications up to 600 W by reducing the output capacitor current ripple, and also reducing the input current ripple, thus allowing a smaller differential-mode electromagnetic interference (EMI) filter to be used [7]. At higher power levels, the high rms switch and inductor currents degrade the use of the BCM topology, making the CCM boost converter a more popular choice [8]–[10].

The output voltage of the BCM boost topology is normally regulated using COTC [11]–[13]. However, the resonance between the MOSFET drain-source capacitance and boost inductor causes a zero-crossing distortion of the input line current which degrades the power quality of the converter [14], [15]. Different methods have been proposed in literature to reduce the zero-crossing distortion of the BCM boost converter. Previous analog solutions have attempted to reduce the input line current zero-crossing distortion, by increasing the converter's on-time based on the instantaneous value of the input voltage [16], [17]. Other analog solutions have used similar methods, where the on-time is increased, but based on a combined function of instantaneous input voltage and operating power level [18], [19]. In [20], [21] a mixed analog-digital solution is used that increases the on-time of the converter based on the instantaneous input voltage and power level. Fully digital solutions have also been proposed to reduce the zero-crossing distortion. A digital solution described in [22] and[23] uses complex algorithms to calculate the additional on-time required to cancel the effects of the boost inductor and MOSFET drain-source capacitance resonance.

All of the aforementioned schemes work very well at reducing the zero-crossing distortion of BCM boost converters, with different trade-offs in performance and implementation requirements between the different solutions. However, all of these solutions are fundamentally limited by the fact they are all open-loop control methods. Therefore they all require accurate feedforward algorithms to adjust the on-time by the correct amount to remove the zero-crossing distortion.

ACMC is a technique that has been widely adopted for the control of CCM boost converters used in PFC applications [24]–[26]. An analog solution is proposed in [27] and [28] where a closed-loop ACMC scheme is implemented to reduce the line current zero-crossing distortion based around the use of a sample-and-hold scheme to generate the current reference by sampling

978-1-5386-1180-7/18/$31.00 ©2018 IEEE

the inductor current at the midpoint of the on-time.

The work presented in this paper demonstrates a digital closed-loop control scheme, based on ACMC using an adaptive current controller gain, that significantly reduces the zero-crossing distortion of the input line current. As this is a digital solution the current reference for the ACMC scheme can easily be generated by multiplying the sensed instantaneous line voltage by the voltage compensator output in microcontroller software. This paper is structured as follows. Section II describes how the valley switching operation of the converter creates a zero-crossing distortion in the line current. Section III introduces the control structure of the proposed ACMC scheme. Section IV describes the current compensator design. Lastly, Section V gives experimental results comparing the proposed ACMC scheme to a COTC scheme.

II. Zero-Crossing Distortion

Fig. 1 shows the simplified circuit diagram of one channel of the interleaved boost converter, including the MOSFET drain-source capacitance C_{ds}.

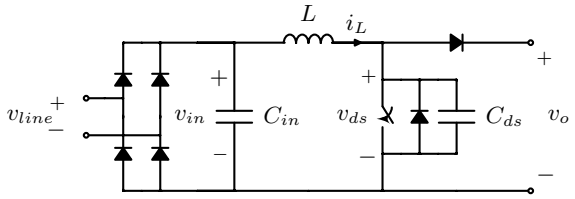

Fig. 1: Single channel of the boost converter and input rectifier including MOSFET drain-source capacitance.

During a single switching cycle of the boost converter operation, the inductor current linearly charges when the MOSFET is turned on. When the MOSFET is turned off the inductor discharges into the boost output capacitor through the boost diode until the inductor current reaches zero and the boost diode becomes reversed biased. At this point, the voltage across the MOSFET drain-source capacitance v_{ds} charges to the output voltage v_o. As $v_o > v_{in}$, the energy stored in the capacitance C_{ds} discharges back through the boost inductor causing a negative inductor current. The zero-voltage detection circuitry is designed to allow the energy stored in C_{ds} to discharge as much as possible to the input capacitor C_{in}, before turning the MOSFET back on. This allows the energy stored in C_{ds} to be saved, which improves converter's efficiency. However, this effect makes the inductor current i_{L1} waveform look as shown in Fig. 2, which shows the typical shape of the inductor current over several switching cycles for high and low instantaneous input voltages.

The downside to this scheme, is that when using a simple COTC scheme during the zero crossings of the input line voltage, the average input current drawn

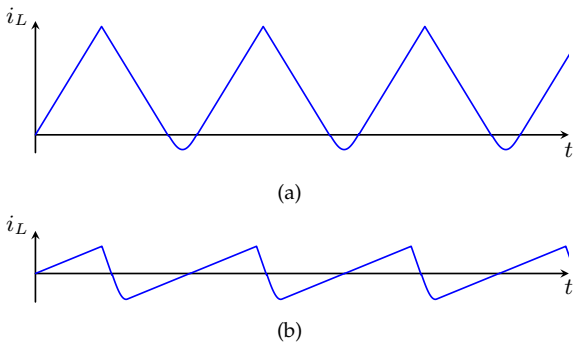

Fig. 2: Inductor current shape at (a) high and (b) low instantaneous input voltages.

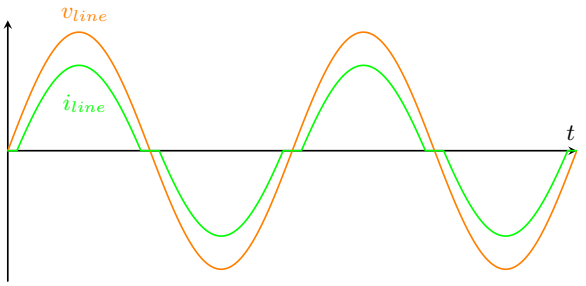

Fig. 3: Line current i_{line} and line voltage v_{line} waveforms with zero-crossing distortion.

by the converter is zero. This creates a zero-crossing distortion in the input line current, which reduces power factor. The shape of the input line current is displayed in Fig. 3.

III. Controller Structure

Fig. 4 and Fig. 5 show the controller structures for the ACMC and COTC schemes, respectively. ACMC works by multiplying the sensed instantaneous input voltage by the output of the voltage compensator v_c to generate the current reference signal i_{ref}. The reference signal is then compared to the sensed input current to generate an error signal that passes through a current compensator to calculate the correct on-time that can accurately track the reference current. In the COTC scheme, the on-time is given by the output of the voltage compensator. For both schemes, the on-time modulator block is used to ensure the correct 180° degree phase shift is maintained [29], while zero-current-detection circuitry on each inductor ensures the converter always operates in BCM. Each control scheme also uses a voltage compensator to regulate the output voltage of the boost converter [30].

IV. CURRENT COMPENSATOR

Over a full-line cycle the inductor currents i_{L1} and i_{L2}, and the input voltage v_{in} look as shown in Fig. 6. Ignoring the effects of the resonance between the boost inductors and C_{ds}, the average instantaneous

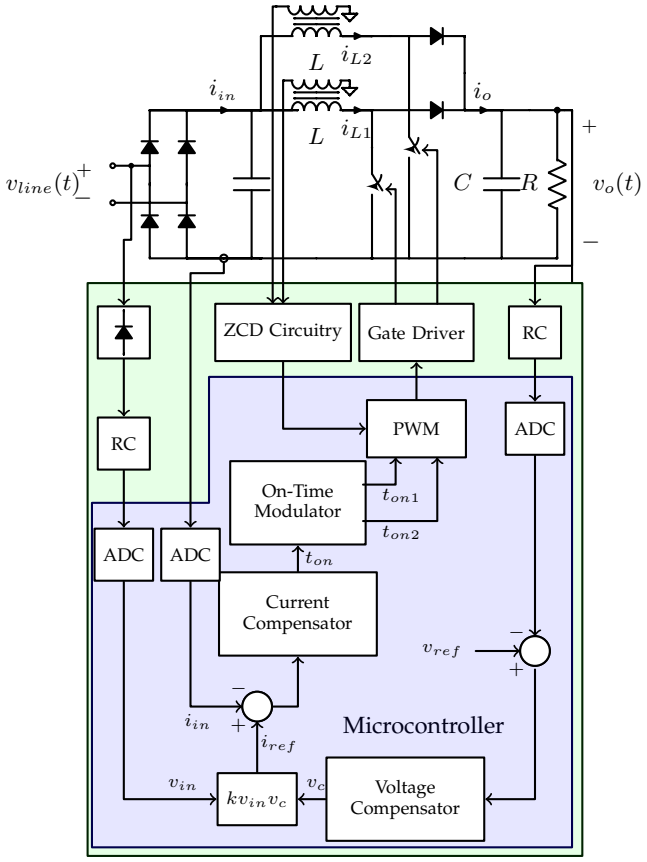

Fig. 4: Controller ftructure of ACMC.

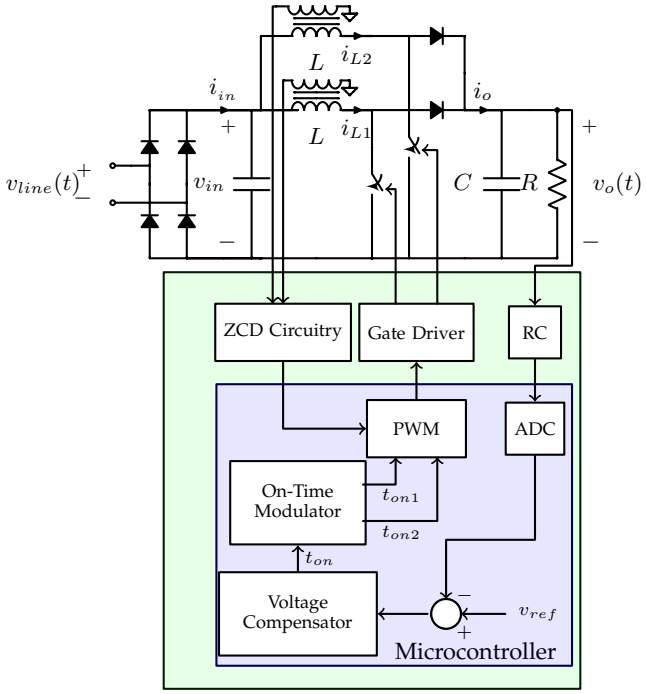

Fig. 5: Controller structure of COTC.

input current i_{in} is given by the peak of the inductor currents, for the interleaved converter.

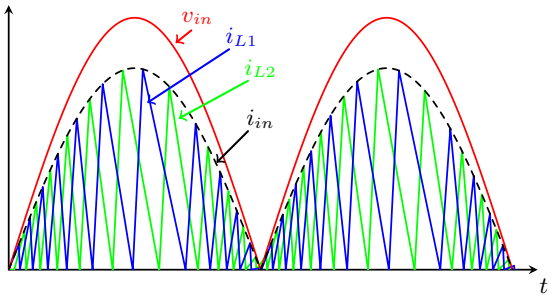

Fig. 6: Inductor currents over many switching cycles

Fig. 7 shows how the inductor current of a single channel i_{L1} looks over a single switching cycle. The average input current of the interleaved BCM boost converter is given by twice the average of i_{L1}, and can be calculated by using (1).

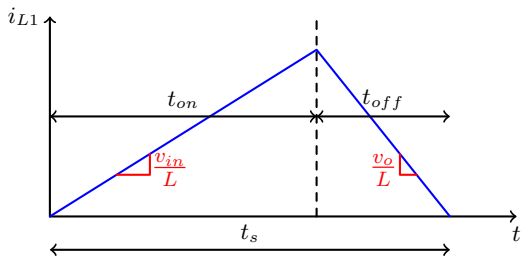

Fig. 7: Inductor current over single switching cycle.

$$i_{in} = \frac{t_{on} v_{in}}{L} \tag{1}$$

where t_{on} is the switch on-time and L is the value of the boost inductance. This equation defines the time-averaged system model, and demonstrates how i_{in} is a function of the input to the system t_{on} and the disturbance v_{in}. Linearising (1) about a dc operating point, the system can be described by the following linear time-averaged model.

$$\widetilde{i_{in}} = \frac{V_{in}}{L} \widetilde{t_{on}} \tag{2}$$

where V_{in} is the dc operating point of the instantaneous input voltage. By converting (2) into the Laplace domain, the open-loop transfer function of the power stage can be described as follows.

$$\frac{I_{in}(s)}{T_{on}(s)} = \frac{V_{in}}{L} \tag{3}$$

The input current to the boost converter contains a large amount of current ripple due to the triangular shapes of the inductor currents. Therefore, to remove this ripple, the total input current is sensed through an analog low-pass filter with a single pole at ω_p, before being passed onto the microcontroller ADC. To obtain

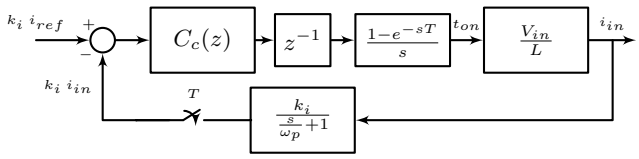

Fig. 8: Control block diagram of the current loop.

a fast current compensator bandwidth, it is important to place the pole ω_p at as high a frequency as possible, but still sufficiently low enough to attenuate the switching frequency ripple from the input current. The switching frequency of the converter described in this work varies from 75 kHz up to 590 kHz. Therefore, the pole w_p has been placed at $\frac{1}{5}$ the minimum switching frequency at 15 kHz.

Fig. 8 shows the control block diagram of the current loop. The sensed input current is subtracted from the reference signal to calculate the error signal which is fed into the current compensator. $C_c(z)$ is the current compensator transfer function implemented in microcontroller software. The microcontroller introduces a delay of z^{-1} and a zero order hold (ZOH). The transfer function of the current sense circuitry is given by $\frac{k_i}{\frac{s}{\omega_p}+1}$. Where k_i is the gain of the current sense circuitry.

Based on Fig. 8, the full compensated open-loop transfer function $T_c(z)$ that defines the system, can be written as,

$$T_c(z) = z^{-1}C_c(z)Z\left\{\frac{1-e^{-sT}}{s}\frac{V_{in}}{L}\frac{k_i}{\frac{s}{\omega_p}+1}\right\}$$
$$= z^{-1}C_c(z)k_i\frac{V_{in}}{L}\frac{1-e^{-\omega_p T}}{z-e^{-\omega_p T}} \quad (4)$$

where T is the sampling period of the input current.

The current compensator transfer function is a type II compensator whose transfer function in the Laplace domain is given by;

$$C_c(s) = \frac{K}{s}\frac{1+a\tau s}{1+\tau s} \quad (5)$$

The bi-linear transformation $s = \frac{2}{T}\frac{z-1}{z+1}$was substituted into (5) to calculate a transfer function for $C_c(z)$ in the z-domain with similar characteristics to that of the type II compensator. Therefore, $C_c(z)$ can be calculated by;

$$C_c(z) = k_c\frac{z+1}{z-1}\left(\frac{z(1+\frac{2a\tau}{T})+(1-\frac{2a\tau}{T})}{z(1+\frac{2\tau}{T})+(1-\frac{2\tau}{T})}\right) \quad (6)$$

The a and τ terms in equation (6) were chosen to inject 45° degrees of phase at the open-loop system cross-over frequency ω_c, and were calculated by a = 5.82 and $\tau = \frac{1}{\omega_c\sqrt{a}}$, where ω_c is the open-loop cross-over frequency. The open-loop system cross-over frequency must be less than the pole ω_p to ensure the

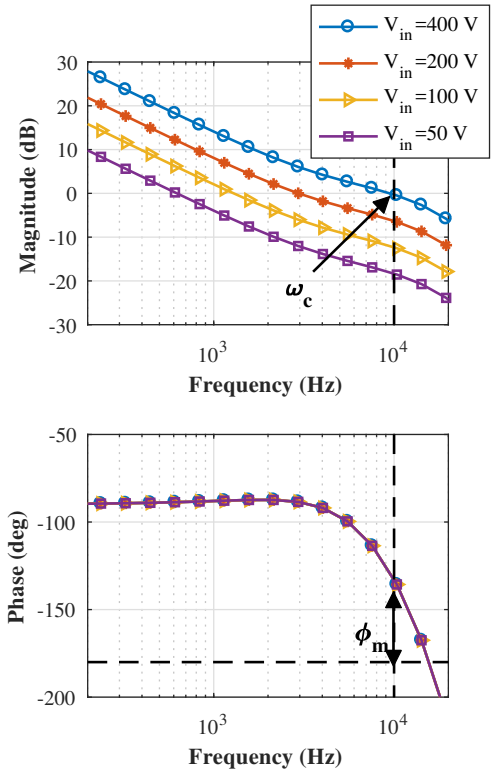

Fig. 9: Compensated open-loop system bode plot $T_c(z)$ variation with instantaneous input voltage.

phase margin of the system ϕ_m is greater than 0° for stability. Therefore ω_c was placed at 10 kHz.

The term k_c in equation (6) was found by calculating the system open-loop gain at $\omega = \omega_c$, which equals 1, as described in (7),

$$|T_c(e^{j\omega_c T})| = 1 \quad (7)$$

Substituting the terms in (4) and (6) for $T_c(z)$ and $C_c(z)$ respectively into (7) and re-arranging, the following expression can be found for the digital current compensator gain k_c. k_c is initially calculated at the maximum possible input voltage of 400 V.

$$k_c = \frac{L|e^{j\omega_c T}-1|\,|e^{j\omega_c T}(1+\frac{2\tau}{T})+(1-\frac{2\tau}{T})|\,|e^{j\omega_c T}-e^{-\omega_p T}|}{k_i V_{in}|1-e^{-\omega_p T}|\,|e^{j\omega_c T}+1|\,|e^{j\omega_c T}(1+\frac{2a\tau}{T})+(1-\frac{2a\tau}{T})|} \quad (8)$$

Fig. 9 shows the compensated open-loop Bode plot of the system at different levels of input voltage. It can be observed that as the input voltage drops the controller phase response stays the same, but the cross-over frequency of the system is dramatically decreased from 10 kHz at 400 V, to nearly 600 Hz at 50 V. This is a very undesirable trait, because for the current compensator to successfully reduce the zero-crossing

distortion, which occurs at low levels of input voltage, it must have very fast tracking performance under this condition.

TABLE I: Adaptive gain look-up table for k

$\mathbf{V_{in}}$ range	k	$\mathbf{V_{in}}$ range	k
$0 < V_{in} \leq 10$	$\frac{400}{10}$	$40 < V_{in} \leq 60$	$\frac{400}{60}$
$10 < V_{in} \leq 15$	$\frac{400}{15}$	$60 < V_{in} \leq 100$	$\frac{400}{100}$
$15 < V_{in} \leq 20$	$\frac{400}{20}$	$100 < V_{in} \leq 200$	$\frac{400}{200}$
$20 < V_{in} \leq 30$	$\frac{400}{30}$	$200 < V_{in} \leq 400$	$\frac{400}{400}$
$30 < V_{in} \leq 40$	$\frac{400}{40}$		

To counteract this undesirable behaviour at low input voltage, an adaptive gain k was used to adjust the gain of the current compensator. The value of k was varied inversely with input voltage by means of a look-up table to ensure that as the input voltage decreased, k increased to ensure the cross-over frequency of the system remained near 10 kHz. Table I shows the look-up table used to calculate the gain k.

V. Experimental Results

A 600 W prototype interleaved BCM PFC converter was built and is capable of using either COTC and ACMC controller structures. Fig. 10 shows the waveforms of v_o, v_{in}, i_{in} and i_{L1}, when the converter is operating at rated power, with an input rms line voltage of 200 V, using the ACMC scheme. The shape of i_{L1} demonstrates correct BCM operation of the converter, and the shape of i_{in} demonstrates correct interleaving operation of the converter.

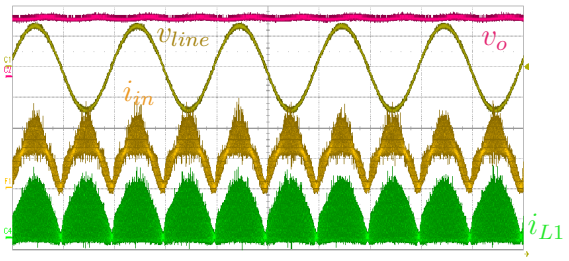

Fig. 10: Waveforms of v_o, v_{in}, i_{in} and i_{L1} at P_o = 600 W and a rms line voltage of 200 V (v_o: 200 V/div, v_{line}: 200 V/div, i_{in}: 5 A/div, i_{L1}: 5 A/div, timebase: 10 ms/div).

A TMS320F28069 microcontroller was used to implement the algorithms for the current compensator, voltage compensator and on-time modulator. The current compensator and on-time modulator were executed at a rate of 100 kHz, while the voltage compensator was executed in a slower interrupt at 10 kHz.

Fig. 12 compares the power quality of the input line current for both the COTC and ACMC schemes, at a rms line voltage of 140V and P_o = 350 W. At this operating point the ACMC scheme has a power factor of 0.997, while the COTC scheme has a power factor of 0.993. The direct comparison clearly displays how the ACMC scheme successfully reduces the zero-crossing distortion at this operating condition.

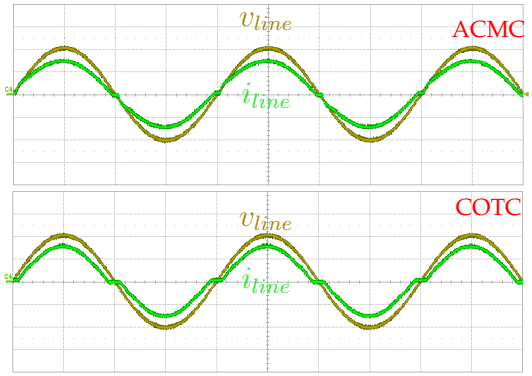

Fig. 11: v_{line} and i_{line} at P_o = 350 W and 140 V rms line voltage, for ACMC (upper) and COTC (lower) (v_{line}: 100 V/div, 1_{line}: 2 A/div, timebase: 5 ms/div).

The reason for this improvement in power quality, is that at the line current zero crossings, the current compensator in the ACMC control structure, will increase t_{on} to draw more line current. Whereas, in the COTC scheme t_{on} remains constant during the line current zero-crossing intervals. A comparison of the variation in t_{on} over four half-line cycles, for ACMC and COTC is shown in Fig. 12.

Although the ACMC control scheme gave significant improvement in the power quality at low-input voltages, the same improvement did not occur at higher input voltages. Fig. 13 compares the power quality of the ACMC and COTC schemes at the same output power of 350 W, but at a higher rms line voltage of 260 V. In this case the COTC scheme actually provided a better power factor of 0.991, when compared to the ACMC control scheme which had a power factor of 0.986.

Fig. 14 shows a direct comparison of power factor of the two control schemes against load, for three different input rms line voltages of 140 V, 200 V and 260 V. It is clear from looking at the 140 V case that the ACMC scheme draws a much better power factor than the COTC scheme. When the rms line voltage is 200 V, the ACMC scheme draws better power factor at higher power levels while the COTC scheme has better power factor at lower power levels. At 260 V, the COTC scheme has slightly better power factor in all cases. When the input rms voltage is higher the current distortion of the input filter capacitor becomes the main cause of distortion in the line current. Although the ACMC scheme can remove the distortion caused around the zero-crossing of the line current it cannot help with the input filter capacitor related distortion.

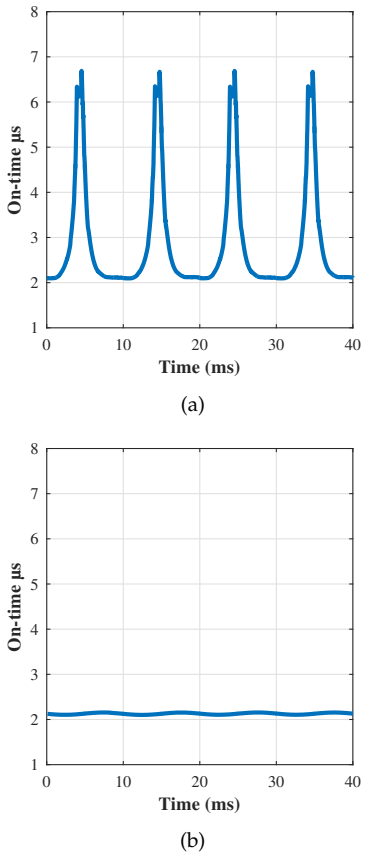

Fig. 12: Measured on-time variation at P_o = 600 W and a rms line voltage of 140 V when using (a) ACMC and (b) COTC.

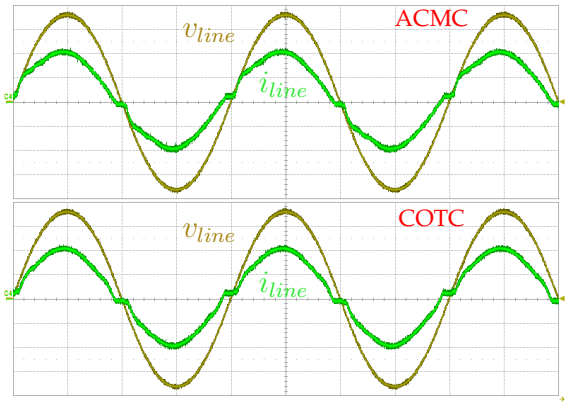

Fig. 13: v_{line} and i_{line} at P_o = 350 W and 260 V line voltage, for ACMC (upper) and COTC (lower) (v_{line}: 100 V/div, 1_{line}: 1 A/div, timebase: 5 ms/div).

Another effect that begins to take hold at higher input voltage is the resolution of the sensed current signal seen by the microcontroller gets worse, this also degrades the power factor of the ACMC scheme at higher input voltages and lower power levels. Overall the ACMC scheme significantly improved the power quality at high power and low input voltage, but slightly degrades power under low power and high input voltage conditions.

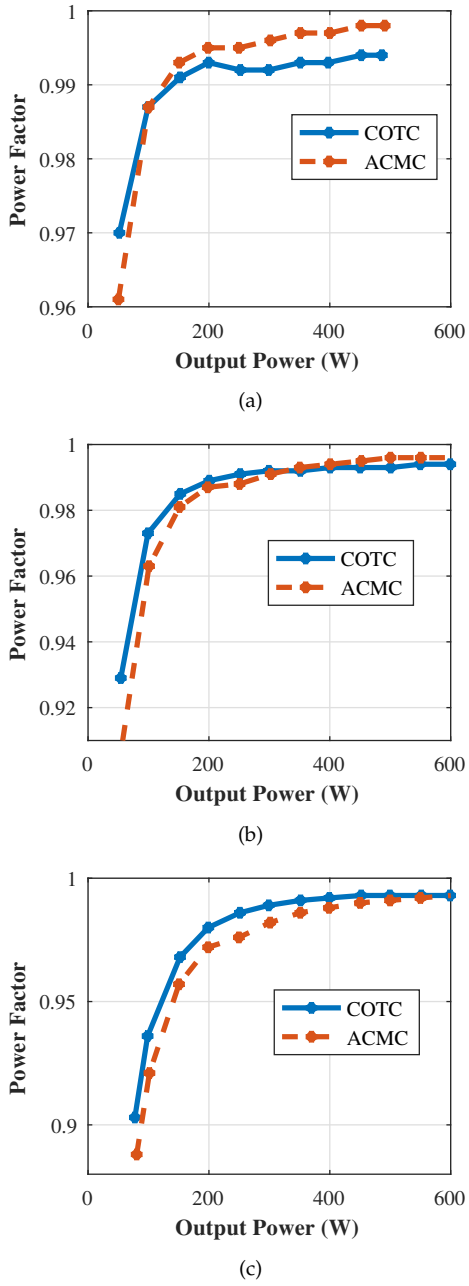

Fig. 14: Measured power factor versus output power for COTC and ACMC controllers at an input rms line voltage of (a) 140 V, (b) 200 V, and (c) 260 V.

Both the ACMC and COTC control implementations drew very low levels of input current harmonics that were well below the limits set by the Class A EN61000-3-2 standard. A comparison of the COTC, ACMC and EN61000-3-2 harmonic limits is given in Fig. 15. Only odd harmonics are shown, as even order harmonics were of all near zero for both COTC and ACMC schemes. The current harmonics were measured at a

rms line voltage of 230 V, and a 600 W output power.

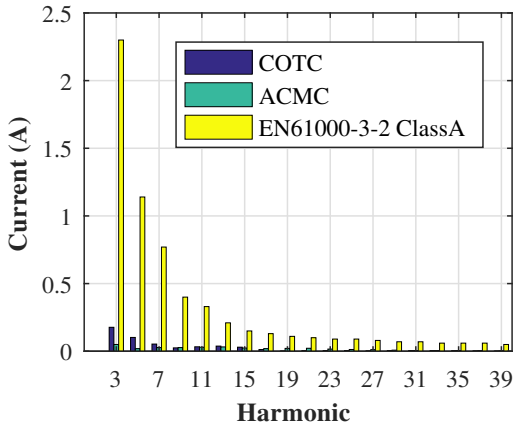

Fig. 15: Comparison of input current harmonics measured at P_o = 600 W and an input rms line voltage of 230 V with the EN6100-3-2 Class A limits.

Fig. 16 gives a direct comparison of the current harmonics drawn using COTC and ACMC, also at 230 V rms line voltage, and 600 W output power. The ACMC scheme draws significantly less current at lower harmonic levels due to the reduction of the zero crossing distortion, but also draws more current for the higher order harmonics This is because the bandwidth of the current compensator in the ACMC control scheme is 10 kHz, so the on-time calculated with ACMC will have some components up to that frequency, whereas with the COTC scheme, the on-time is calculated by the voltage compensator which has a much lower bandwidth of 15 Hz, which strongly filters out all the frequencies of the higher-order harmonics.

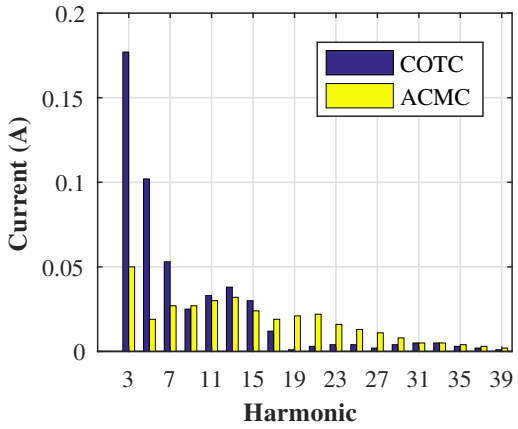

Fig. 16: Comparison of input current harmonics measured at P_o = 600 W and an input rms line voltage of 230 V.

VI. Conclusion

A digital closed-loop control scheme to reduce the zero-crossing distortion of a BCM boost converter for PFC applications, has been presented. The open-loop system model for the system was derived, and a current compensator was designed for the ACMC scheme. The relationship between the operating input voltage and the controller performance was examined, demonstrating how at low values of the instantaneous input voltage, the cross-over frequency of the system is severely reduced. An adaptive gain parameter was adopted in the ACMC scheme to improve the performance of the controller, by ensuring the gain changed to adjust the cross-over frequency of the system in response to the input voltage.

Experimental results were demonstrated on a 600 W interleaved BCM boost prototype and show a strong increase in power factor for high output power and low input rms voltage conditions when replacing the COTC control scheme with ACMC. However the ACMC scheme slightly degraded power factor at low-power and high input voltage conditions.

The ACMC also requires the microcontroller to run a current compensator algorithm at a fast rate of 100 kHz. This means the ACMC scheme requires greater CPU bandwidth than the COTC scheme, making this advanced control technique more difficult to implement on a low-cost microcontroller.

Acknowledgment

The authors would like to thank Excelsys Technologies for invaluable support, co-funding and use of equipment during this work.

The authors would like to acknowledge the Irish Research Council for co-funding to make this project possible.

References

[1] J. W. Shin, G. S. Seo, B. H. Cho, and K. C. Lee, "Digitally controlled open-loop master-slave interleaved boost PFC rectifier," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 304–309, Feb 2012.

[2] J. Jang, S. K. Pidaparthy, S. Lee, and B. Choi, "Performance of an interleaved boundary conduction mode boost PFC converter with wide band-gap switching devices," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, pp. 1–6, Nov 2015.

[3] H. Choi and L. Balogh, "A cross-coupled master-slave interleaving method for boundary conduction mode (BCM) PFC converters," *IEEE Transactions on Power Electronics*, vol. 27, pp. 4202–4211, Oct 2012.

[4] X. Xu and A. Q. Huang, "A novel closed-loop interleaving strategy of multiphase critical mode boost PFC converters," in *2008 IEEE Twenty-Third Annual Applied Power Electronics Conference and Exposition (APEC)*, pp. 1033–1038, Feb 2008.

[5] C.-Y. Lim, J. H. Kim, Y. Jeong, D.-K. Kim, H.-S. Youn, and G. W. Moon, "A high efficiency critical mode boost PFC using a variable inductor," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, pp. 2792–2797, May 2016.

[6] Y. L. Chen, H. J. Chen, Y. M. Chen, and K. H. Liu, "A stepping on-time adjustment method for interleaved multichannel PFC converters," *IEEE Transactions on Power Electronics*, vol. 30, pp. 1170–1176, March 2015.

[7] X. Xu, W. Liu, and A. Q. Huang, "Two-phase interleaved critical mode PFC boost converter with closed loop interleaving strat-

egy," *IEEE Transactions on Power Electronics*, vol. 24, pp. 3003–3013, Dec 2009.

[8] J. C. Hernandez, L. P. Petersen, and M. A. E. Andersen, "A comparison between boundary and continuous conduction modes in single phase PFC using 600 V range devices," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*, pp. 1019–1023, June 2015.

[9] H. C. Sartori, J. E. Baggio, H. L. Hey, J. R. Pinheiro, and F. Beltrame, "Integrated methodology design to improve the efficiency and reduce volume of the CCM PFC boost converters with pre-sizing settings," in *2015 IEEE 24th International Symposium on Industrial Electronics (ISIE)*, pp. 1378–1385, June 2015.

[10] J. Zhang, M. M. Jovanovic, and F. C. Lee, "Comparison between CCM single-stage and two-stage boost PFC converters," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol. 1, pp. 335–341 vol.1, Mar 1999.

[11] S. P. Yang, S. J. Chen, and C. M. Huang, "Small-signal modeling and controller design of BCM boost PFC converters," *Proceedings of the 2012 7th IEEE Conference on Industrial Electronics and Applications, ICIEA 2012*, pp. 1096–1101, 2012.

[12] Y. C. Hsu, D. Chen, S. F. Hsiao, H. Y. Cheng, and C. S. Huang, "Modeling of the control behavior of current-mode constant on-time boost converters," *IEEE Transactions on Industry Applications*, vol. 52, pp. 4919–4927, Nov 2016.

[13] B. Choi, S.-S. Hong, and H. Park, "Modeling and small-signal analysis of controlled on-time boost power-factor-correction circuit," *IEEE Transactions on Industrial Electronics*, vol. 48, pp. 136–142, Feb 2001.

[14] C. Adragna, L. Huber, B. T. Irving, and M. M. Jovanovic, "Analysis and performance evaluation of interleaved DCM/CCM boundary boost PFC converters around zero-crossing of line voltage," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, pp. 1151–1157, Feb 2009.

[15] L. Huber, B. T. Irving, and M. M. Jovanovic, "Effect of valley switching and switching-frequency limitation on line-current distortions of DCM/CCM boundary boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 24, pp. 339–347, Feb 2009.

[16] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-time control of the critical conduction mode boost power factor correction converter to improve zero-crossing distortion," in *2005 International Conference on Power Electronics and Drives Systems*, vol. 2, pp. 1542–1546, Nov 2005.

[17] Y. Li, Y. Yang, Z. Zhu, and W. Qiang, "Zero-crossing distortion analysis in one cycle controlled boost PFC for low THD," in *ASIC (ASICON), 2011 IEEE 9th International Conference on*, pp. 661–664, Oct 2011.

[18] J. C. Tsai, C. L. Chen, Y. T. Chen, C. L. Ni, C. Y. Chen, K. H. Chen, C. J. Chen, and H. L. Pan, "Perturbation on-time (POT) control and inhibit time control (ITC) in suppression of THD of power factor correction (PFC) design," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, Sept 2011.

[19] J. C. Tsai, C. L. Chen, Y. T. Chen, C. L. Ni, C. Y. Chen, and K. H. Chen, "Perturbation on-time (POT) technique in power factor correction (PFC) controller for low total harmonic distortion and high power factor," *IEEE Transactions on Power Electronics*, vol. 28, pp. 199–212, Jan 2013.

[20] Z. Guo, X. Ren, H. Gui, Y. Wu, Z. Zhang, and Q. Chen, "A universal variable on-time compensation to improve THD of high-frequency CRM boost PFC converter," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1–6, Sept 2016.

[21] Z. Guo, X. Ren, Y. Wu, Z. Zhang, and Q. Chen, "A novel simplified variable on-time method for CRM boost PFC converter," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1778–1784, March 2017.

[22] J. W. Kim, H. S. Youn, and G. W. Moon, "A digitally controlled critical mode boost power factor corrector with optimized additional on time and reduced circulating losses," *IEEE Transactions on Power Electronics*, vol. 30, pp. 3447–3456, June 2015.

[23] J. W. Kim and G. W. Moon, "Minimizing effect of input filter capacitor in a digital boundary conduction mode power factor corrector based on time-domain analysis," *IEEE Transactions on Power Electronics*, vol. 31, pp. 3827–3836, May 2016.

[24] A. Kar and M. Sengupta, "Design, analysis, fabrication and testing of a 3 szrdskW power factor correction boost rectifier," in *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1–6, Dec 2016.

[25] J. Moldaschl, J. Broulím, and L. Paločko, "Boost power factor correction topology with average current control," in *2014 International Conference on Applied Electronics*, pp. 213–216, Sept 2014.

[26] S. M. O'Driscoll and D. A. Grant, "Combining peak current mode control with average current mode control using digitally assisted analog," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 76–88, March 2014.

[27] Y. L. Chen, Y. M. Chen, and H. J. Chen, "On-time compensation method for CRM/DCM boost pfc converter," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 3096–3100, March 2013.

[28] Y. L. Chen and Y. M. Chen, "Line current distortion compensation for DCM/CRM boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 31, pp. 2026–2038, March 2016.

[29] R. T. Ryan, J. G. Hayes, D. Hogan, and R. Morrison, "A digital closed-loop control strategy for maintaining the 180 phase shift of an interleaved BCM boost converter for PFC applications," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 4927–4934, October 2017.

[30] R. T. Ryan, J. G. Hayes, R. Morrison, and D. Hogan, "Digital control of an interleaved BCM boost PFC converter with fast transient response at low input voltage," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 257–264, October 2017.