Online Condition Monitoring Based Dead-time Compensation for High Frequency SiC Voltage Source Inverter

Jacob Dyer, Zheyu Zhang, Fred Wang, Daniel Costinett, Leon M. Tolbert, and Benjamin J. Blalock
Center for Ultra-Wide-Area Resilient Electric Energy Transmission Networks (CURENT)
Department of Electrical Engineering and Computer Science
The University of Tennessee, Knoxville, TN 37996-2250, USA
jdyer11@vols.utk.edu

***Abstract*— Dead-time, device output capacitance, and other non-ideal characteristics cause voltage error for the midpoint PWM voltage of the semiconductor phase-leg employed in a voltage-source inverter (VSI). Voltage-second balancing is a well-known concept to mitigate this distortion and improve converter power quality. This paper proposes a unique voltage-second balancing scheme for a SiC based voltage source inverter using online condition monitoring of turn-off delay time and drain-source voltage rise/fall time. This data is sent to the micro-controller to be used in an algorithm to actively adjust the duty cycle of the input PWM gate signals to match the voltage-second of the non-ideal output voltage with an ideal output voltage-second. The monitoring system also allows for this implementation to eliminate the need for precise current sensing and allows for the implementation to be load independent. Dynamic current sensing is still a developing technology, and each load has a unique effect on the output voltage distortion. Test results for a 1 kW half-bridge inverter implementing this monitoring system and voltage-second balancing scheme show a 70% enhancement on the error against the ideal fundamental current value of the output current and a 2% THD improvement on the output current low frequency harmonics.**

***Key words*—Condition monitoring (CM), silicon carbide (SiC), voltage source inverter (VSI), current sensing, dead-time compensation, voltage-second balancing**

I. INTRODUCTION

VOLTAGE source converter (VSC) is a common topology used in power electronic converter design. Its basic building block is a phase-leg, which is two series-connected power semiconductors. Then the various types of converters are enabled with a dc voltage source across the lower and upper terminals of the phase-leg and an inductor, as the dc or ac current source, connected to the middle point of the phase leg. In recent years, a shift has been taking place where silicon carbide (SiC) power semiconductors have replaced traditional silicon (Si) power semiconductors in VSCs [1]. This is because SiC offers faster switching capabilities, increased junction operating temperature, increased blocking voltages, and lower on-resistance.

However, a trade-off from higher switching frequency is PWM voltage distortion because of non-ideal switching commutation in the converter; therefore, dead-time compensation, a voltage distortion reduction scheme, is advantageous to improve converter performance [2]. The basic idea behind dead-time compensation (DTC) is to mitigate the negative distortion effects on fundamental frequency voltage/current amplitude caused by the dead-time and other non-ideal characteristics of the switching devices and overall converter.

One major method of dead-time compensation is using the voltage-second balance theory [3-6]. All of these papers analyze what causes the midpoint PWM voltage to distort from the ideal pulse square waveform and how to best compensate for the distortion this causes on the converter. Limitations, however, include the need for a high bandwidth current transducer with inaccurate dynamic current sensing and/or offline model-based implementation, which potentially does not account for variables involved in creating the voltage distortion like the load condition's effect on the voltage distortion.

Another common dead-time compensation scheme is using a feedback controller that sends the output characteristics back to the controller and compares to a reference to compensate for this distortion [7, 8]. This method is limited, especially in high frequency applications, because of the slow response time aspect of feedback controllers. Also, these methods require high control bandwidth and a complex controller that limit the flexibility of this type of compensation scheme.

This paper presents a feedforward voltage-second balancing strategy from online condition monitoring data of SiC devices employed in a high frequency VSI application to improve power quality. First, the factors causing output voltage distortion are analyzed. Then, the proposed voltage-second balancing scheme based on online monitored data is detailed. Finally, experimental results of fundamental voltage/current amplitude improvement and THD reduction are shown for a SiC based 1 kW half-bridge inverter with a fixed load.

II. VOLTAGE DISTORTION MODELING

A. Derivation of Voltage-Second Area

For phase-leg configurations of SiC semiconductors in power converters, the dead-time between the two devices is necessary to prevent both devices from turning on and causing shoot-through failures; however, it causes issues in converter performance. Dead-time (t_{dt}) adds voltage distortion at the

midpoint of the phase-leg. The ideal midpoint voltage of a phase-leg is meant to mirror the input PWM signal; however, the device parasitic capacitance and non-ideal characteristics of the inductive load along with the previously mentioned dead-time cause the midpoint voltage to become distorted from the input PWM signal. The model for the distorted voltage is shown in detail in Fig. 1 showing the process from PWM control signals to power semiconductor device switching signals, which includes the effect of dead-time (t_{dt}), propagation delay (t_{pd}), turn on/off delay time (t_{d_off}, t_{d_on}), voltage rise/fall time or otherwise called voltage commutation time (t_{vc}), and the body diode voltage effect (V_{diode}). Although the voltage distortion process has been evaluated in some previous research, few have considered the non-ideal characteristics of the inductive load and the parasitic capacitance of the switching device, especially a SiC switching device.

Since this work is implementing compensation based on the voltage-second balancing theory, the expressions that are derived are based upon the voltage-second area lost/gained in each dead-time interval. One assumption made in this work is the cancelling effect that the control-level propagation delays have on the voltage-second area analysis. It can be reasonably assumed the t_{pd} time is the same for each case in the gate driving process. The derived equations (1)-(3) will be for the case of current flowing into the midpoint of the phase-leg as shown in Fig. 1(b). The voltage-second lost/gained for the low side device turn-off transition and corresponding dead-time interval is given in (1) and (2):

$$VS_{lost\_L(-)} = t_{d\_offL}V_{DC} + \frac{1}{2}t_{vc\_off}V_{DC} \quad (1)$$

$$VS_{gain\_L(-)} = V_{diode}(t_{dt} - t_{d\_offL} - t_{vc\_off}) \quad (2)$$

The voltage-second area gained for the high side device turn-off transition and corresponding dead-time interval is given in (3):

$$VS_{gain\_H(-)} = (V_{DC} + V_{diode})t_{dt} + (V_{DC} + V_{diode})t_{d\_onL} + \frac{1}{2}V_{DC}t_{vc\_on} \quad (3)$$

The derived equations (4)-(6) will be for the case of current flowing out of the midpoint of the phase-leg as shown in Fig. 1(c). The voltage-second lost for the low side device turn-off transition and corresponding dead-time interval is given in (4):

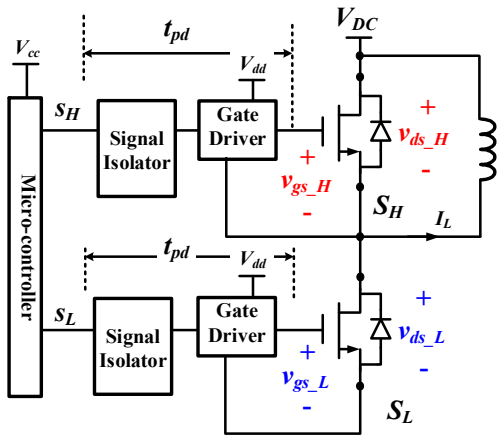
$$VS_{lost\_L(+)} = (V_{DC} + V_{diode})t_{dt} + (V_{DC} + V_{diode})t_{d\_onH} + \frac{1}{2}V_{DC}t_{vc\_on} \quad (4)$$

The voltage-second area lost/gained for the high side device turn-off transition and corresponding dead-time interval is given in (5)-(6):

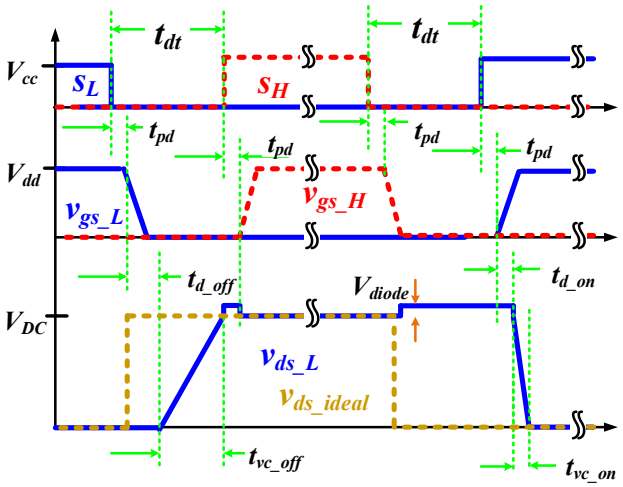
$$VS_{gain\_H(+)} = t_{d\_offH}V_{DC} + \frac{1}{2}t_{vc\_off}V_{DC} \quad (5)$$

$$VS_{lost\_H(+)} = V_{diode}(t_{dt} - t_{d\_offH} - t_{vc\_off}) \quad (6)$$

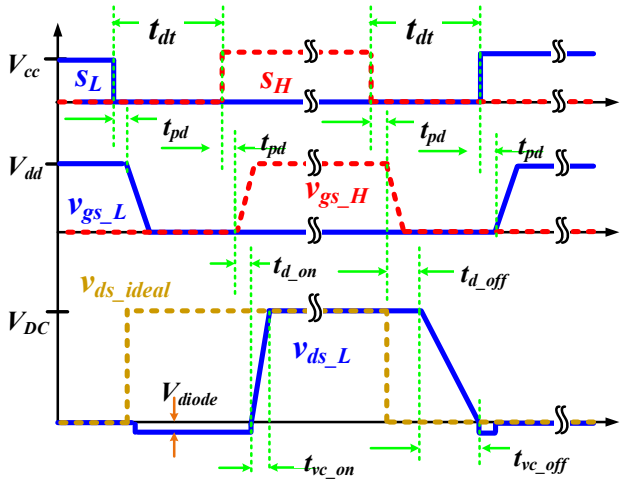
These equations will serve as the basis for the voltage-second balancing equations detailed and implemented in section III. Another assumption made in this work because of its small influence is ignoring the effect of a partial hard turn–on at very low currents (i.e. zero-current clamping phenomenon) [9]. This



(a) SiC phase-leg with gate driver and controls



(b) Switching voltage distortion when current is flowing into the phase-leg



(c) Switching voltage distortion when current is flowing out of the phase-leg

Fig. 1. Model of phase-leg output voltage distortion and resulting voltage-second error

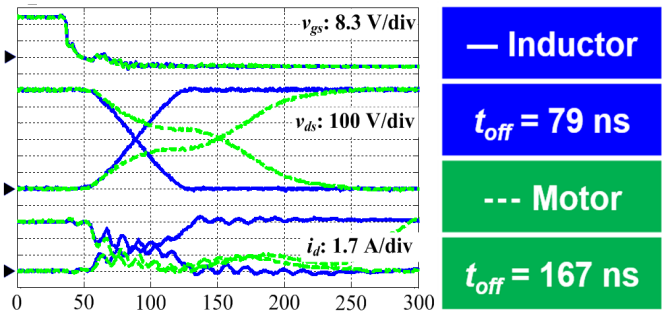


Fig. 2. Effect load conditions have on output voltage distortion from different associated parasitic capacitances

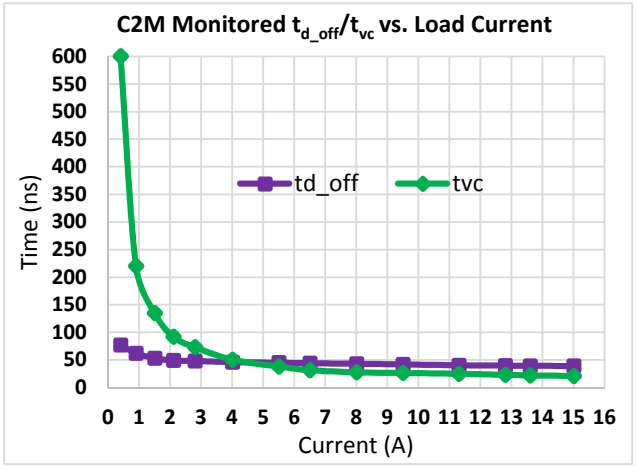


Fig. 3. Monitored test results with respect to load current

work is also able to minimize this phenomenon by setting an initial conservative dead-time in the experimental section.

The next subsection will focus on the voltage rise/fall time component of the voltage-second area expressions and its variation for SiC switching devices, which will lead to a need to online monitor this condition for accurate dead-time compensation results.

B. SiC Specific Issues

Drain-source voltage rise/fall time is highly sensitive to operating conditions and converter load characteristics [10]. Fig. 2 shows the difference in an inverter PWM output voltage switching at the turn-off transition for a motor load and inductor load [11]. The motor load introduces more parasitics that affect the switching performance of the semiconductor device shown with a longer turn-off time compared to the inductor load case.

Fig. 3 demonstrates the non-linear variance effect of parasitic capacitance on the switching time with respect to load current. After obtaining the Fig. 3 monitored data, the output voltage distortion was further examined for cases around the current zero-crossing in Fig. 4. The snapshot is taken around the zero-current crossing to show the different variations on the midpoint PWM voltage distortion based on the current magnitude and polarity.

There are two major sections of a SiC MOSFET turn-off interval relating to the drain-source voltage non-ideal switching. The first section is the turn-off delay time (t_{d_off}), which is the time from when V_{gs} starts to fall to when V_{ds_L} starts to rise/fall. The second interval in the SiC turn-off is the voltage commutation time (t_{vc}), which is the time from when V_{ds_L} either rises from V_{ds_on} to V_{dc} or falls from V_{dc} to V_{ds_on} depending on which phase-leg device turn-off interval is being analyzed. This time is highly dependent on load current because during this time the load current is charging C_{oss} so the amount of load current determines the dv_{ds_L}/dt. Fig. 4 also shows the idea behind the voltage-second lost/gained from the non-ideal switching when looking at the ideal "Area A" compared to the non-ideal "Area B". The next section will show a monitoring system for t_{d_off} and t_{vc} leveraged to balance the voltage-second of the output voltage by adjusting the duty cycle.

III. Voltage-Second Balancing Scheme

A. Online Monitoring System

The unique method of voltage-second balancing is based on an online condition monitoring system for SiC devices [12]. This monitoring system captures the previously mentioned critical timing conditions in the turn-off transition of both devices in the phase-leg. This system diagram is shown in Fig. 5, where the devices are connected to the gate driver and gate drive assist circuits.

The gate drive assist circuits send signals to the edge capture detector, which also receives an isolated high resolution PWM (HRPWM) auxiliary signal. The output is an indicator of edge detection that gets isolated and sent back to the MCU to process

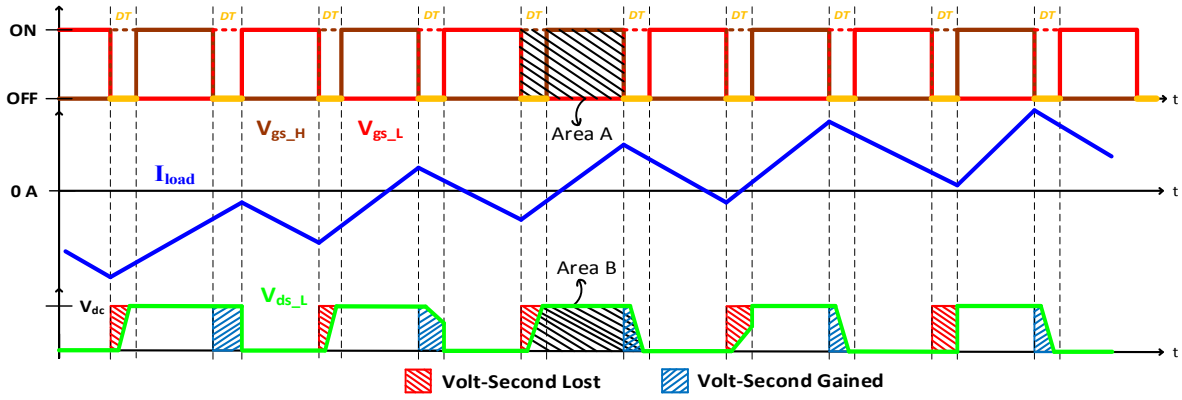


Fig. 4. Inverter operation around the current zero-crossing

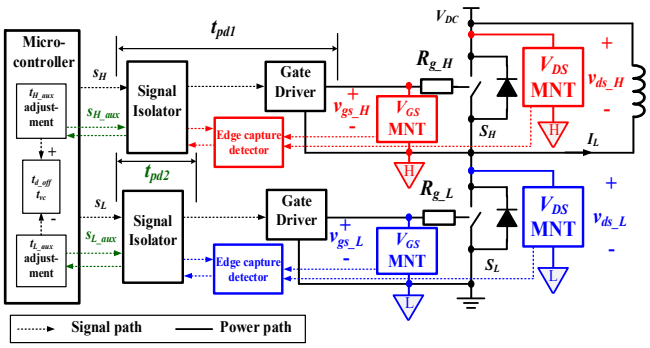


Fig. 5. Online t_{vc} and t_{d_off} monitoring system [11]

the monitored times during the turn-off transition of both devices. These online and accurately monitored times of t_{d_off} and t_{vc} can be leveraged for a competitive dead-time compensation scheme.

As previously shown in Fig. 4, there are different shapes the output voltage can take depending on the load current and dead-time. This is shown in more detail in Fig. 6 showing the two different turn-off transitions for the low side device turn-off as well as the resulting voltage-second error.

B. Current Polarity Detection

Another important feature of the online monitoring system is also shown in Fig. 6 where current polarity can be detected based on data monitored in the online monitoring system. This is historically a difficult issue to accommodate for in VSI systems that implement a dead-time compensation. This is because most available current sensors are limited in bandwidth, thus sensing current around the current zero-crossing is inaccurate and unreliable. Dead-time compensation strategies need to sense current polarity so they can know the type of switching that will occur (i.e. hard or soft switching), and as observed in prior sections, this greatly affects the voltage-second area lost/gained for a given switching cycle. Newer work has used other conditions to indicate the current polarity and thus type of switching [13]. This work leverages the monitored turn-off delay time value to indicate these different types of switching. This can be seen as mentioned in

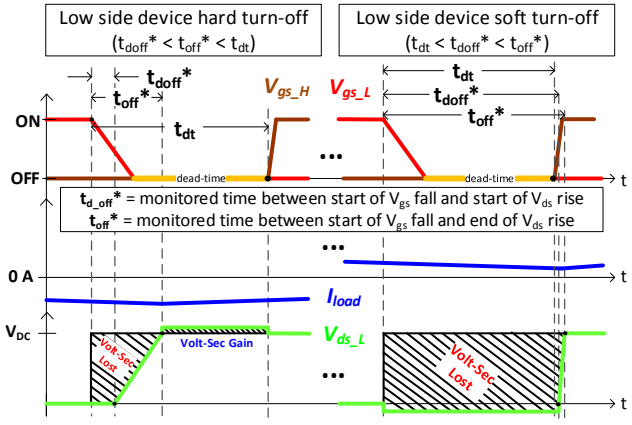


Fig. 6. Detailed voltage-second analysis for low side turn-off and difference in monitored turn-off delay time (t_{d_off}) for positive and negative load current.

Fig. 6 where in the hard turn-off case, the monitored turn-off delay time is the normal turn-off delay time value. However, in the soft turn-off case, the monitored turn-off delay time is not the actual turn-off delay time but the monitoring scheme gives the system a value that is greater than the set dead-time and can indicate a soft turn-off. This is an advantageous approach since it does not add any additional sensors or complexity since the monitoring system is already proven to be necessary for accurate dead-time compensation.

C. Processing in the MCU

Using (1)-(6) from section II and the monitoring system described in the previous two subsections, this work then creates the micro-controller code to enable this dead-time compensation scheme. A TI TMS320F28335 Delfino MCU is used as the micro-controller, and the SPWM control scheme is used to drive the VSI. The goal of the voltage-second balancing scheme is to adjust the duty cycle for a given switching cycle to better match the control side voltage-second with the abnormal power switching side voltage-second that has been analyzed in section II. This is done with (7), which converts the net voltage-second gained/lost into a portion of duty cycle that can be added/subtracted to the initial duty cycle for a given switching cycle,

$$d_{comp} = \frac{\Delta VS}{V_{DC} \times T_s} \tag{7}$$

where the net voltage-second area is given in (8).

$$\Delta VS = VS_{gain} - VS_{lost} \tag{8}$$

Based on the previous evaluation, three switching cycle scenarios are used in the implementation. The first scenario is when the current is flowing into the midpoint of the phase-leg for both dead-time intervals in a switching period. This scenario looks like Fig. 1(b) and produces the voltage-second area lost/gained of (1)-(3). However, for the implementation, the parameters t_{d_on} and t_{vc} are ignored since they are not monitored in the system and are very short time periods. Therefore, when you combine the three equations using (8) and then convert the net voltage-second area into a compensated duty cycle value with (7), the result is (9) that is used in the micro-controller

$$\begin{aligned} Case\ 1{:}\ d_{comp} = &-\left(\frac{t_{d\_offL}}{T_s} + \frac{1}{2}\frac{t_{vc\_off}}{T_s}\right) \\ &+ \frac{V_{diode}}{V_{DC}}\left(\frac{t_{dt}}{T_s} + \frac{t_{d\_offL}}{T_s} + \frac{1}{2}\frac{t_{vc\_off}}{T_s}\right) \\ &+ \left(1 + \frac{V_{diode}}{V_{DC}}\right)\frac{t_{dt}}{T_s} \end{aligned} \tag{9}$$

The second scenario is when current is flowing into the midpoint of the phase-leg for the low side device turn-off but flowing out of the midpoint of the phase-leg during the high side device turn-off (i.e. both cases are hard turn off switching). This scenario is a combination of the hard turn-off parts of Fig. 1(b) and 1(c) and uses the voltage-second area calculations of (1), (2), (5), and (6). In this scenario, no parameters are ignored as this work captures all the time conditions in this case. Therefore, as before the resulting compensated duty cycle is shown in (10).

$$Case\ 2{:}\ d_{comp} = \left(\frac{t_{d\_offH}}{T_s} + \frac{1}{2}\frac{t_{vc\_offH}}{T_s}\right) - \frac{V_{diode}}{V_{DC}}\left(\frac{t_{dt}}{T_s} + \frac{t_{d\_offH}}{T_s} + \frac{1}{2}\frac{t_{vc\_offH}}{T_s}\right) - \left(\frac{t_{d\_offL}}{T_s} + \frac{1}{2}\frac{t_{vc\_offL}}{T_s}\right) + \frac{V_{diode}}{V_{DC}}\left(\frac{t_{dt}}{T_s} + \frac{t_{d\_offL}}{T_s} + \frac{1}{2}\frac{t_{vc\_offL}}{T_s}\right) \quad (10)$$

The third scenario is when current is flowing out of the midpoint of the phase-leg for both dead-time intervals in a switching period. This scenario resembles the switching waveforms shown in Fig. 1(c) and produces the voltage-second area lost/gained given in (4)-(6). Similar to the first scenario, the t_{d_on} and t_{vc} parameters are ignored. Therefore, the compensated duty cycle value calculated based on (4)-(8) yield the expression shown in (11).

$$Case\ 3{:}\ d_{comp} = \left(\frac{t_{d\_offH}}{T_s} + \frac{1}{2}\frac{t_{vc\_off}}{T_s}\right) - \frac{V_{diode}}{V_{DC}}\left(\frac{t_{dt}}{T_s} + \frac{t_{d\_offH}}{T_s} + \frac{1}{2}\frac{t_{vc\_off}}{T_s}\right) - \left(1 + \frac{V_{diode}}{V_{DC}}\right)\frac{t_{dt}}{T_s} \quad (11)$$

IV. Experimental Results

A. 1 kW Half-Bridge Inverter Test Results

A single-phase half-bridge inverter is assembled, as shown in Fig. 7, for testing the power quality improvements of this voltage-second balancing technique. Wolfspeed C2M0080120D SiC devices are employed in the hardware setup. The load condition is a 400 µH inductor with low associated parasitic capacitance in series with a 10 Ω resistor and 4.8 µF capacitor in parallel.

The monitored times of t_{d_off} and t_{vc} are shown in Fig. 8 in an oscilloscope capture during the half-bridge inverter operation. The capture is a low side device hard turn-off, where persistence mode of the oscilloscope was enabled to show the capturing of the drain-source voltage rise time (in green) with

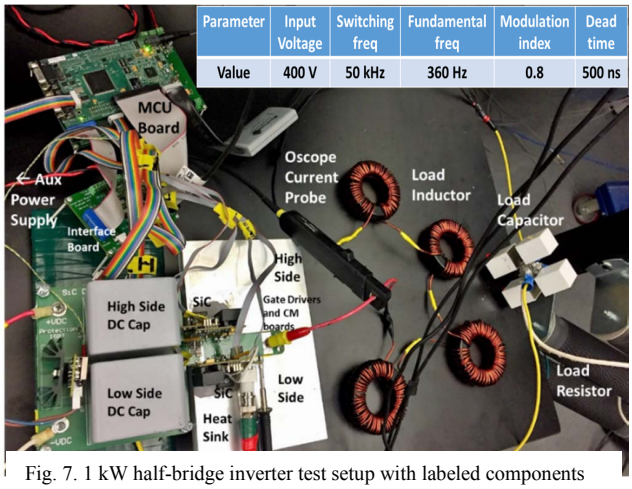


Fig. 7. 1 kW half-bridge inverter test setup with labeled components

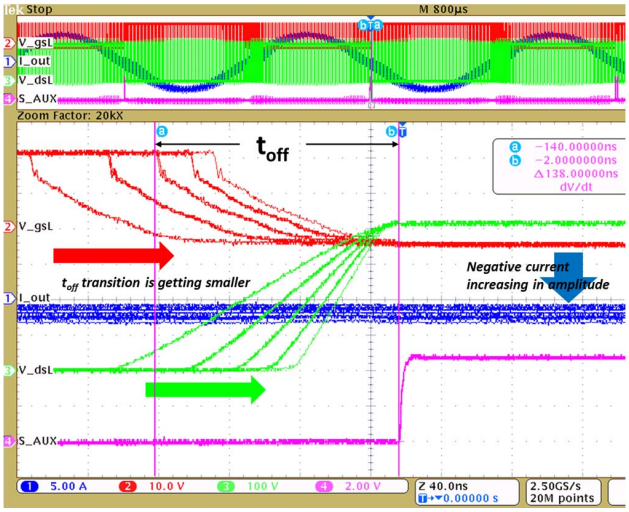


Fig. 8. Voltage rise time monitoring for multiple switching cycles during HB inverter operation.

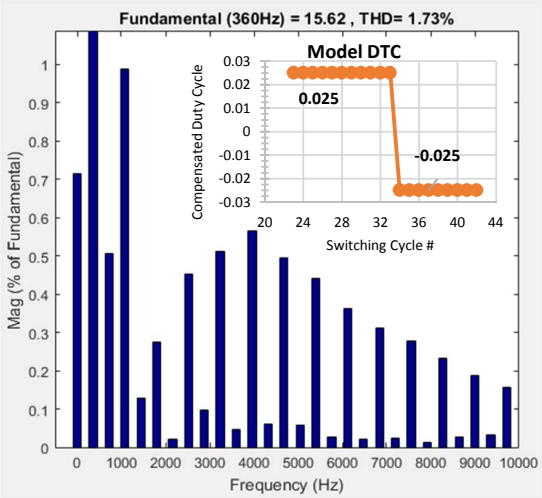
the auxiliary signal (in pink) for multiple switching cycles in a fundamental cycle. The monitored data, processed in the MCU, is used in (9)-(11) to update the duty cycle values for each switching cycle in the fundamental cycle to better match the voltage-second area.

To analyze the power quality improvements from this voltage-second matching, the 1 kW half-bridge inverter output current was obtained under four different conditions: no compensation, classic dead-time model-based compensation, improved model-based compensation, and full monitor-based compensation. The current fundamental value and THD improvement results for the three compensation schemes are shown in Fig. 9.

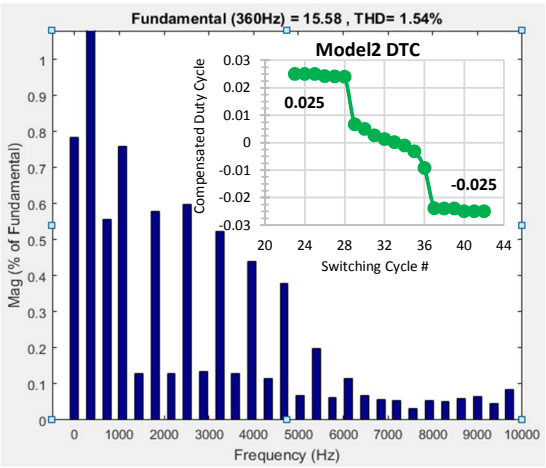
Table 1 shows the incremental improvement towards the ideal VSI case with each dead-time compensation scheme with the proposed scheme giving the best results. The reason for including the fundamental current value is voltage-second balancing mainly corrects average voltage/current error, which in turn would improve the fundamental voltage and current values closer to the ideal case. The classic model-based approach only considers the dead-time effect on the voltage-second error and needs a precise current sensing to know the current polarity. The newer model technique only considers the t_{vc} effect around the current zero-crossing along with the dead-time effect. The full monitoring technique considers the t_{d_off}, t_{vc}, and t_{dt} effect for the full fundamental cycle. The graph inside each chart is the compensated duty cycle values used around the current zero-crossing. Also, the charts are zoomed in to show the reduction in the low frequency harmonics around the fundamental frequency.

Table 1. Experimental results for output current characteristics of HB inverter under different DTC

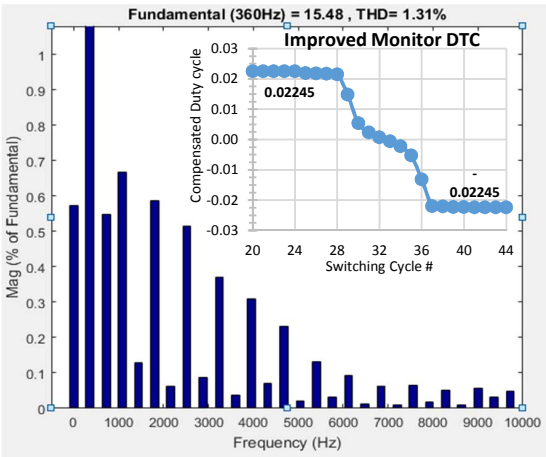
	Ideal VSI	No DTC	Model1 DTC	Model2 DTC	Monitor DTC
Fundamental Value	15.24 A	14.42 A	15.62 A	15.58 A	15.48 A
THD	0%	3.3%	1.73%	1.54%	1.31%



(a) Model-based compensation approach considering t_{dt}



(b) Model-based compensation approach considering t_{dt} and t_{vc}



(c) Monitor-based compensation approach considering t_{dt}, t_{vc}, and t_{d_off}

Fig. 9. Output inverter current THD results and DTC scheme to achieve it

V. Conclusion

A voltage-second balancing scheme is designed based upon an online condition monitoring system for SiC devices to improve power quality for VSIs. Voltage-second balancing can help mitigate the negative effects of dead-time, parasitic capacitance and switching time sensitivity in high frequency SiC VSIs. The online monitoring system distinguishes itself by also detecting current polarity based on the V_{ds} switching waveform, which eliminates the need for a current sensor that can be unreliable around the zero current crossing.

A 1 kW half-bridge inverter experimental test, switching at 50 kHz, was conducted to compare the results of different dead-time compensation implementations. The test results show a 70% enhancement on the error against the ideal fundamental current value of the output current and a 2% THD improvement on the output current low frequency harmonics. In addition, the monitoring feature enables the scheme to be load application independent, eliminate the need for precise current sensing, especially during zero-crossing, and improve over offline modeling for accurate and dynamic implementation.

Acknowledgment

The authors would like to thank II-VI Foundation and the DOE WBG Traineeship for its support of this research work. This work made use of the Engineering Research Center Shared Facilities supported by the Engineering Research Center Program of the National Science Foundation and DOE under NSF Award Number EEC-1041877 and the CURENT Industry Partnership Program.

References

[1] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics,* vol. 29, pp. 2155-2163, 2014.

[2] M. Ogawa, S. Ogasawara, and M. Takemoto, "A Feedback-Type Dead-Time Compensation Method for High-Frequency PWM Inverter; Delay and Pulse Width Characteristics," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 100-105.

[3] C. Li, Y. Gu, W. Li, X. He, Z. Dong, G. Chen, *et al.*, "Analysis and Compensation of Dead-Time Effect Considering Parasitic Capacitance and Ripple Current," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1501-1506.

[4] Z. Zhang and L. Xu, "Dead-Time Compensation of Inverters Considering Snubber and Parasitic Capacitance," *IEEE Transactions on Power Electronics,* vol. 29, pp. 3179-3187, 2014.

[5] Y. Wang, Q. Gao, and X. Cai, "Mixed PWM for Dead-Time Elimination and Compensation in a Grid-Tied Inverter," *IEEE Transactions on Industrial Electronics,* vol. 58, pp. 4797-4803, 2011.

[6] B. Liu, R. Ren, E. Jones, F. Wang, D. Costinett, and Z. Zhang, "A Modulation Compensation Scheme to Reduce Input Current Distortion in GaN Based High Switching Frequency Three-Phase Three-level Vienna Type Rectifiers," *IEEE Transactions on Power Electronics,* vol. 33, pp. 283-298, 2017.

[7] Y. Yang, K. Zhou, H. Wang, and F. Blaabjerg, "Harmonics Mitigation of Dead Time Effects In PWM Converters Using a Repetitive Controller," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 1479-1486.

[8] J. Yuan, Z. Zhao, B. Chen, C. Li, J. Wang, C. Tian, *et al.*, "An Immune-Algorithm-Based Dead-Time Elimination PWM Control

Strategy in a Single-Phase Inverter," *IEEE Transactions on Power Electronics,* vol. 30, pp. 3964-3975, 2015.

[9] W. Dafang, Y. Bowen, Z. Cheng, Z. Chuanwei, and Q. Ji, "A Feedback-Type Phase Voltage Compensation Strategy Based on Phase Current Reconstruction for ACIM Drives," *IEEE Transactions on Power Electronics,* vol. 29, pp. 5031-5043, 2014.

[10] Z. Zhang, B. Guo, F. Wang, L. M. Tolbert, B. J. Blalock, Z. Liang, *et al.*, "Impact of ringing on switching losses of wide band-gap devices in a phase-leg configuration," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 2542-2549.

[11] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Decoupling of Interaction between WBG Converter and Motor Load for Switching Performance Improvement," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 1569-1576.

[12] J. Dyer, Z. Zhang, F. Wang, D. Costinett, L. M. Tolbert, and B. J. Blalock, "Online Condition Monitoring Of SiC Devices Using Intelligent Gate Drive for Converter Performance Improvement," in *IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, pp. 182-187.

[13] L. Gang, W. Dafang, J. Yi, W. Miaoran, and Z. Peng, "Current-Detection-Independent Dead-Time Compensation Method Based on Terminal Voltage A/D Conversion for PWM VSI," *IEEE Transactions on Industrial Electronics,* vol. 64, pp. 7689-7699, 2017.